

international
**ELECTRON
DEVICES**
meeting

1992

SAN FRANCISCO, CA
DECEMBER 13-16, 1992

TECHNICAL DIGEST

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WELCOME FROM THE GENERAL CHAIRMAN

The Conference Committee and I welcome you to the 1992 IEEE International Electron Devices Meeting. This year the conference returns to San Francisco, California, and continues a 37-year tradition as a forum for the presentation of the latest research and development in the area of electron devices and their applications. The strong international nature of the IEDM is reflected in this year's exciting program which was selected from 659 submitted abstracts from 23 countries. While the majority of the abstracts were submitted from North America, papers were also submitted from Asia, Europe, South America, Australia, and Africa. A strong effort was made this year to solicit papers from eastern Europe. Industrial facilities generated the largest number of submitted abstracts but many were also submitted from Universities and government institutes. The area of greatest interest this year was Device Technology with 131 abstracts. Over 100 abstracts were also received in the areas of Modeling and Simulation, Quantum Electronics, and CMOS Devices. The total number of accepted abstracts this year was 223.

On Sunday, the 1992 IEDM will offer two short courses specially designed to enhance one's technical vitality. These courses are designed to broadly appeal to IEDM participants, including those unfamiliar with the topic areas. The courses are entitled, "Interconnect for the 90's", and "Reliability—Silicon to System Considerations". Both of these courses cover recent developments in their perspective areas as well as serving as tutorial and review courses.

The Tuesday luncheon will feature Mr. Jaron Lanier, President of VPL Research Inc., Foster City, California, who will discuss the topic of Virtual Reality. Mr. Lanier is a recognized authority in this area and has given numerous presentations on this subject and served on various panels discussing the uses and directions for Virtual Reality.

On behalf of the IEEE Electron Devices Society, which sponsors the IEDM, and Malcolm Thompson, Technical Program Chairman, I wish to express my sincere appreciation and congratulations to the members of the Conference Committee for the outstanding job they have done in planning and organizing the 1992 meeting. The authors are to be commended for their efforts in preparing and presenting the high-quality papers that form the foundation of this conference. It is with great pleasure that I extend a hearty welcome to them and to all of the attendees of the 1992 IEEE International Electron Devices Meeting.



Al Ipri
General Chairman



Malcolm Thompson
Technical Program
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General Chairman

SPECIAL PRESENTATIONS

PLENARY SESSION Monday, December 14

J. J. EBERS AWARD

To: Louis Parrillo and Richard Payne

The J.J. Ebers Award is given annually by the IEEE Electron Devices Society for outstanding technical contributions to electron devices. This year it is presented to:

PAUL RAPPAPORT AWARD

To: H. Fukuda, A. Imai, T. Terasawa and S. Okazaki Hitachi, Ltd.,
Tokyo, Japan

For the paper entitled: "New Approach to Resolution Limit and
Advanced Image Formation Techniques in Optical Lithography"

1991 ROGER A. HAKEN BEST STUDENT PAPER AWARD:

To: Elyse Rosenbaum
University of California, Berkeley, CA

For the paper entitled: "The Effects of Oxide Stress Waveform on
MOSFET Performance"

IEDM LUNCHEON Tuesday, December 15

1992 IEEE DAVID SARNOFF AWARD

To: J. Jim Hsieh
Lasertron, Inc., Burlington, MA

"For the invention and commercialization of the GaInAsP semicon-
ductor laser for fiber-optic communications"

1992 IEEE JACK A. MORTON AWARD

To: Takuo Sugano
Toyo University, Saitama, Japan

"For contributions to Metal-Insulator-Semiconductor devices and
technology"

LUNCHEON PRESENTATION

Virtual Reality: A presentation by Mr. Jaron Lanier, Chief Scientist and
Founder of VPL Research, Inc. on Virtual Reality.

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Seated from left to right: Jason Woo, Publicity Vice Chairman; Rick Sivan, Short Course Chairman; Malcolm Thompson, Program Chairman; Al Ipri, General Chairman; John Aitken, Program Vice Chairman; Alan Lewis, Publications Chairman; Steve Hillenius, Short Course Vice Chairman; John Kerr, International Arrangements Chairman. *Standing from left to right:* Bijan Davari, Subcommittee Chairman, Device Technology; Ken Galloway, Subcommittee Chairman, CMOS Devices; Martin Schmidt, Subcommittee Chairman, Detectors, Sensors, and Displays; Jim Sturm, Subcommittee Chairman, Solid State Devices; Stan Swirhun, Subcommittee Chairman, Quantum Electronics and Compound Semiconductors; Jim Paterson, Subcommittee Chairman, Integrated Circuits; Connor Rafferty, Subcommittee Chairman, Modeling and Simulation; Melissa Widerkehr, Conference Manager. *Not pictured:* Kazuhiko Hashimoto, International Arrangements Vice Chairman; Hans Stork, Publicity Chairman; Michael Gaitan, Treasurer; Richard Abrams, Subcommittee Chairman, Vacuum Electronics.

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Invited Papers

Chairman: M. Thompson, Xerox Palo Alto Research Center

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- 1.2 **Conducting Polymers: Novel Materials for Novel Devices**, A. Heeger, *Institute for Polymers and Organic Solids, University of California and UNIAx Corporation, Santa Barbara, CA*
- 1.3 **ULSI Technology Toward the Next Century: Driven by DRAMs or MPUs**, Y. Nishi, *Hewlett Packard, Palo Alto, California*

Session 2: Integrated Circuits—Advanced CMOS and BiCMOS Technologies

Monday, December 14, 1:00 p.m.

Grand Ballroom A

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H. Kirsch, Motorola Inc.

- 1:00 p.m.
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- 1:55 p.m.
2.3 **Integration of Power LDMOS into a Low-Voltage 0.5µm BiCMOS Technology**, P. Tsui, P. Gilbert and S. Sun, *Motorola Inc., Austin, TX*
- 2:20 p.m.
2.4 **A Low Power 0.25µm CMOS Technology**, P. Woerlee, C. Juffermans, H. Lifka, W. Manders, H. Pomp, G. Paulzen, A. Walker and R. Woltjer, *Philips Research Laboratories, Eindhoven, The Netherlands*
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2.5 **A High Speed SOI Technology with 12ps/18ps Gate Delay Operating at 5V/1.5V VDD**, J. Chen, J. King, S. Parke, F. Asaderaghi, P. Ko and C. Hu, *University of California, Berkeley, CA*
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2.6 **A 27 GHz Double Polysilicon Bipolar Technology on Bonded SOI with Embedded 58µm² CMOS Memory Cells for ECL-CMOS SRAM Applications**, T. Hiramoto, N. Tamba, M. Yoshida, T. Hashimoto, T. Fujiwara, K. Watanabe, M. Odaka, M. Usami and T. Ikeda, *Hitachi, Ltd., Tokyo, Japan*
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3.2 **Characterization of Super-Resolution Photolithography**, H. Fukuda, R. Yamanaka, T. Terasawa, K. Hama, T. Tawa and S. Okazaki, *Hitachi Ltd., Tokyo, Japan*
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J. Van der Spiegel, University of Pennsylvania

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Co-Chairmen: G. Hu, Cypress Semiconductor

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Monday, December 14, 1:00 p.m.

Continental Ballroom 7-9

Co-Chairmen: G. Scheitrum, Litton Systems E.D.D.

A. McCurdy, University of Southern California

1:00 p.m.

Introduction

1:05 p.m.

- 8.1 Experimental Investigation of a Broadband Two-Stage Tapered Gyro-TWT Amplifier**, J. Choi, SAIC, McLean, VA, G. Park, Omega-P, Inc., New Haven, CT, S. Park, Pohang Inst. of Sci. and Tech., Pohang, Korea, C. Armstrong and A. Ganguly, Naval Research Laboratory, Washington, DC and R. Kyser, B-K Systems, Rockville, MD 195

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- 8.2 Large Signal Simulation and Design of a 95 GHz Harmonic Gyrokystron Amplifier**, S. Begum, G. Scheitrum and B. Arfin, Litton Electron Devices, San Carlos, CA 199

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- 8.3 Design and Development of a Third Harmonic, 95 GHz Gyro-TWT**, W. DeLope, G. Hu, M. Mizuhara, J. Neilson and R. Schumacher, Varian Associates, Palo Alto, CA and C. Chong, A. Lin, N. Luhmann, Jr., D. McDermott and T. Stewart, University of California, Los Angeles, CA 203

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- 8.4 High Power Second Harmonic Gyro-TWT Amplifier**, Q. Wang, D. McDermott, C. Kou, A. Lin, K. Chu and N. Luhmann, Jr., University of California, Los Angeles, CA and J. Pretterbner, University of Stuttgart, Stuttgart, Germany 207

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- 8.5 Synchronous Mode Locking in Gyrotrons**, A. McCurdy, University of Southern California, Los Angeles, CA 211

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- 8.6 A Linearly Polarized Input Coupler for Slotted Waveguide Interaction Structures**, G. Park and J. Hirshfield, Omega-P, Inc., New Haven, CT and C. Armstrong, Naval Research Laboratory, Washington, DC, and R. Kyser, B-K Systems, Inc., Rockville, MD 215

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- 8.7 The Double Cusp Gyro-Gun**, K. Nguyen, D. Smithe and L. Ludeking, Mission Research Corporation, Newington, VA 219

Session 9: Solid State Devices—Power Devices and Integrated Circuits 223

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Imperial Ballroom

Co-Chairmen: J. Sutor, Motorola Inc.

G. Dolny, David Sarnoff Research Center

1:00 p.m.

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- 9.1 A 50V Smart Power Process with Dielectric Isolation by SI-MOX**, J. Weyers and H. Vogt, Fraunhofer Institute of Microelectronic Circuits and Systems, Duisburg, Germany 225

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- 9.2 Prospects of High Voltage Power ICs on Thin SOI (Invited Paper)**, A. Nakagawa, N. Yasuhara, T. Ogura, Y. Yamaguchi, T. Matsudai and I. Omura, Toshiba Corporation, Kawasaki, Japan 229

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- 9.3 Polycrystalline-Silicon Thin-Film Transistor Technology for Low Cost, High Power Integrated Circuits**, G. Dolny, A. Ipi and G. Nostrand, David Sarnoff Research Center, Princeton, NJ and C. Wheatley and P. Wodarczyk, Harris Semiconductor, Mountaintop, PA 233

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- 9.4 An Optimized RESURF LDMOS Power Device Module Compatible with Advanced Logic Processes**, T. Eiland, S. Malhi, O-K. Kwon, W. Bailey, W-T. Ng, M. Torreno and S. Keller, Texas Instruments, Inc., Dallas, TX 237

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- 9.5 IGBT Mode Turn-Off Thyristor (IGTT) Fabricated on SOI Substrate**, T. Ogura and A. Nakagawa, Toshiba Corporation, Kawasaki, Japan 241

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- 9.6 Dielectrically Isolated Lateral High Voltage P-i-N Rectifiers for Power ICs**, S. Sridhar, Y. Huang and B. Baliga, North Carolina State University, Raleigh, NC 245

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- 9.7 The Bilateral Emitter Switched Thyristor (BEST)**, J. Huang, Honeywell, Plymouth, MN 249

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- 9.8 Modeling and Analysis of Current Sensors for N-Channel, Vertical IGBTs**, T. Chow and Z. Shen, Rensselaer Polytechnic Institute, Troy, NY and D. Pattanayak, E. Wildi and M. Adler, General Electric Company, Schenectady, NY and B. Baliga, North Carolina State University, Raleigh, NC 253

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Co-Chairmen: C.Y. Lu, ERSO/ITRI

K. Chiu, Hewlett Packard

9:00 a.m.

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9:05 a.m.

- 10.1 A New Cylindrical Capacitor Using Hemispherical Grained Si (HSG-Si) for 256MbDRAMs**, H. Watanabe, T. Tatsumi, S. Ohnishi, T. Hamada, I. Honma and T. Kikkawa, NEC Corporation, Kanagawa, Japan 259

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- 10.2 A High-C Capacitor (20.4 fF/ μm^2) with Ultrathin CVD-Ta₂O₅ Films Deposited on Rugged Poly-Si for High Density DRAMs**, P. Fazan and V. Mathews, Micron Semiconductor, Inc., Boise, ID and N. Sandler, LAM Research Corporation, Fremont, CA and G. Lo and D. Kwong, University of Texas, Austin, TX 263

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- 10.3 ULSI DRAM Technology with Ba_{0.7}Sr_{0.3}TiO₃ Film of 1.3-nm Equivalent SiO₂ Thickness and 10-9A/cm² Leakage Current**, E. Fujii, Y. Uemoto, S. Hayashi, T. Nasu, Y. Shimada, A. Matsuda, M. Kibe, M. Azuma, T. Otsuki, and G. Kano, Matsushita, Osaka, Japan, M. Scott and L. McMillan, Symetrix Corporation, Colorado Springs, CO and C. Paz de Araujo, University of Colorado, Colorado Springs, CO 267

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- 10.4 High Quality Ultra Thin Si₃N₄ Film Selectively Deposited on Poly-Si Electrode by LPCVD with In Situ HF Vapor Cleaning**, M. Yoshimaru, N. Inoue, M. Itoh, H. Kurogi, H. Tamura, N. Hirasita, F. Ichikawa and M. Ino, Oki Electric Industry Co., Tokyo, Japan 271

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- 10.5 Trench Isolation with ∇ (NABLA)-Shaped Buried Oxide for 256Mega-Bit DRAMS**, K. Shibahara, Y. Fujimoto, M. Hamada, S. Iwao, K. Tokashiki and T. Kunio, NEC Corporation, Kanagawa, Japan 275

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- 10.6 A Poly-Buffer Recessed LOCOS Process for 256Mbit DRAM Cells**, N. Shimizu, Y. Naito, Y. Itoh, Y. Shibata, K. Hashimoto, M. Nishio, A. Asai, K. Ohe, H. Umimoto and Y. Hirofujii, Matsushita, Osaka, Japan 279

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Grand Ballroom B

Co-Chairmen: S. Wong, Stanford University

S. Chambers, Intel Corporation

9:00 a.m.

Introduction

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- 11.1 High Quality High Rate SiO₂ and SiN Room Temperature Formation by Utilizing High Excited Ions**, T. Fukuda, K. Saito, M. Ohue, K. Shima and M. Momma, Hitachi, Ibaraki, Japan 285

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- 11.2 "TOP-PECVD": A New Conformal Plasma Enhanced CVD Technology using TEOS, Ozone and Pulse-Modulated RF Plasma**, Y. Ikeda, K. Kishimoto, K. Hirose and Y. Numasawa, NEC Corporation, Kanagawa, Japan 289

9:55 a.m.

- 11.3 A Fully Planarized Multilevel Interconnection Technology Using Selective TEOS-Ozone APCVD**, M. Suzuki, T. Homma, H. Koga, T. Tanigawa and Y. Murao, NEC Corporation, Kanagawa, Japan 293

- 10:20 a.m.
11.4 CVD Cu Interconnections for ULSI, J. Cho, H. Kang, I. Asano and S. Wong, *Stanford University, Stanford, CA* **297**
- 10:45 a.m.
11.5 Damascene Stud Local Interconnect in CMOS Technology, F. White, W. Hill, S. Eslinger, E. Payne, W. Cote, B. Chen and K. Johnson, *IBM, Essex Junction, VT* **301**
- 11:10 a.m.
11.6 A Quarter-Micron Planarized Interconnection Technology with Self-Aligned Plug, K. Ueno, K. Ohto, K. Tsunenari, K. Kajiyana, K. Kikuta and T. Kikkawa, *NEC Corporation, Kanagawa, Japan* **305**

Session 12: Quantum Electronics and Compound Semiconductor Devices—Compound Semiconductor FETs

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Tuesday, December 15, 9:00 a.m.
Continental Ballroom 1-3

Co-Chairmen: L. Nguyen, Hughes Research Laboratories
 R. Surridge, Bell Northern Research

9:00 a.m.

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12.1 High Performance Heterojunction InGaAs/InP JFET Grown by MOCVD Using Tertiarybutylphosphine (TBP), M. Hashemi, J. Shealy, S. DenBaars and U. Mishra, *University of California, Santa Barbara, CA* **311**
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12.2 Anisotype-Gate Self-Aligned P-Channel Heterostructure Field-Effect Transistors, J. Abrokwa, J. Huang, W. Ooms and J. Hallmark, *Motorola, Inc. Tempe, AZ* **315**
- 9:55 a.m.
12.3 Very High Voltage AlGaAs/InGaAs Pseudomorphic Power HEMTs, M. Kao, S. Fu, P. Ho, P. Smith, P. Chao, K. Nordheden and S. Wang, *General Electric Company, Syracuse, NY* **319**
- 10:20 a.m.
12.4 0.25 μ m Gate Length N-InGaP/InGaAs/GaAs HEMT DCFL Circuit with Lower Power Dissipation than High-Speed Si CMOS Circuits, S. Kuroda, H. Suehiro, T. Miyata, S. Asai, I. Hanyu, M. Shima, N. Hara and M. Takikawa, *Fujitsu Laboratories, Atsugi, Japan* **323**
- 10:45 a.m.
12.5 A 150 GHz Sub-0.1- μ m E/D MODFET MSI Process, H. Rohdin and A. Nagy, *Hewlett-Packard, Palo Alto, CA* **327**
- 11:10 a.m.
12.6 0.7 Micron Gate Length Complementary $Al_{0.75}Ga_{0.25}As/In_{0.25}Ga_{0.75}As/GaAs$ HIGFET Technology for High Speed/Low Power Digital Circuits, D. Grider, J. Nohava, I. Mactaggart and J. Stronczek, *Honeywell, Bloomington, MN* and P. Ruden and R. Tran, *University of Minnesota, Minneapolis, MN* **331**

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Continental Ballroom 5

Co-Chairmen: A. Kamgar, AT&T Bell Laboratories
 L. Palkuti, Defense Nuclear Agency

9:00 a.m.

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13.1 Elimination of Bipolar-Induced Breakdown in Fully-Depleted SOI MOSFETs, E. Ver Ploeg and J. Plummer, *Stanford University, Stanford, CA* and T. Watanabe, *Toshiba Corporation* and N. Kistler and J. Woo, *University of California, Los Angeles, CA* **337**
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13.2 Quasi-SOI MOSFETs Using Selective Epitaxy and Polishing, C. Nguyen, S. Kuehne and S. Wong, *Stanford University, Stanford, CA* and P. Renteln, *National Semiconductor, Santa Clara, CA* **341**

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- 13.3 Novel Poly-Si/TiN Stacked-Gate Structure for Fully-Depleted SOI/CMOS**, J.-M. Hwang and G. Pollack, *Texas Instruments Inc., Dallas, TX* **345**

10:20 a.m.

- 13.4 Hot-Carrier Effects in Fully-Depleted SOI nMOSFETs**, L. Su, H. Fang, J. Chung and D. Antoniadis, *Massachusetts Institute of Technology, Cambridge, MA* **349**

10:45 a.m.

- 13.5 SOI Technology for High-Temperature Applications**, P. Francis, A. Terao, B. Gentinne, D. Flandre and J. Colinge, *UCL, Louvain-la-Neuve, Belgium* **353**

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- 13.6 Measurement and Modeling of Self-Heating Effects in SOI nMOSFETs**, L. Su, K. Goodson, D. Antoniadis, M. Flik and J. Chung, *Massachusetts Institute of Technology, Cambridge, MA* **357**

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 J. Wilson, NASA Lewis Research Center

9:00 a.m.

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14.2 Nanometer Scale Thin-Film-Edge Emitter Devices with High Current Density Characteristics, A. Akinwande, P. Bauhahn, T. Ohnstein and J. Holmen, *Honeywell, Bloomington, MN*, and H. Gray, *Naval Research Laboratory, Washington, DC* **367**
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14.3 Field Emission Imaging Study of Silicon Field Emitters, J. Liu and J. Hren, *North Carolina State University, Raleigh, NC* and C. Sune and G. Jones, *MCNC, Research Triangle Park, NC* and H. Gray, *Naval Research Laboratory, Washington, DC* **371**
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14.4 Complete Vacuum Microelectronic Structures Using GaAs, S. Bandy, C. Nishimoto, C. Webb and G. Zdasiuk, *Varian Associates, Palo Alto, CA* **375**
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14.5 Simulation of Thin Film Field Emitter Array Cathodes, R. True, *Litton Systems, San Carlos, CA* **379**
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14.6 Density-Gradient Analysis of Effects of Geometry on Field-Emitter Characteristics, M. Ancona, *Los Alamos, NM* **383**
- 11:35 a.m.
14.7 IC-Processed Hot-Filament Vacuum Microdevices, K. Williams and R. Muller, *University of Berkeley, Berkeley, CA* **387**

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Imperial Ballroom

Co-Chairmen: J. Burghartz, IBM T.J. Watson Research Center
 T. Yamaguchi, Tektronix Inc.

9:00 a.m.

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15.2 Sub-20psec ECL Circuits with 50GHz fmax Self-Aligned SiGe HBTs, F. Sato, T. Hashimoto, T. Tatsumi, H. Kitahata and T. Tashiro, *NEC Corporation, Kanagawa, Japan* **397**

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15.4 A High-Performance Low-Complexity Bipolar Technology Using Selective Collector Compensation, R. Taft, J. Hayden, D. Denning and H. Kirsch, *Motorola, Inc., Austin, TX* **405**

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15.5 Analytical Collector Current Density and Base Transit Time Models for High-Injection Regions, K. Suzuki, *Fujitsu Laboratories, Ltd., Atsugi, Japan* **409**

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15.6 A New Experimental Technique for Extracting Base Resistance and Characterizing Current Crowding Phenomena in Bipolar Transistors, G. Verzellesi, L. Vendrame, R. Turetta, P. Pavan and E. Zanoni, *Universita di Padova, Padova, Italy* and A. Chantre and A. Marty, *France Telecom, Meylan Cedex, France* and M. Cavone and R. Rivoir, *Tecnopolis CSATA, Bari, Italy* **413**

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Co-Chairmen: J. Jensen, Hughes Research Laboratories
P. Nuytens, Draper Laboratories

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- 2:20 p.m.
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16.2 64-Bits Integrated Light-Emitting Device Array with Shift Register Separated Self-Scanning Light Emitting Device (S-SLED), Y. Kusuda, N. Komaba, Y. Kuroda, S. Ohno and S. Tanaka, *Nippon Sheet Glass Co., Ibaraki, Japan* **427**

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16.3 Neuron-MOS Binary-Logic Circuits Featuring Dramatic Reduction in Transistor Count and Interconnections, K. Kotani, T. Shibata and T. Ohmi, *Tohoku University, Sendai, Japan* **431**

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16.4 Hardware-Backpropagation Learning of Neuron-MOS Neural Network, H. Ishii, T. Shibata, H. Kosaka and T. Ohmi, *Tohoku University, Sendai, Japan* **435**

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16.5 A New Structure for the Silicon Retina, C. Wu and C. Chiu, *National Chiao-Tung University, Taiwan, Republic of China* **439**

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Tuesday, December 15, 2:15 p.m.
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Co-Chairmen: R. Eklund, Texas Instruments, Inc.
A. Uchiyama, Oki Electric Industrial Co., Ltd.

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- 2:20 p.m.
17.1 Bipolar Technology for 0.5-Micron-Wide Base Transistor with an ECL Gate Delay of 21.5 Picoseconds, S. Nakamura, T. Toyofuku, M. Sueda, K. Hasegawa, I. Kato and T. Takada, *Fujitsu, Ltd., Kawasaki, Japan* **445**

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17.2 A High Performance BiCMOS Process Featuring 40 GHz/21ps, M. Kerber, E. Bertagnolli, R. Mahnkopf, J. Popp, A. Felder, H. Rein, A. Weisgerber and H. Klose, *Siemens AG, Munich, Germany* **449**

- 3:10 p.m.
17.3 A Versatile, SOI BiCMOS Technology with Complementary Lateral BJTs, S. Parke, F. Assaderaghi, J. Chen, J. King, C. Hu and P. Ko, *University of California, Berkeley, CA* **453**

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17.4 Kinetics of High Concentration Arsenic Deactivation at Moderate to Low Temperatures, S. Luning, P. Rousseau, P. Griffin and J. Plummer, *Stanford University, Stanford, CA*, and P. Carey, *Lawrence Livermore Laboratory, Livermore, CA* **457**

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17.5 Vertically Scaled, High Reliability EEPROM Devices with Ultra-Thin Oxynitride Films Prepared by RTP in N₂O/O₂ Ambient, U. Sharma, R. Moazzami, P. Tobin, Y. Okada, S. Cheng, J. Yeargain, *Motorola, Inc., Austin, TX* **461**

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17.6 High-Performance Scaled Flash-Type EEPROMs with Heavily Oxynitrided Tunnel Oxide Films, H. Fukuda, A. Uchiyama, T. Kuramochi, T. Hayashi, T. Iwabuchi, T. Ono and T. Takayashiki, *Oki Electric Industry Company, Ltd., Tokyo, Japan* **465**

- 4:50 p.m.
17.7 A MOSFET with Si-implanted Gate-SiO₂ Insulator for Non-volatile Memory Applications, T. Hori, T. Ohzone, Y. Odake, and J. Hirase, *Matsushita Electric Industrial Company, Ltd., Osaka, Japan* **469**

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Tuesday, December 15, 2:15 p.m.
Continental Ballroom 1-3

Co-Chairmen: J. Randall, Texas Instruments
M. Dutta, U.S. Army ETDL

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18.1 Monolithic Integration of InGaAs/InAlAs Resonant Tunneling Diode and HEMT for Single-Transistor Cell SRAM Application, Y. Watanabe, Y. Nakasha, K. Imanishi and M. Takikawa, *Fujitsu, Atsugi, Japan* **475**

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18.2 Observation of Zero-Bias Multi-State Behavior in Selectively Doped Two-Terminal Quantum Tunneling Devices, K. Gullapalli, A. Tsao and D. Neikirk, *University of Texas, Austin, TX* **479**

- 3:10 p.m.
18.3 Hybrid RBT with Resonant-Tunneling-Diode and Hetero-Bipolar-Transistor in InP Substrate, A. Miura, T. Yakihara, S. Kobayashi, S. Oka, A. Nonoyama and T. Fujita, *Teratec Corporation, Tokyo, Japan* **483**

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18.4 Single-Electron Switch for Phase-Locked Single-Electron Logic Devices, K. Nakazato and J. White, *Hitachi Cambridge Laboratory, Cambridge, UK* **487**

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18.5 Three-Terminal Operation of a Quantum Interference Device Using a Quantum Wire with a Novel Stub Structure, K. Aihara, M. Yamamoto and T. Mizutani, *NTT LSI Laboratories, Kanagawa, Japan* **491**

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18.6 A Novel Analog-to-Digital Conversion Architecture Using Electron Waveguides, C. Eugster, P. Nuytens and J. del Alamo, *Massachusetts Institute of Technology, Cambridge, MA* **495**

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G.B. Hocker, Honeywell

2:15 p.m.

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- 19.1 A Low Cost Monolithic Accelerometer; Product/Technology Update**, S. Sherman, W. Tsang, T. Core, D. Quinn, R. Payne, K. Chau, J. Farash and S. Baum, *Analog Devices Semiconductor, Wilmington, MA* 501

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- 19.2 Quality Factor Control for Micromechanical Resonators**, C. Nguyen and R. Howe, *University of California, Berkeley, CA* 505

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- 19.3 Micro-Machined Array Probe Card**, M. Beiley and S. Wong, *Stanford University, Stanford, CA* 509

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- 19.4 Two-Dimensional Numerical Analysis of Novel Magnetotransistor with Partially Removed Substrate**, C. Riccobene, G. Wachutka and H. Baltes, *Swiss Federal Institute of Technology, Zurich, Switzerland* 513

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- 19.5 Multiple-Gate Split-Drain MOSFET Magnetic-Field Sensing Device and Amplifier**, F. Kub and C. Scott, *Naval Research Laboratory, Washington, DC* 517

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- 19.6 Robust, Wide-Range Hydrogen Sensor**, J. Rodriguez, R. Hughes, W. Corbett and P. McWhorter, *Sandia National Laboratories, Albuquerque, NM* 521

Session 20: CMOS Devices and Reliability—Hot Carrier Effects I

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Tuesday, December 15, 2:15 p.m.

Continental Ballroom 5

Co-Chairmen: P. Ko, University of California, Berkeley
S. Lai, Intel Corporation

2:15 p.m.

Introduction

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- 20.1 Photon Emission from 70nm Gate Length MOSFETs**, H. Kurino, H. Hashimoto, Y. Hiruma, T. Fujimori and M. Koyanagi, *Hiroshima University, Hiroshima, Japan* 1015

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- 20.2 A Two-Dimensional Analysis of Hot-Carrier Photoemission from LOCOS- and Trench-Isolated MOSFETs**, T. Ohzone and H. Iwata, *Toyama Prefectural University, Toyama, Japan* and Y. Uraoka and S. Odanaka, *Matsushita Elec. Ind. Company, Ltd., Osaka, Japan* 527

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- 20.3 Hot-Carrier Degradation of p-MOSFETs in Analog Operation: The Relevance of the Channel-Length-Independent Drain Conductance Degradation**, R. Thewes, M. Brox, G. Tempel and W. Weber, *Siemens AG, Munich, Germany* and K. Gosser, *Universitat Dortmund, Dortmund, Germany* 531

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- 20.4 Universal Description of Hot-Carrier-Induced Interface States in NMOSFETs**, R. Woltjer and G. Paulzen, *Philips Research Laboratories, Eindhoven, The Netherlands* 535

4:00 p.m.

- 20.5 Prediction of Hot-Carrier Degradation in Digital CMOS VLSI by Timing Simulation**, E. Minami, K. Quader, P. Ko and C. Hu, *University of California, Berkeley, CA* 539

4:25 p.m.

- 20.6 Self-Consistent Simulation of Hot-Carrier Damage Enhanced Gate Induced Drain Leakage**, A. Schwerin, W. Bergner and H. Jacobs, *Siemens AG, Munich, Germany* 543

4:50 p.m.

- 20.7 A New Bi-directional PMOSFET Hot-Carrier Degradation Model for Circuit Reliability Simulation**, C. Li, K. Quader, E. Minami, C. Hu, and P. Ko, *University of California, Berkeley, CA* 547

Session 21: Modeling and Simulation—Physical Device Models and Ultrasmall Devices

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Tuesday, December 15, 2:15 p.m.

Continental Ballroom 6

Co-Chairmen: R. Green, Intel Corporation
M. Lundstrom, Purdue University

2:15 p.m.

Introduction

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- 21.1 Monte Carlo Simulation of a 30 nm Dual-Gate MOSFET: How Short Can Si Go?**, D. Frank, S. Laux and M. Fischetti, *IBM, Yorktown Heights, NY* 553

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- 21.2 Molecular-Dynamics Study of Single-Electron Phenomena—Impact of Charge Quantization on 1-100 nm Si-MOSFETs**, K. Yano and K. Seki, *Hitachi Central Research Laboratory, Tokyo, Japan* and D. Ferry, *Arizona State University, Tempe, AZ* 557

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- 21.3 Lattice Wigner Simulations of Quantum Devices**, D. Miller and D. Neikirk, *University of Texas, Austin, TX* 561

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- 21.4 New Algorithm Simulation for Mesoscopic Electron Wave Devices Employing High Mobility 2D Electron Gas**, T. Usuki, M. Takatsu, M. Saito, M. Okada and N. Yokoyama, *Fujitsu Laboratories, Ltd., Atsugi, Japan* 565

4:00 p.m.

- 21.5 A Physical Model for MOSFET Output Resistance**, J. Huang, Z. Liu, P. Ko and C. Hu, *University of California, Berkeley, CA* and M. Jeng, *Cadence Design Systems, Santa Clara, CA* 569

4:25 p.m.

- 21.6 A New Analytical Model and the Impact of Base Charge Storage on Base Potential Distribution, Emitter Current Crowding and Base Resistance**, T. Chiu, P. Tien, J. Sung and T. Liu, *AT&T Bell Laboratories, Holmdel, NJ* 573

4:50 p.m.

- 21.7 A Physical SiGe-Base HBT Model for Circuit Simulation and Design**, G. Hong and J. Fossum, *University of Florida, Gainesville, FL* and M. Ugajin, *NTT LSI Laboratories, Atsugi-shi, Japan* 577

5:15 p.m.

- 21.8 HEMT Short-gate Noise Modeling and Parametric Analysis of NF Performance Limits**, F. Bonani, G. Ghione and C. Naldi, *Politecnico di Torino, Torino, Italy*, and R. Schnell and H. Siweris, *Siemens R & D, Munich, Germany* 581

Session 22: Evening Panel Discussion

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Tuesday, December 15, 8:00 p.m.

Continental Ballroom 4

Information Systems and the Semiconductor Industry

Panel Moderator: L. Terman

IBM

Yorktown Heights, NY

Session 23: Evening Panel Discussion

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Tuesday, December 15, 8:00 p.m.

Continental Ballroom 5

Panel Organizers: The Berkeley Roundtable

The Electronics Industry and the New World Order: Technology, Politics and Industrial Competition