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on

**Multichip Modules and High
Density Packaging**

MCM 98

April 15-17, 1998

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Denver, Colorado**

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1998

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Sponsored by:



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Proceedings

1998 International Conference on Multichip Modules and High Density Packaging

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Message from the General Chair

Welcome to the 7th International Conference and Exhibition on MCMs and High Density Packaging. This is your opportunity to see leading edge products from more than 74 exhibitors and hear the latest technology presentations from over 100 speakers. Six Professional Development Courses are also offered by industry experts to provide an in-depth treatment of timely topics. In addition, the social functions hosted as part of the conference will provide you the opportunity to network with the leaders in this industry. With over 1,000 attendees, this is the industry's largest Conference dedicated to MCMs and high density packaging.

Now in its 7th year, the Conference name has been expanded to reflect the evolution in technology and applications since 1992. The MCMs most commonly envisioned in 1992 interconnected 60 to 100 chip on a thin film substrate. While this vision was achieved, alternatives were also developed to achieve the optimum balance of density, cost and performance for a particular application. For example, the advent of the ball grid array package opened the door for few chip PBGA packages. As a second example, high density substrate technologies developed to address the wiring density demands of MCMs are now being used to interconnect chipscale packages or flip chips with traditional SMT. All of these technologies are interrelated and focused toward common goals. Although the Conference has addressed both MCMs and other high density packaging approaches in its technical program in recent years, the Conference name did not properly reflect this fact. Technical sessions this year on ChipScale Packages (CSP), High Density Interconnect on Flex, and Integrated Passives along with presentations throughout the other sessions, reflect the broader, interrelated approaches to high density packaging.

The Adam's Mark Hotel has completed their renovations and expansion. The Conference registration, technical sessions and exhibits will all be adjacent and on the same level in the hotel. You will enjoy the conveniences of the hotel and its location in the heart of Denver.

The Conference Committee, Session Chairs, Speakers and Exhibitors have all worked very hard to make this Conference a success. I hope you will join with me in extending thanks to them for their hard work.

Again, Welcome to Denver and the 7th International Conference and Exhibition on MCMs and High Density Packaging. Enjoy yourself and discover the latest technology in this rapidly evolving field.

R. Wayne Johnson
Auburn University

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1997 BEST PAPER AWARDS

BEST PAPER OF THE CONFERENCE

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R.G. Arnold, C.C. Faulkner, D.J. Pedder, Mitel Semiconductor

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Christopher D. Cotton and Dennis R. Kling, Raytheon Company; George Sebesta, CECOM RDEC AMSEL-RD-AS-BE

DESIGN CONSIDERATIONS FOR USING INTEGRATED PASSIVE COMPONENTS

James P. Parkerson, Leonard W. Schaper, University of Arkansas (HiDEC); Timothy G. Lenihan, Sheldahl Corporation

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R.G. Arnold, C.C. Faulkner, D.J. Pedder, Mitel Semiconductor

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BUILDING A DOMESTIC HIGH DENSITY FLIP CHIP ORGANIC SUBSTRATE CAPABILITY: ITRI/SEMATECH CHIP CARRIER PROJECT

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Abstract

In 1996, SEMATECH the US consortium for semiconductor R&D, and the Interconnection Technology Research Institute (ITRI) the US consortium for interconnection R&D, joined forces to address the need for sources of high density organic substrates for direct flip chip attach. These substrates are to be used to manufacture BGA packages or multi chip modules for high pincount (500 I/O and greater) flip chip die at a cost competitive with ceramic packages. The joint effort has progressed from technical discussions between the semiconductor manufacturers and the Printed Wiring Board (PWB) fabricators, to the design, manufacture, and test of very high density BGA organic substrates.

This paper reviews the problem being addressed and the goals and approach of the project. The designs of both the phase 1 test vehicle and the phase 2 test are described, together with a discussion of the trade-offs and lessons learned. Results of the phase 1 build together with descriptions of the substrate technologies included are reviewed. Substrate flatness tests, moisture resistance tests, and a series of environmental stress tests, including temp cycle, pressure cooker, and 85/85 were performed on the test vehicles. Results of those tests are summarized. Finally, a description of the phase 2 plan and status will be presented.

Key Words: Microvia, Flip Chip, BGA, Substrate, Substrate Design

Introduction

The need for smaller, lighter electronics assemblies, primarily for the fast growing portables market, and the rapidly increasing I/O count of semiconductor devices has created a revolution in the semiconductor packaging industry. The traditional molded leadframe plastic encapsulated semiconductor package cannot effectively handle array pinouts, particularly in I/O counts above 500. At the same time, market factors have created an opportunity to return semiconductor assembly to the U.S., most of which is currently done off shore.

Recognizing this, SEMATECH and ITRI, R&D consortia serving the domestic semiconductor and interconnect industries respectively, joined forces to work towards establishing a domestic capability to provide low cost, high density substrates for Ball Grid Array (BGA) and Chip Scale (CS) packages utilizing high density Printed Wiring Board (PWB) microvia technology.

Semiconductor industry motivation –

Semiconductor suppliers are interested in this activity for the following reasons:

- Understanding of BGA package manufacturing and reliability issues
- Design and layout tradeoffs

- Package material source based on U.S. currency
- Evaluate various substrate technologies
- "Build where you sell" driving the need for domestic assembly.
- Local source for quick turn and prototype packages.

PWB suppliers motivation –

Manufacturers of PWBs are interested for the following reasons:

- The market for PWBs as platforms for semiconductor chip packaging is predicted to grow from about \$800 million in 1997 to around \$17 billion world wide by 2007 [1]
- The value of a square inch of PWB used in semiconductor packaging applications is significantly higher than a square inch of PWB used in a conventional application
- This represents totally new business for PWB manufacturers, not just market share to be passed around
- Semiconductor suppliers are new customers with new applications not familiar to the domestic PWB suppliers

A joint development program is an excellent way for both sides to work together to rapidly gain the knowledge they need to meet their future needs.

Approach

The project team chose an approach similar to that used in the ITRI October Project Microvia evaluation [2]. This consists of the definition and design of a test vehicle by the users (in this case the semiconductor suppliers) which represents their future needs and incorporates the expected technical challenges. The PWB fabricators then build this vehicle and the team assembles and subjects it to a series of tests and evaluations.

In the first phase of the program, bare daisy chained substrates were fabricated and tested. In the second phase, the test vehicle was redesigned based on our experience in the first phase. Fully functional parts were then assembled using test die and mounted to boards for test.

Phase I Results

Although Phase I was to be a substrates only build and test, the test vehicle design was chosen to match the test die to be used in the Phase II build. The test die is a device designed and manufactured by Sandia. In the implementation used in this program, the device has 1000 I/Os which are pinned out in a flip chip solder bump array. Two devices were to be used in Phase II, each with the same die size, pin count and pinout placement. The first device incorporates active structures such as stress sensors, heaters, and ring oscillators as well as a number of pins daisy chained together for continuity measurements. The second device has all pins daisy chained together.

Substrate design

A square grid chip pad layout was used with the signal I/O on 250 micron pitch, and the power and ground connections on 500 micron in the center of the array (figure 1). A 35 millimeter (mm) package body size was chosen with BGA pads on 1 mm pitch.

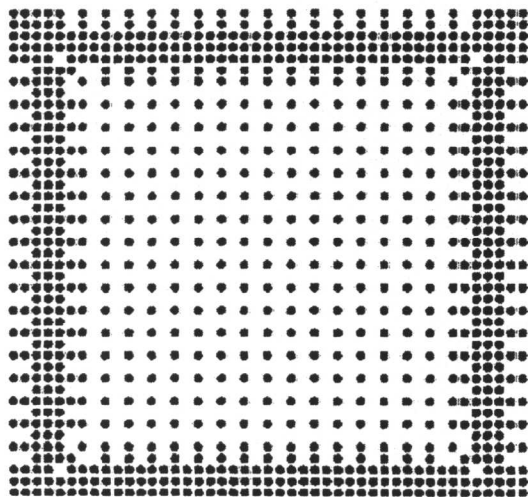


Figure 1

This resulted in an eight layer substrate with 75 micron lines and spaces for fanout typical, and 62.5 micron smallest. The internal two layers for power and ground were constructed using a conventional 2 sided PWB laminate with 200 micron drilled holes and 350 micron capture pads. Three layers of microvia build up were fabricated on both sides of this core. The microvias were 75 micron in diameter in 150 micron capture pads. Both the flip chip pads and the BGA pads used microvias in the pads. (see figure 2a and 2b).

8 Layer Substrate Cross Section

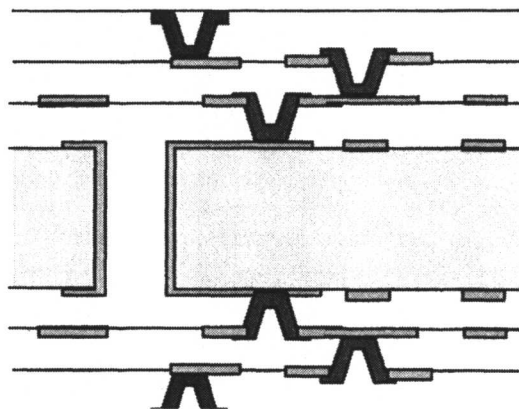


Figure 2a

BGA Substrate Fan Out

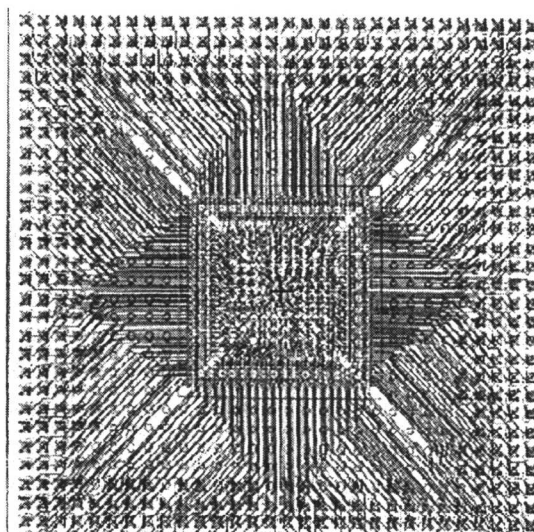


Figure 2b

Several different fabricators manufactured the substrates using their own microvia technology. Variations included photoimaged approaches, laser drilled microvias, and screen printed filled vias.

Finished substrates were measured for flatness over temperature, moisture resistance, and performance through a series of environmental stresses.

The substrate design proved to be a significant challenge for the fabricators. The combination of fine lines, small pads, small vias, with 3 build up layers on each side of a drilled core, represents one of the most complex microvia substrates ever fabricated. In spite of this, four different domestic manufacturers were able to deliver parts for testing. These parts represent the state-of-the-art in microvia technology today.

Flatness measurement

A shadow Moire technique was used to measure flatness [3]. Parts were measured at four temperature points: 26 degrees C initial, 225 degrees C peak, 183 degrees C cooling, and 26C degrees final, to evaluate performance through the assembly process. Figures 3a&b shows a representative scan and 2 dimensional plot generated.

T = 26 °C Initial

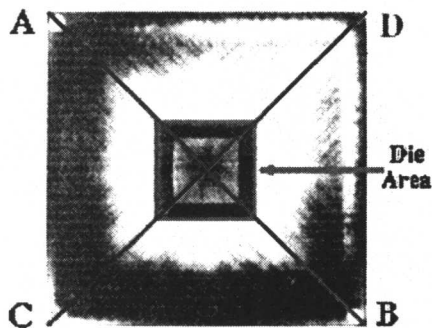


Figure 3a

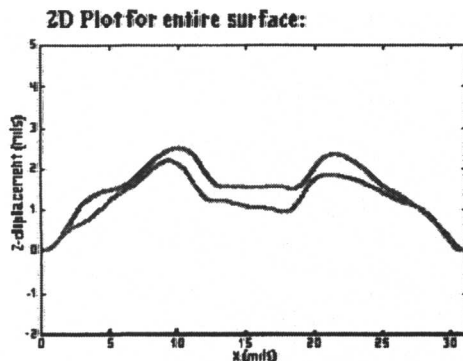


Figure 3b

Parts differed significantly between fabricators in flatness over temperature. The best showed total distortion in the order of a few

thousands of an inch (mils), and were very stable over temperature. The worst displayed bow and twist of over 25 mils, and changed dramatically through temperature cycling. Figure 4 is a graph summarizing the measurements for twist for the four manufacturers samples.

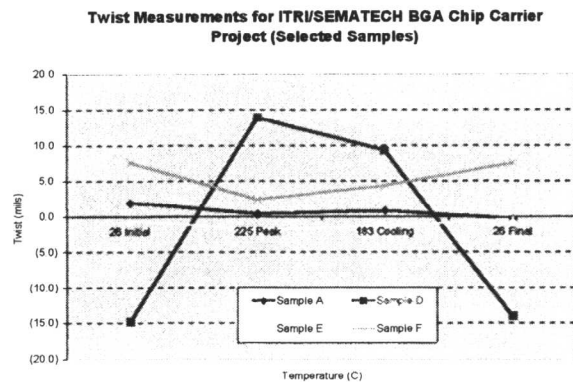


Figure 4

Although it is suspected that the bow and twist exhibited by the most extreme samples would impact assembly yields of both the flip chip die to substrate and substrate to board, the extent of this impact is not known. In the second phase of the project, assembly yields will be monitored and related to measurements of flatness.

Moisture Resistance

Moisture resistance performance was measured to J-STD-020 requirements, utilizing a reflow simulation unit and real-time deformation measurement system [4]. Visual examination and scanning acoustic microscopy was then used to verify failures and locate failure points. Samples were first preconditioned to level 3 requirements and subjected to simulated reflow. If they passed, additional parts were then preconditioned to level 2 and level 1 until failures occurred.

Samples representing five different material combinations from four different fabricators were tested. One sample variation failed under level 3 conditions. Three variations failed at level 1, and one sample variation showed no moisture sensitivity.

Normally, moisture resistance is performed on the finished encapsulated package. Due to the developmental nature of the materials and technologies used to fabricate the BGA substrates, the project team decided to first evaluate the bare substrates. Obviously, if the bare substrate could not pass moisture resistance, then the encapsulated package could not be expected to pass. This