GaAs IC SYMPOSIUM

IEEE GALLIUM ARSENIDE INTEGRATED CIRCUIT SYMPOSIUM
Co-Sponsored by The IEEE Electron Devices Society,
The IEEE Microwave Theory and Techniques Society, and
The IEEE Solid-State Circuits Society

23rd
Annual

TECHNICAL DIGEST 2001

BALTIMORE, MARYLAND

OCTOBER 21-24, 2001

01CH37191

GaAs IC SYMPOSIUM

IEEE GALLIUM ARSENIDE INTEGRATED CIRCUIT SYMPOSIUM
Co-Sponsored by The IEEE Electron Devices Society,
The IEEE Microwave Theory and Techniques Society, and
The IEEE Solid-State Circuits Society

23rd
Annual

TECHNICAL DIGEST 2001

BALTIMORE, MARYLAND

OCTOBER 21 – 24, 2001

01CH37191

GaAs IC Symposium - IEEE Gallium Arsenide Integrated Circuit Symposium

IEEE Catalog Number 01CH37191

ISBN: 0-7803-6663-8 (Softbound Edition)
0-7803-6664-6 (Microfiche Edition)

ISSN: 1064-7775

Additional copies can be ordered from

IEEE Service Center
445 Hoes Lane
P.O. Box 1331
Piscataway, NJ 08855-1331

1-800-678-IEEE
1-732-981-1393
1-732-981-1721 (FAX)

Welcome to the 2001 IEEE GaAs IC Symposium

On behalf of the organizing committee and the IEEE EDS, MTT-S and SSCS, it's my pleasure to the 23rd IEEE GaAs IC Symposium in the Renaissance Harborplace Hotel, overlooking the inner harbor in Baltimore.

Over the last 23 years, the IEEE GaAs IC Symposium has become the preeminent international forum on developments in high speed integrated circuits using GaAs, InP, SiGe, GaN, SiC and other compound semiconductors. In 2001, the Symposium continues its tradition of presenting the best from around the world in high frequency microelectronics. Major focus areas of this year's GaAs IC Symposium, organized by Tim Henderson and the Technical Program Committee, include state-of-the-art circuits and technology for:

- Wireless and broadband communications
- Very high-speed optical communications
- Highly-efficient, linear, power amplifiers
- Optoelectronics for optical interconnect
- Millimeter-wave systems

The technical sessions will highlight all aspects of technology: device development and fabrication, characterization and modeling, IC design and testing, high volume manufacturing, reliability, and system applications.

The 23rd IEEE GaAs IC Symposium continues our tradition of providing focused educational opportunities through our Short Course and Primer Course, both held on Sunday, October 21st. Chris Bozada has organized a very interesting and highly applicable one-day Short Course on 'Optical Fiber Systems' taught by five industry experts. In addition, Stephen Long and Donald Estreich will once again present our Primer Course, which is not only an excellent tutorial but is presented within the context of this year's symposium contents.

You have the opportunity to learn of new products from the approximately 40 exhibitors in the GaAs IC Technology Exhibition and potential customers for the latest commercially available GaAs ICs can hear about these in the Vendor Product Forum.

To complement the full technical program, we have provided several social events to allow interactions with colleagues while catching up with the newest technology available on the market. These events include the Sunday evening Opening Reception, the Monday evening Technology Exhibition Reception, and the Tuesday evening of fun, science and an Imax movie at the Baltimore Science Center.

It's my happy duty to announce the winners of our 4th Outstanding Paper Award from the 2000 Symposium - *M. Sokolich, C. Fields, B. Shi, Y. K. Brown, M. Montes, R. Martinez, A. R. Kramer, S. Thomas III & M. Madhav* of HRL Laboratories for their paper **'A Low Power 72.8 GHZ Static Frequency Divider Implemented in AlInAs/InGaAs HBT IC Technology'**.

I'd like to thank the members of the Technical Program Committee, Overseas Advisors, and the Executive Committee who volunteer their time to ensure that this symposium is the best it can be.

We're pleased you've chosen to join us in Baltimore for the 23rd IEEE GaAs IC Symposium.

John Sitch
Chairman
2001 IEEE GaAs IC Symposium

2001 IEEE GaAs IC Symposium Organizers

EXECUTIVE COMMITTEE

John Sitch
Symposium Chairman
Nortel Networks
Ottawa, Ont., Canada

Tim Henderson
Technical Program Chairman
TriQuint Semiconductor Texas
Dallas, TX

Chris Bozada
Technical Program Vice Chairman
Air Force Research Lab
WPAFB, OH

Mohammad Madihian
Publications Chairman
NEC USA Inc.
Princeton, NJ

Brad Nelson
Local Arrangements
Stanford Microdevices
Sunnyvale, CA

Mitch Shifrin
Publicity Chairman
Hittite Microwave
Woburn, MA

Bill Peatman
Symposium Secretary
Anadigics Inc.
Warren, NJ

Kevin Kobayashi
Symposium Treasurer
Stanford Microdevices
Long Beach, CA

Dave Osika
Webmaster & Electronic Media
Anadigics Inc.
Warren, NJ

OVERSEAS ADVISORS

Derek Abbot
University of Adelaide
AUSTRALIA

Mohammad Madihian
NEC USA, Inc.
Princeton, NJ

Yasuro Yamane
NTT Photonics Labs
Atsugi-shi, Kanagawa, JAPAN

Marc Rocchi
OMMIC
Limeil Brevannes, FRANCE

Jan-Erik Mueller
Infineon AG
Munich, GERMANY

IEEE ADVISORS

Fazal Ali
MTT-S Liaison
Nokia
San Diego, CA

Herbert S. Bennett
EDS Liaison
NIST
Gaithersburg, MD

TECHNICAL PROGRAM COMMITTEE

Derek Abbott
University of Adelaide
Allan Armstrong
Vitesse Semiconductor
Chris Bozada
US Air Force
Young-Kai Chen
Lucent Technologies
Norman Chiang
California Eastern Laboratories
Steve Consolazio
Northrop Grumman
Beth Glass
Motorola
Dave Halchin
RF Micro Devices
Tim Henderson
TriQuint Semiconductor Texas
Vincent Hietala
Quellan Inc.
Tony Immorlica
Sanders, a Lockheed Martin Company

Kevin Kobayashi
Stanford Microdevices
Zhihao Lao
OpNext Inc.
Mohammad Madihian
NEC USA Inc.
Pierre Mandeville
Nortel Networks
Mehran Mokhtari
HRL Laboratories
Jan-Erik Mueller
Infineon Technologies
Brad Nelson
Stanford Microdevices
The'Linh Nguyen
Finisar Corporation
Dave Osika
Anadigics Inc.
Bert Oyama
TRW S&EG
Bill Peatman
Anadigics Inc.

Marc Rocchi
OMMIC, Limeil
Mitchell Shifrin
Hittite Microwave Corp.
Tim Shirley
Agilent
John Sitch
Nortel Networks
Marko Sokolich
HRL Laboratories
Jim Sowers
Space Systems/Loral
Malcolm Stubbs
Communications Research Centre
Benjamin Tang
Primarion
Tho Vu
Top-Vu Technology, Inc
Walter Wohlmuth
TriQuint Semiconductor
Yasuro Yamane
NTT Photonics Labs

CONSULTANTS

Harry Kuemmerle, III
Diane Conti
Meeting & Exhibit Management
VIP Meetings & Conventions
Pacific Palisades, CA

Mary Clemente
Registrar and Publishing
IEEE
Piscataway, NJ

SYMPOSIUM HEADQUARTERS

The Renaissance Harborplace Hotel
202 East Pratt Street
Baltimore, MD 21202

CONTENTS

SESSION C

Monday, October 22, 2001 - 3:00 p.m.

Single & Multi-Channel Opto- Electronics

Chairpersons: The'Linh Nguyen, *Finisar Corp*
Benjamin Tang, *Primarion*

SESSION D

Tuesday, October 23, 2001 – 8:30 a.m.

HBT Amplifiers

Chairpersons: Kevin Kobayashi, *Stanford Microdevices*
David Osika, *Anadigics*

SESSION E

Tuesday, October 23, 2001 – 8:30 a.m.

Physical Layer IC's For 10 & 40 GB/s Optical Communications

Chairpersons: Allan Armstrong, *Vitesse Semiconductor*
Mehran Mokhtari, *HRL Laboratories*

SESSION F

Tuesday, October 23, 2001 – 10:30 a.m.

Power Amplifier Applications

Chairpersons: Norman Chiang, *California Eastern Labs*
Dave Halchin, *RF Micro Devices*

SESSION G

Tuesday, October 23, 2001 – 10:30 a.m.

Transceiver Components For 40GB/s Optical Communications

Chairpersons: Tho Vu, *Top-Vu Technology*
Zhihao Lao, *OpNext*

VENDOR PRODUCT FORUM
Wireless' Latest and Greatest

Tuesday, October 23, 2001 – 1:30 p.m.

Organizers/Moderators: Bill Peatman, *Anadigics Inc.*
Norman Chiang, *California Eastern Labs*

The wireless industry is on the verge of a major revolution in technology and applications. The handset power amplifier itself is undergoing rapid change in many of it's attributes. This forum will review recent wireless product developments from some of the leaders in the industry. Questions we hope to address include 1) What recent improvements have been made to the HBT regarding performance and reliability, 2) Is there a role for Enhancement Mode FETs as alternatives to the HBT, 3) What are the technology choices for 2.5 and 3G handset power amplifiers, 4) How much integration inside the PA module is required, and 5) What new material developments may impact wireless development going forward.

Forum Members:

Charles Krumm	*Conexant Systems*
Damian McCann	*Celeriteck*
Jennifer Palella	*Anadigics*
Peter Sahjani	*Agilent Technologies*
Roger Welser	*Kopin Corporation*

PANEL SESSION 3

Tuesday, October 23, 2001 – 1:30 p.m.

40 Gb/s IC's

Organizers/Moderators:
Tho Vu, *Top-Vu Technology*
Marko Sokolich, *HRL Laboratories*
Zhihao Lao, *OpNext Inc.*

To continue on a high-interest panel from last year on "Industry Roadmap to 40Gb/s", this year we'll focus on the integrated circuits for 40 Gbps systems. Following are some of the questions that we'll try to address: How will such data rates be achieved? What process technologies will be successful? What circuit techniques will be used? When will such products be manufacturable and reliable? Is expectation outrunning the technical capability? Does demand exceed capacity? Is there a need in the US and throughout the world? What is driving to 40 Gbps?

Panel Members:

Hisao Shigematsu	*Fujitsu*
Greg Freeman	*IBM*
Y.K. Chen	*Lucent*
John Sitch	*Nortel Networks*
Marc Rocchi	*OMMIC*
Dwight Streit	*TRW*

SESSION H

Tuesday, October 23, 2001 – 3:30 p.m.

Next Generation RF Technologies

Chairpersons: Malcolm Stubbs, *Communication Research Centre*
Steve Consolazio, *Northrop Grumman*

SESSION I

Tuesday, October 23, 2001 – 3:30 p.m.

Device Modeling & Reliability

Chairpersons: Beth Glass, *Motorola*
Bill Peatman, *Anadigics*

SESSION J

Wednesday, October 24, 2001 – 8:30 a.m.

HBT Technologies

Chairpersons: Jan-Erik Mueller, *Infineon Technologies*
Young-Kai Chen, *Lucent Technologies*

SESSION K

Wednesday, October 24, 2001 – 8:40 a.m.

Power Amplifier Techniques

Chairpersons: Mitchell Shifrin, *Hittite Microwave Corp*
Brad Nelson, *Stanford Microdevices*

SESSION L

Wednesday, October 24, 2001 – 10:30 a.m.

Packaging & Technology

Chairpersons: Tony Immorlica, *BAE Systems*
Walter Wohlmuth, *TriQuint Semiconductor*

SESSION M

Wednesday, October 24, 2001 – 10:30 a.m.

Low Noise FET Technology

Chairpersons: Jim Sowers, *Space Systems/Loral*
Pierre Mandeville, *Nortel Networks*

PANEL SESSION 4

Wednesday, October 24, 2001 – 1:00 p.m.

OEICs: Reality or Laboratory Curiosity?

Organizers/Moderators: Allan Armstrong, *Vitesse*
Walter Wohlmouth, *TriQuint*

The field of optoelectronic integrated circuits has been maturing at an accelerated rate due to the insatiable demand for bandwidth in both metropolitan and long-haul fiber optic networks. Many different methods of integration have evolved due to this enormous demand. Conventional III-V OEIC technology will be compared against potentially disruptive technology with unusual twists on optical to electrical integration.

The panel will address the following questions: To what extent and degree will the integration be in a monolithic as opposed to a hybrid form? What are the different demands and requirements for OEICs in long-haul and metropolitan networks? Are OEICs the natural strength of III-V material systems and ICs or will silicon, lithium niobate, polymers, or other materials systems become prevalent?

Panel Members:

Ronald T. Logan Jr.	*Phasebridge, Inc.*
Yves Baeyens	*Lucent Technologies / Bell Laboratories*
Abhay M. Joshi	*Discovery Semiconductor*
Mark Itzler	*JDS Uniphase*
Rick Thomson	*Teraconnect*
Ron Reedy	*Peregrine Semiconductor*

PANEL SESSION 5

Wednesday, October 24, 2001 – 1:00 p.m.

High Voltage, High Power PA's

Organizers/Moderators: Jan-Erik Mueller, *Infineon*
Chris Bozada, *Air Force Research Lab*

This panel discusses the status and prospects of various semiconductor technologies for high voltage, high power microwave applications. Typical system insertions are power amplifiers for base stations, radar and satellite telecommunications. The panelists are asked to present:

- Technology Advantages
- Figures of merit like breakdown voltage, output power, power density, PAE, gain versus frequency, linearity, etc.
- Technology status including integration capability, wafer diameter, reliability status, etc.
- Commercial prospects, such as market share and cost per Watt.

Technologies to be discussed include HEMT, LDMOS, HBT, GaN, SiC, and Si Bipolar.

Panel Members:

Scott Behan	*Xemod*
Lyle Leverich	*GHz Technology*
Gregory C. DeSalvo	*Northrup-Grumman*
Tim Henderson	*TriQuint*
Naotaka Iwata	*NEC*
Toshi Kikkawa	*Fujitsu*
Ray Pengelly	*Cree*

SESSION N

Wednesday, October 24, 2001 – 3:00 p.m.

Enabling Technologies For 40GB/s Optical Communications

Chairpersons: Benjamin Tang, *Primarion*
Marko Sokolich, *HRL Laboratories*

SESSION O

Wednesday, October 24, 2001 – 3:00 p.m.

Late News Papers

Chairpersons: **TBD**

SESSION A

Monday, October 22, 2001 – 8:30 a.m.

PLENARY SESSION

Chairpersons: Chris Bozada, *US Air Force*
Brad Nelson, *Stanford Microdevices*

A.1 **Prospects of CMOS Technology for High-Speed Optical Communication Circuits**
(Invited Paper), Behzad Razavi, *University of California, Los Angeles, CA*

A.2 **Advances in InP HEMT Technology for High Frequency Applications**
(Invited Paper), P.M. Smith, K. Nichols, W. Kong, L. MtPleasant, D. Pritchard, R. Lender, J. Fisher, R. Actis, D. Dugas, D. Meharry, A.W. Swanson, *BAE Systems, NH*

A.3 **A Fully Integrated Transceiver for Bluetooth**
(Invited Paper), H. Darabi, S. Khorram, E. Chien, M. Pan, S. Wu, S. Moloudi, J.C. Leete, J.J. Rael, M. Syed, R. Lee, P. Kilcoyne, B. Ibrahim, M. Rofougaran, A. Rofougaran, *Broadcom Corporation, CA*

A.4 **The Challenge of GaAs IC Manufacturing in Taiwan for Asian Pacific Wireless Market**
(Invited Paper), L.W. Yang, Liz Wu, RF Integrated Corporation, CA; P.C. Chao, *WIN Semiconductors Corp., Taiwan*

A.5 **Why You Should Be Interested in Technology Roadmaps for Compound Semiconductors**
(Invited Paper), Herbert S. Bennett, *National Institute of Standards and Technology, MD*

Prospects of CMOS Technology for High-Speed Optical Communication Circuits

Behzad Razavi
Electrical Engineering Department, University of California, Los Angeles, CA 90095
and Transpectrum Technologies, Los Angeles, CA 90024

Abstract

This paper explores the potential of CMOS technology for circuits operating at tens of gigahertz in an optical communications environment. An overview of modern CMOS processes is given and a generic optical system illustrating integration challenges is studied. The design of high-speed building blocks such as amplifiers, oscillators, and phase detectors is also described.

I. Introduction

The explosive demand for high data rates has revitalized optical communications, motivating intensive research on high-speed devices, circuits, and systems. The new optical revolution is reminiscent of the monumental change that the RF design paradigm began to experience in the early 1990s: modular, general-purpose building blocks are gradually replaced by end-to-end solutions that benefit from device/circuit/architecture codesign, and mainstream VLSI technologies such as BiCMOS and CMOS continue to take over the territories thus far claimed by GaAs and InP devices.

This paper examines the potential of CMOS technology for high-speed optical communications. We begin with an overview of modern CMOS processes, justifying their use for high-speed design. Next, we study a generic optical system and describe the speed and noise issues in the integration of transceivers. We then present the design of important building blocks such as amplifiers, oscillators, and phase detectors in CMOS technology. As a framework, we use the OC-768 standard for the design targets in the paper.

II. Why CMOS?

A. General Attributes

Aggressive scaling and the competition to follow Moore's Law have improved the intrinsic speed of MOSFETs by more than three orders of magnitude in the past 30 years. The f_T of NMOS transistors in the 0.15-μm and 0.13-μm generations approaches 80 GHz and is likely to exceed 120 GHz for 0.1-μm devices. Also, more relevant benchmarks such as differential ring oscillators and frequency dividers exhibit maximum operating speeds of several tens of gigahertz in the 0.13-um generation.

Despite rapid scaling, the present MOS technologies may appear inadequate for systems operating in the range of 40 Gb/s. However, another important property of CMOS processes, namely, the availability of multitude of metal layers, can substantially boost the performance by providing high-quality *passive* devices. As noted throughout this paper, monolithic components such as inductors, transmission lines, MOS varactors, and linear capacitors prove essential to extending the capabilities of CMOS technology to 40 Gb/s. Fortunately, the extensive research carried out on passive devices in both RF IC design and millimeter-wave circuit design can be exploited in optical systems as well.

In addition to scaling the dimensions and providing many metal layers, CMOS technology exhibits two other attributes germane to circuit design for optical communications. First, the inevitable scaling of the supply voltage does reduce the overall power dissipation of the system even though it creates many difficulties in the design of the building blocks. For example, a 1-to-16 demultiplexer (DMUX) with low-voltage differential signaling (LVDS) outputs across 100-Ω differential loads typically draws a supply current of 16×5 mA $= 80$ mA, a significant fraction of the overall transceiver's current. Thus, if the supply voltage is decreased from 3 V to 1.5 V, the DMUX power dissipation drops considerably.

The second attribute relates to the cost. Owing to lower fabrication cost, higher yield, and greater density of MOS devices, CMOS implementations prove more economical than their BiCMOS or III-V counterparts. While the cost advantage may not be apparent for low-complexity circuits such as transimpedance amplifiers (TIAs) and limiters, it does rise as a distinguishing factor when a full transceiver must be integrated on a single chip. In systems where many channels are carried on different wavelengths or on a bundle of fibers, multiple transceivers must be realized monolithically, further underlining the potential of CMOS technology. Moreover, the shift of paradigm towards integrating transceivers and framers on the same chip may select CMOS technology as the only viable solution. This trend is similar to the increasing sophistication that has appeared in RF CMOS transceivers.

B. Passive Devices

The extensive work on inductors, varactors, and oscillators inherited from RF CMOS design proves invaluable in high-speed applications as well. Since spiral inductors occupy a large area, stacked structures connected in series can be used [Fig. 1(a)]. Also, the bottom spiral can be moved away from the top one to reduce the parasitic capacitance significantly

0-7803-6663-8/01/$10.00©2001 IEEE

[Fig. 1(b)] [1]. Addition of a grounded n-well shield under the inductors suppresses cross-talk, an important feature in integrating various broadband circuits on the same substrate.

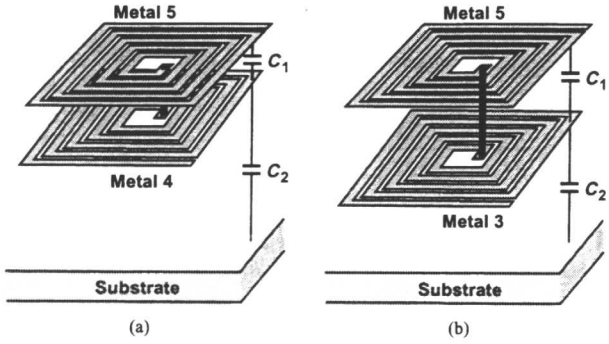

Fig. 1. (a) Stacked inductors, (b) modification to lower the total capacitance.

At speeds of tens of gigahertz, the use of on-chip transmission lines becomes an attractive technique. Shown in Fig. 2 are two topologies suited to integration in CMOS processes. The coplanar structure in Fig. 2(a) provides a relatively small capacitance per unit length but it suffers from resistive loss in the substrate. The microstrip line depicted in Fig. 2(b) exhibits a slightly greater capacitance but terminates the electric field lines on metal 1, thereby lowering the loss. These structures have been successfully used in CMOS circuits operating at tens of gigahertz.

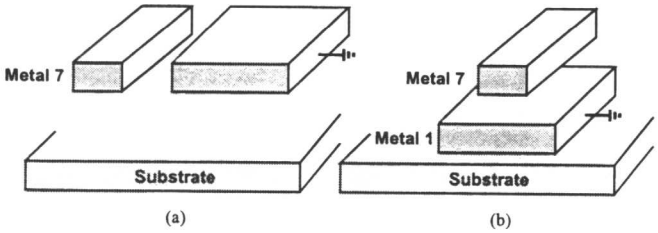

Fig. 2. (a) Coplanar transmission line, (b) microstrip line.

MOS varactors (Fig. 3) directly benefit from the scaling of the channel length as their quality factor is determined by the n-well resistance between the source and drain terminals. Offering a wider range and accommodating both positive and negative voltages, MOS varactors provide much more flexibility in design than pn junctions do.

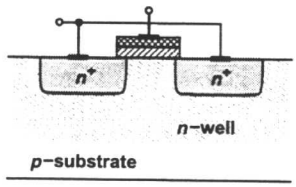

Fig. 3. MOS varactor.

At low supply voltages, capacitive coupling between cascaded stages may relax the voltage headroom constraints. However, both the bottom-plate parasitic capacitance and the low density of typical "native" capacitor structures make their use difficult. A practical solution is the "fringe" capacitor shown in Fig. 4, whereby the large fringe capacitance between adjacent metal lines is heavily exploited. With six or seven metal layers, a bottom-plate parasitic of only a few percent and a density of about 0.5 fF/μm can be achieved.

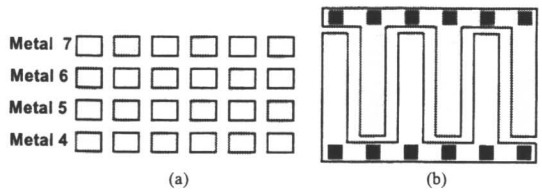

Fig. 4. Fringe capacitor, (a) cross section, (b) top view.

III. System Overview

Figure 5 shows a typical optical system. In the transmitter (TX), a number of channels are multiplexed into a high-speed

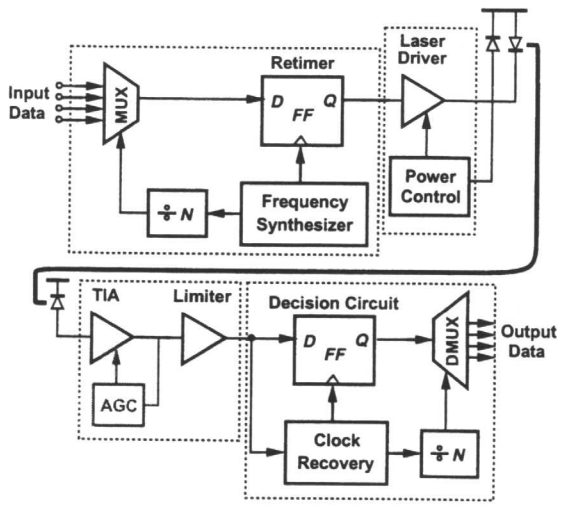

Fig. 5. Optical transceiver system.

data stream, the result is retimed and applied to a laser driver, and the optical output thus produced is delivered to the fiber. A frequency synthesizer generates clocks for both the multiplexer (MUX) and the retiming flipflop (FF). Also, since the laser output power varies with temperature and aging, a monitor photodiode (PD) and a power control circuit continuously adjust the output level of the driver.

In the receiver (RX), a photodiode converts the optical signal to a current and a transimpedance amplifier and a limiter raise the signal swing to logical levels. [The TIA may incorporate automatic gain control (AGC) to accommodate a wide range of input currents.] Subsequently, a clock recovery circuit extracts the clock from the data with proper edge alignment and retimes the data by a "decision circuit." The result is then demultiplexed, thereby producing the original channels.

The transmitter of Fig. 5 entails several issues that manifest themselves at high speeds and/or in scaled IC technologies. Since the jitter of the transmitted data is determined by primarily that of the synthesizer, a robust, low-noise phase-locked loop (PLL) with high supply and substrate rejection becomes

essential. Furthermore, the design of skew-free, synchronous multiplexers proves difficult at high data rates.

Another critical challenge arises from the laser driver, a circuit that must deliver tens of milliamperes of current with very short rise and fall times. Since laser diodes may experience large voltage swings between on and off states, the driver design becomes more difficult as scaled technologies impose lower supply voltages. The package parasitics also severely limit the speed with which such high currents can be switched to the laser.

The receiver of Fig. 5 also presents many problems. The noise, gain, and bandwidth of the TIA and the limiter directly impact the sensitivity and speed of the overall system, raising additional issues as the supply voltage scales down. Moreover, the clock and data recovery functions must provide a high speed, tolerate long runs (sequences of identical bits), and satisfy stringent jitter and bandwidth requirements.

Full integration of the transceiver shown in Fig. 5 on a single chip raises a number of concerns. The high-speed digital signals in the MUX and DMUX may corrupt the receiver input or the oscillators used in the synthesizer and the CDR circuit. The high slew rates produced by the laser driver may lead to similar corruptions and also desensitize the TIA. Finally, since the VCOs in the transmit synthesizer and the receive CDR circuit operate at slightly different frequencies (with the difference given by the mismatch between the crystal frequencies in two communicating transceivers), they may pull each other, generating substantial jitter.

The above issues have resulted in multichip solutions that integrate the noisy and sensitive functions on different substrates. The dashed boxes in Fig. 5 indicate a typical partitioning, suggesting the following single-chip blocks: the synthesizer/MUX circuit (also called the "serializer"), the laser driver along with its power control circuitry, the TIA/limiter combination, and the CDR/MUX circuit (also called the "deserializer"). Recent work has integrated the serializer and deserializer (producing a "serdes") but the TX and RX amplifiers remain in isolation.

IV. Building Blocks

A. Broadband Amplification

An attractive solution for low-voltage broadband amplifiers is inductive peaking. Owing to the extensive work on monolithic inductors in RF design, this method can now be realized with accurate modeling and prediction of the performance in optical communication circuits as well. Interestingly, inductor quality factors (Q's) as low as 3 to 4 prove adequate for increasing the bandwidth, allowing the use of simple, compact spiral structures.

Figure 6(a) shows a differential stage incorporating inductive peaking. It can be shown that an ideal inductor increases the bandwidth by approximately 82% if a 7.5% overshoot in the step response is acceptable. With the finite Q and parasitic capacitance of the inductors included, the enhancement is around 50%, still quite a significant factor.

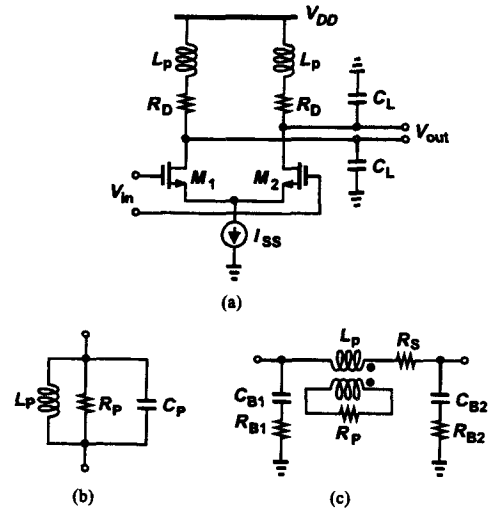

Fig. 6. (a) Inductive peaking, (b) simple inductor model, (c) more complete inductor model.

An interesting difficulty in modeling the inductors in the above circuit arises from the narrowband nature of the definition of the Q, an issue rarely encountered in RF design. Figure 6(b) depicts a rough model where $R_P/(L_P\omega)$ yields the correct Q at about 3/4 of the -3-dB bandwidth. The approximation is reasonable because the inductor manifests itself only near the high end of the band. Alternatively, a more complete model such as that in Fig. 6(c) can be used. Here, R_S denotes the effective series resistance, R_{B1} and R_{B2} represent the resistance seen by the electric coupling to the substrate, R_P models the resistance seen by the magnetic coupling to the substrate, and the capacitors approximate the parasitic capacitances. While the values of some of the components in this model do vary with frequency, the overall model can be fitted to measured data over a broader range than the parallel tank of Fig. 6(b) can.

Another technique suited to broadband signals is distributed amplification. Illustrated in Fig. 7 in differential form, such an amplifier distributes the transistor capacitances along a transmission line, thereby allowing a greater gain as more sections are added and hence relaxing the trade-off between gain and bandwidth. Since transmission lines in CMOS technology exhibit a moderate loss, a relatively high gain can be achieved. In fact, with a large number of sections drawing currents from the termination resistors, the overall gain may be limited by

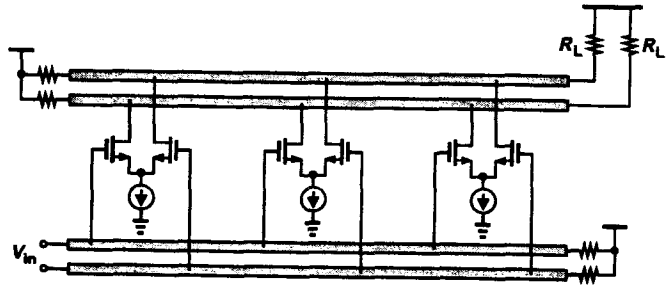

Fig. 7. Differential distributed amplifier.

the voltage headroom rather than the line loss. Examples of CMOS distributed amplifiers are reported in [2, 3].

B. Oscillators and Frequency Dividers

The transmitter of Fig. 5 requires that the last retiming flipflop be driven by a full-rate clock, e.g., 40 GHz for OC-768. Note that if the flipflop is omitted or the 40-GHz clock is derived by doubling the frequency of a 20-GHz signal, then mismatches yield considerable jitter in the transmitted data. For such speeds, an LC oscillator may be used (Fig. 8). Monolithic

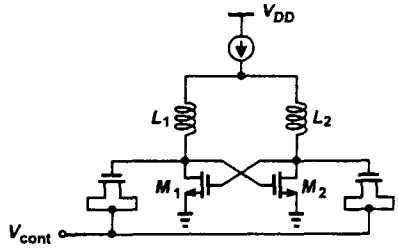

Fig. 8. LC VCO using MOS varactors.

inductors and varactors provide sufficiently high Q's at 40 GHz to afford low-noise oscillation. Alternatively, placing the distributed amplifier of Fig. 7 in a negative-feedback loop leads to an oscillator [2].

The frequency dividers employed in the transmit PLL must operate at high speeds while driving the large capacitance of the chain of multiplexers. For example, the divider following the VCO must typically drive nine differential pairs while sensing a 40-GHz clock. A candidate for division at high speeds is an injection-locked oscillator running at half the input frequency (Fig. 9). Addition of tuning can widen the frequency range of

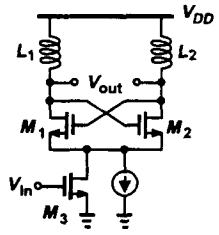

Fig. 9. Injection-locked frequency divider.

injection, allowing for process and temperature variations.

C. Half-Rate Phase Detectors

If the data rate is higher than the maximum tolerable speed of phase detectors and VCOs, a half-rate CDR architecture can be used. The idea is to run the VCO at a frequency equal to half of the data rate, thereby relaxing the design of the circuits in the signal path. Half-rate architectures usually demultiplex the data as well.

The principal challenge in half-rate CDR circuits relates to the design of phase and frequency detectors that operate properly while sensing full-rate data and a half-rate clock. Figure 10 depicts an example of a linear half-rate PD [4]. The circuit employs four D latches and two XOR gates. Since latches L_1 and L_2 sample D_{in} on rising and falling edges

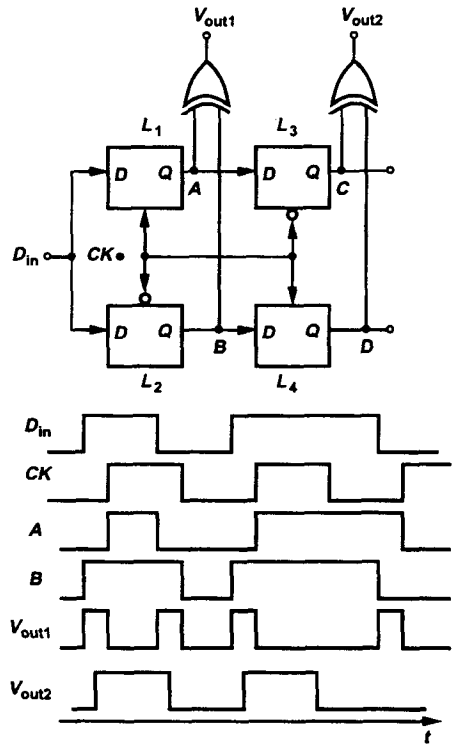

Fig. 10. Half-rate linear PD.

of CK, $A \oplus B$ produces a pulse each time a data transition occurs between a rising edge and a falling edge of the half-rate clock. The waveforms at C and D are identical except for a phase difference equal to half of the clock period. Thus, $C \oplus D$ produces a constant-width pulse on every data transition, serving as a reference. Note that the waveforms at C and D are the retimed, demultiplexed versions of the input stream. Thus, no explicit retiming of data is required.

Other examples of half-rate phase and frequency detectors are described in [5, 6].

REFERENCES

[1] A. Zolfaghari, A. Y. Chan, and B. Razavi, "Stacked Inductors and Transformers in CMOS Technology," *IEEE Journal of Solid-State Circuits*, vol. 36, pp. 620-628, April 2001.

[2] B. Kleveland et al, "Monolithic CMOS Distributed Amplifier and Oscillator," *ISSCC Dig. of Tech. Papers*, pp. 70-71, Feb. 1999.

[3] B. Ballweber, R. Gupta, D. Allstot, "Fully-Integrated CMOS RF Amplifiers," *ISSCC Dig. of Tech. Papers*, pp. 72-73, Feb. 1999.

[4] J. Savoj and B. Razavi, "A 10-Gb/s CMOS Clock and Data Recovery Circuit with a Half-Rate Linear Phase Detector," *IEEE Journal of Solid-State Circuits*, vol. 36, pp. 761-768, May 2001.

[5] M. Wurzer et al, "A 40-Gb/s Integrated Clock and Data Recovery Circuit in a 50-GHz f_T Silicon Bipolar Technology," *IEEE Journal of Solid-State Circuits*, vol. 34, pp. 1320-1324, Sept. 1999.

[6] J. Savoj and B. Razavi, "A 10-Gb/s CMOS Clock and Data Recovery Circuit with Frequency Detection," *ISSCC Dig. of Tech. Papers*, pp. 78-79, Feb. 2001.

Advances in InP HEMT Technology for High Frequency Applications

P.M. Smith, K. Nichols, W. Kong, L. MtPleasant, D. Pritchard,
R. Lender, J. Fisher, R. Actis, D. Dugas, D. Meharry and A.W. Swanson

BAE SYSTEMS, Nashua, NH 03060

Abstract

This paper presents an overview of the rapid progress being made in the development of InP HEMT devices and circuits for high frequency analog applications. Although widespread use of InP HEMTs has to date been limited by their comparatively high cost, commercialization now appears to be inevitable due to recent progress on two parallel fronts--the development of metamorphic HEMTs (MHEMTs) and the scaling of InP substrates to larger sizes (4- and 6-inch).

I. Introduction

The superior frequency response of InP HEMTs is well established--there have been several reports of devices with f_t in the 300-400 GHz range [1]-[6] as well as two reports of 600 GHz f_{max} [7],[8]. The f_t values are the highest of any technology, and the f_{max} is exceeded only by that of transferred-substrate InP HBTs [9].

Additionally, InP HEMTs have demonstrated the lowest noise figures of any transistor technology in the 2-200 GHz frequency range [10]-[12] and the highest power-added efficiencies (PAE's) at millimeter-wave frequencies [7],[13]. Other attributes include their unequalled high-frequency gain response, suitability for ultra-wide bandwidth amplifiers (1-180 GHz has been demonstrated [14]), and ability to amplify with extremely low DC power consumption.

Applications for which the InP HEMT is best suited include lightwave communication ICs, ultra-sensitive low noise receivers, high-efficiency transmitters and amplifiers requiring low DC power consumption, ultra-wide bandwidth or operation beyond 100 GHz. Moreover, the impending availability of InP HEMT/MHEMT chips produced *at costs comparable to GaAs PHEMT* will enable much wider commercialization of this technology.

The performance of the InP HEMT results from the physical properties of the InAlAs/InGaAs material system, where the high indium content InGaAs channel (typically 53-80% on InP substrates) possesses enhanced electron mobility and velocity, and the increased conduction band discontinuity at the heterojunction supports high two-dimensional electron gas (2DEG) densities, resulting in high current and transconductance.

The first microwave HEMTs were based on the AlGaAs/GaAs heterojunction. In 1986, a GaAs-based PHEMT with a pseudomorphic $In_{0.15}Ga_{0.85}As$ channel delivered improved high frequency performance [15]. Also in 1986, Aksun et al. reported an InP HEMT--with an $In_{0.53}Ga_{0.47}As$ channel grown lattice-matched on an InP substrate--that demonstrated 50% higher f_t and f_{max} than a GaAs-based PHEMT of similar geometry [16]. Pseudomorphic InP HEMTs with $In_xGa_{1-x}As$ channels, where indium mole fraction has been increased to as high as 80%, have also been exploited to further improve performance [1], but at the expense of unacceptably low breakdown voltages, and so InP PHEMTs have in practice either been limited to approximately 65% indium content or the breakdown issue has been addressed in other ways (see, for example, [17]).

Pseudomorphic InGaAs channels are *strained* layers in which the strain due to lattice mismatch between the InGaAs and adjacent layers is accommodated elastically, provided the InGaAs layer is kept below a critical thickness. The metamorphic HEMT, or MHEMT, allows high-indium InGaAs channels to be realized on GaAs substrates (see, for example, [18]). The active layers are grown on a relatively thick (1-2 μm) compositionally graded buffer that shifts the lattice constant (providing *strain relaxation*) by creating dislocations and then traps them to prevent their propagation into the device active

Property	InP HEMT	MHEMT
Substrate Availability, Cost	- 4-inch now, higher cost	+ 6-inch available now
MBE Growth Time	+ ~1/2 hour	- 1-2 hours
Processing Difficulty/ Yield	- Higher breakage, more difficult/ slower backside process	+ Lower breakage, standard GaAs backside process
Performance, Impedance Char.	No difference	No difference
Achievable Channel Indium Content	53-80%	+ 30-80%
Thermal Resistance	+ Lowest--InP has 50% higher thermal cond. than GaAs	Comparable to GaAs PHEMT, effect of buffer unclear
Reliability	Proven for low noise, unproven for power	Excellent initial data for low noise, power unknown

Table 1. Comparison of InP HEMT and MHEMT technologies. Advantages are indicated by a +, while weaknesses are denoted by a -.

0-7803-6663-8/01/$10.00©2001 IEEE