MICROCIRCUIT ENGINEERING 91

Edited by

A. Tucciarone, A. Paoletti and P. Paroli

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Preface

Microcircuit Engineering 91 was held in Rome, Italy, on 17–19 September 1991, organised by Università di Roma – Tor Vergata and Consiglio Nazionale delle Ricerche, under the auspices of Comune di Roma, Assessorato alla Cultura, with the support of Telettra SpA and Texas Instruments Italia. During the conference, 10 invited and 118 contributed papers were presented (52 as posters). This volume contains the full texts of 8 invited and 107 contributed papers.

The papers presented at the conference were mainly from the following countries: Germany (36), USA (29), Japan (14), UK (13), Italy (11), USSR (10), France (9), Belgium (7) and the Netherlands (6). Former Eastern European countries contributed with 18 papers: a larger participation may be anticipated in the future.

All papers were refereed by members of the Programme Committee. The main reasons for rejection of manuscripts were: (i) insufficient technical content and (ii) language, in that order. In cases of serious objections or rejections, three referees were involved and authors were urged to carry out improvements up to seven weeks after the conference. Because of the wider geographical participation, for the first time propriety in the use of the English language was an issue. It was decided that, at this conference, only questionable clarity of technical content could constitute sufficient ground for rejection, a rule which was shared by the publisher. However, there was a strong view in the Programme Committee that, in the future, it should be made clear that language is to be considered an essential tool in scientific communication. Perhaps, Programme Committees could explicitly address this delicate issue from the start, in the Call for Papers.

The conference was the seventeenth in the series and was attended by over 300 registered participants coming mainly from Germany (76), Italy (58), USA (39), UK (34), Japan (20), France (18), the Netherlands (10), Belgium (9), Switzerland and the USSR (8).

Preparation of these conference proceedings was only possible with the help of colleagues of the Mechanical Engineering Department: Giuseppe Balestrino, Marco Marinelli and Enrico Milani. The Editors would like to thank them sincerely.

Rome, 12 November 1991
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A. Paoletti
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ELECTRON BEAM LITHOGRAPHY

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Progress in EB-Cell Projection Lithography

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Abstract
The throughput and accuracy of electron beam cell projection lithography are discussed. The method drastically reduces the number of e-beam exposure shots utilizing a specially shaped beam. A system designed to produce 64 and 256M-DRAMs is introduced. A 0.2 μm exposed pattern is also shown.

1. INTRODUCTION

There is no doubt on the resolution of e-beam lithography[1]. The problem is that the throughput and accuracy do not easily stand together. Many ways for high-throughput have been proposed, however they were not applied to the practical device production because of the lack of accuracy. This paper proposes an e-beam cell projection lithography system[2-4] of which writing method resemble to the usual variable shaped method. In this method, the accuracy is equivalent to the conventional one but the throughput is drastically improved.

2. THROUGHPUT AND ACCURACY

Total wafer writing time T in e-beam lithography is the sum of the beam exposure time T_e and the overhead time T_{oh}.

$$T=T_e+T_{oh} \qquad (1)$$

The main part of T is the beam exposure time T_e in DRAMs larger than 64Mbits. The T_{oh} includes the time for mark detection, stage movement, etc. and can be reduced to less than 100 sec per wafer. In this section, the relationship between throughput and accuracy is discussed.

2.1. Exposure unit and throughput

Figure 1(a) shows a wafer exposed with shot as an exposure unit. The T_e is the product of the number of shots "n" per wafer and the unit time "t_u" per shot as expressed by equation 2. Here, n depends on the size of the shot. When a 6" wafer is covered with 5 μm square shot, n becomes $3x10^8$ at 50% coverage. The unit time "t_u" is the sum of the resist exposure time and electrical settling time t_s as expressed by equation 3.

$$T_e = n \times t_u \quad (2)$$
$$t_u = S/J + t_s \quad (3)$$

where S is the resist sensitivity and J is the current density. The exposure time map made on the n-t_u plane can give us an e-beam system design target as shown in Figure 1(b). Here, the profitable region for memory production is considered under a t_u of 100 nS. In the variable shaped beam method, the shot number for a 64M-DRAM becomes 2×10^{10}. To be profitable, the t_u must be smaller than 5 nS, which is not realistic even if state of the art techniques are used. If we make a 5 μm shot, which includes several cells, the shot number can be decreased to 3×10^8. In this case a t_u of 200 nsec would be profitable and realistic. This is the idea of cell projection lithography[2-4].

2.2. Exposure unit and accuracy

The shot size limitations are discussed in this section. The first limitation comes from the gun. The current density J is limitted by the below next two equations,

$$J \leqq B\pi(\varepsilon/\sqrt{2}l)^2 \quad (4)$$
$$J \leqq B\pi\alpha^2 \quad (5)$$

where B is the brightness, ε the emittance of the gun, l the side length of the shot and α the beam semi-angle on the wafer. This relationship is shown in Figure 2. The shot size is inversely proportional to J. The second limitation comes from the objective lens. The square shape is distorted by the beam deflection. For a 256M-DRAM, the distortion should be less than 0.01 μm. An example of square distortion is seen in a typical deflection system[5]. If we limit the deflection distance to within 5 mm, a 5 μm square shot is the applicable maximum as shown in Figure 3.

3. CELL PROJECTION LITHOGRAPHY SYSTEM

3.1. Exposure experiment

Exposure experiments were conducted to verify the above idea. Figure 4(a) shows a cell aperture made of Si wafer using LSI process techniques. The aperture size is 40μm x 45μm and the image is reduced to 1/25. Figure 4(b) shows the exposed resist pattern under 30 kV. The minimum line width is 0.2 μm on the wafer. This pattern corresponds to the FG layer of a 256M-DRAM.

3.2. Specifications of the newly designed system

A system is under development for 64 and 256M-DRAMs. The specifications are shown in Table 1. To achieve a 200 nS t_u, both the e-beam system, as well as, a new process have to be developed. Assuming a 1 μC/cm² resist, the electron optical column and control electronics have been optimized. This t_u corresponds to 10A/cm² current density and a 100 nS settling time. Table 2 lists the optical constants[5]. To reduce the overhead time, the write-on-the-fly method has been chosen, where the stage moves at variable speeds.