THE DESIGN AND ANALYSIS OF VLSI CIRCUITS

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PREFACE

In 1959 Robert Noyce and Jack Kelby changed the technological and economic profile of the world when the independently invented the planar integrated circuit. Since 1961 the number of transistors that can be successfully fabricated on a single chip has doubled almost every year. This has caused a revolutionary and exponential decrease in the cost per unit function for digital electronics. Enticed by the multibillion-dollar market that opened as a result of this technological explosion, the engineering community has developed volumes of specialized knowledge, techniques, and theories to harness the power quiescent in a few milligrams of silicon. In *The Design and Analysis of VLSI Circuits* we will examine one of the fields essential to this technology—integrated circuit design.

The purpose of this text is to bring the reader to the next level of sophistication beyond that offered by introductory VLSI design books. For instance, *The Design and Analysis of VLSI Circuits* is both more advanced and more specialized than the classic work by Mead and Conway, *Introduction to VLSI Systems.* At the Massachusetts Institute of Technology, one of the courses that uses this material has as its prerequisite either an introductory VLSI course in the style of Mead and Conway or a circuit design-oriented course in the style of the book by Hodges and Jackson, *Analysis and Design of Digital Integrated Circuits.* We have made an effort, however, to include the necessary materials to allow this book to be used as a first course in VLSI circuits in cases where the constraints of the curriculum and the student's background warrant it. This text has been successfully used in introductory VLSI courses.

We assume that the reader is familiar with elementary circuits, device physics, and logic design. The text is appropriate for a senior- or graduate-level course on the design of MOS circuits; it will also be useful to the engineer or scientist wishing to become a knowldgeable practitioner in the field of integrated-circuit design. This book was used extensively at Digital Equipment Corporation in the initial training and continuing education of circuit designers, systems designers, technology experts, and CAD professionals.

The book begins with a heuristic treatment of a number of nMOS and CMOS circuit design methodologies that provides a broad base from which the reader can understand what a methodology is, and what is involved in its use or design. Discussions of static and dynamic circuit techniques and the role of regular structures are included. Because we are dealing with circuit techniques, it is possible to understand, qualitatively, how fairly complex circuits are constructed. This is the approach of Chapter 1, in which the context and motivation for the rest of the book are developed. Of the seven remaining chapters, Chapters 2 through 5 emphasize traditional "electrical engineering" issues, while Chapters 6 through 8 are oriented more toward "computer science." While we feel that all of this material is the legitimate domain of the VLSI circuit designer, readers with a computer science background might profit from first reading Chapters 1, 6, 7, and 8, then backtracking to the material in Chapters 2 through 5.

While qualitative discussions are fine for understanding elementary circuit techniques, they are unfortunately insufficient to enable one to actually do quality circuit design. Therefore the emphasis of later chapters shifts to a more quantitative perspective. In Chapter 2 the physics of MOS devices and interconnect is developed. Engineering is largely concerned with models and their appropriate use. In this chapter we develop a number of models of varying levels of complexity and accuracy. Some are useful for "back of the envelope" calculations, while others are useful only when incorporated into sophisticated circuit simulation programs. In fact, starting with Chapter 1, computer-aided design plays an integral part in our approach to VLSI circuits. A computer, however, is no substitute for insight, so we also work to develop a feel for how the various first- and second-order physical phenomena in MOS devices influence the terminal characteristics of capacitors, transistors, and interconnect. The limits of validity of the models are examined. These, and other points in the book, are emphasized in numerous problems and examples. Starting in Chapter 2, we identify numbered equations that are of central importance with a star.

Chapter 3 contains the aspects of fabrication technology that we feel circuit designers must know. A suite of integrated circuit fabrication techniques are presented. We then show how these techniques are used

to build MOS circuits. A key section contains a discussion of design rules and their origins. The chapter also includes the development of elementary yield formulas.

Chapter 4 develops the concepts necessary for using the basically analog MOS transistor as a basis in constructing reliable digital systems that meet specifications. Among the concepts discussed are noise, noise margins, macromodeling, and worst-case design. The dynamics of logic gates are carefully investigated. We see examples of the interplay of device physics and circuit design. the inverter, as the archetypical logic element, is the main vehicle of the chapter. We examine two types of nMOS inverters and two types of CMOS inverters.

With these foundations, we present in Chapter 5 a host of specialized circuit techniques including the optimization of large fan-out and fan-in circuits, clock drivers, substrate-bias generation, input protection devices, level conversion, Schmitt triggers, and so forth. Along with our presentation of each circuit technique, we develop the conceptual and analytical tools necessary for studying them. After mastering this chapter, readers will know enough to place new circuit techniques, invented by themselves or someone else, in proper context.

Chapter 6 provides a discussion of clocking methodologies. These methodologies include nonoverlapping clocks, overlapping clocks, and self-timed techniques. The emphasis is on nonedge-triggered systems. Clock generators and issues of skew are addressed. Synchronization circuits are examined quantitatively.

Chapter 7 examines the circuit design of large arrays and regular structures, including decoders, RAM, ROM, and systolic arrays. We see how layout, circuit design, topology, and logic design interact in fascinating ways. The retiming and optimization of systolic arrays are examined. The study of these issues provides a smooth introduction to Chapter 8: "The Microarchitecture of VLSI Systems."

A few years ago microarchitecture would have had no place in a book on circuit design; however, the world has changed. A digital VLSI sicruit is a digital system. In Chapter 8 we concentrate on the points of synergy between microarchitecture and circuit design. The microprocessor is used as the archetypical VLSI logic chip. Techniques for data-path and control-path design are presented. For the data path we emphasize carry propagation as a critical issue. For the control path we emphasize microprogram context switches.

To get the most out of this book, it would be helpful to have access to a computer running SPICE2. To provide realism to the examples and problems and to illustrate points in the text, we have developed hypothetical 2 μm nMOS and CMOS processes that form a common theme. Catagories such as design rules, process specifications, and SPICE models for these processes are listed in the appendixes and are used in many examples. Because these processes are fully specified, it is

possible to do significant paper designs as part of a course or self-study program.

The problems at the end of each chapter are categorizd into three levels of difficulty: reasonable, hard, and extremely difficult. Hard problems are denoted by a "△" at the end of the problem statement. These problems either involve a lot of work, difficult concepts, or significant innovation. Extremely difficult problems are denoted by a "△△" at the end of the problem statement. These problems indicate lines of investigation worth pursuing. If these problems have answers, those answers often depend on information not covered in the book.

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CONTENTS

1 CIRCUIT FORMS AND METHODOLOGIES

The domain of the integrated circuit designer stretches from the realms of device physics and nonlinear circuit theory to the regime of digital system microarchitecture. Integrated circuit design plays a central role in VLSI technology and encompasses multiple levels of abstraction: electrostatics, topology, switching theory, and so forth. The VLSI circuit designer is challenged to transcend these disparate disciplines and transform an idea into the detailed specifications for a manufacturable machine.

Each abstraction has a hierarchy of detail. Systems must be decomposed into subsystems, subsystems into modules, and modules into components. With each decomposition the instantiation of the machine becomes more complete. There are many ways to navigate the two-dimensional hierarchy of abstraction and detail, but whatever course is chosen, its ultimate success depends on bottom-up understanding. For this reason we begin our study of VLSI design at the lower levels, with transistors and interconnect.

1.1 A qualitative model of the MOS transistor

In this chapter, our objective is to obtain a good qualitative feel for how a digital MOS circuit works. As part of this task we need to understand how some of the low-level components in a VLSI circuit behave and how

they are composed to form interesting functional modules. We discuss a number of different design methodologies, but they should be thought of as parts of a larger, unified whole. In later chapters, these and other circuit techniques will be investigated with more quantitative precision.

Figure 1.1 shows a photomicrograph of an LSI chip [Olsen 81]. The two-dimensional nature of the integrated circuit is clearly evident. Only two primitive elements—transistors and wire—are used to build today's magnificent variety of VLSI circuitry. Most of what we see in Fig. 1.1 is wire, with the transistors taking up only about 10% of the area. The chip contains 13,000 transistors (a small chip by modern standards). It is a few millimeters on a side and only a fraction of a millimeter thick, and all of the interesting structure exists within a few microns of the surface. Several large regular structures are evident. These represent most of the transistors, but only a fraction of the labor. We must take a closer look at the chip to see a single transistor.

A transistor occurs at the intersection of two wires. Figure 1.2 shows two close-up views of some circuitry viewed from the top, but again we have mostly wire; the transistors can be seen only if one knows where to look. We can see why it is often said that in VLSI the transistors

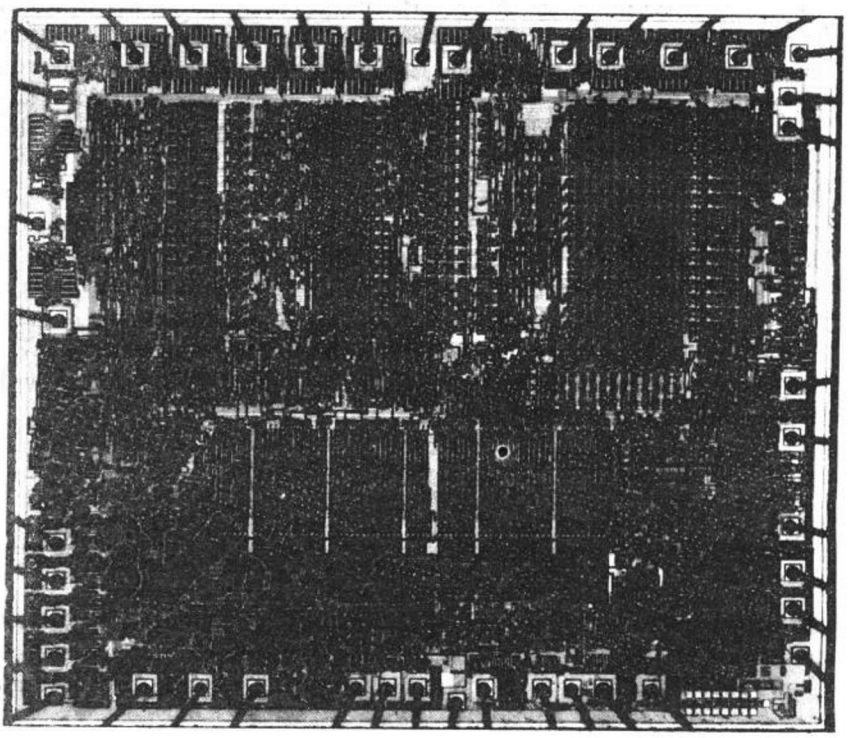


FIGURE 1.1 Photomicrograph of the T11 microprocessor. (Copyright ©Digital Equipment Corporation 1985. All rights reserved. Reprinted with permission.)

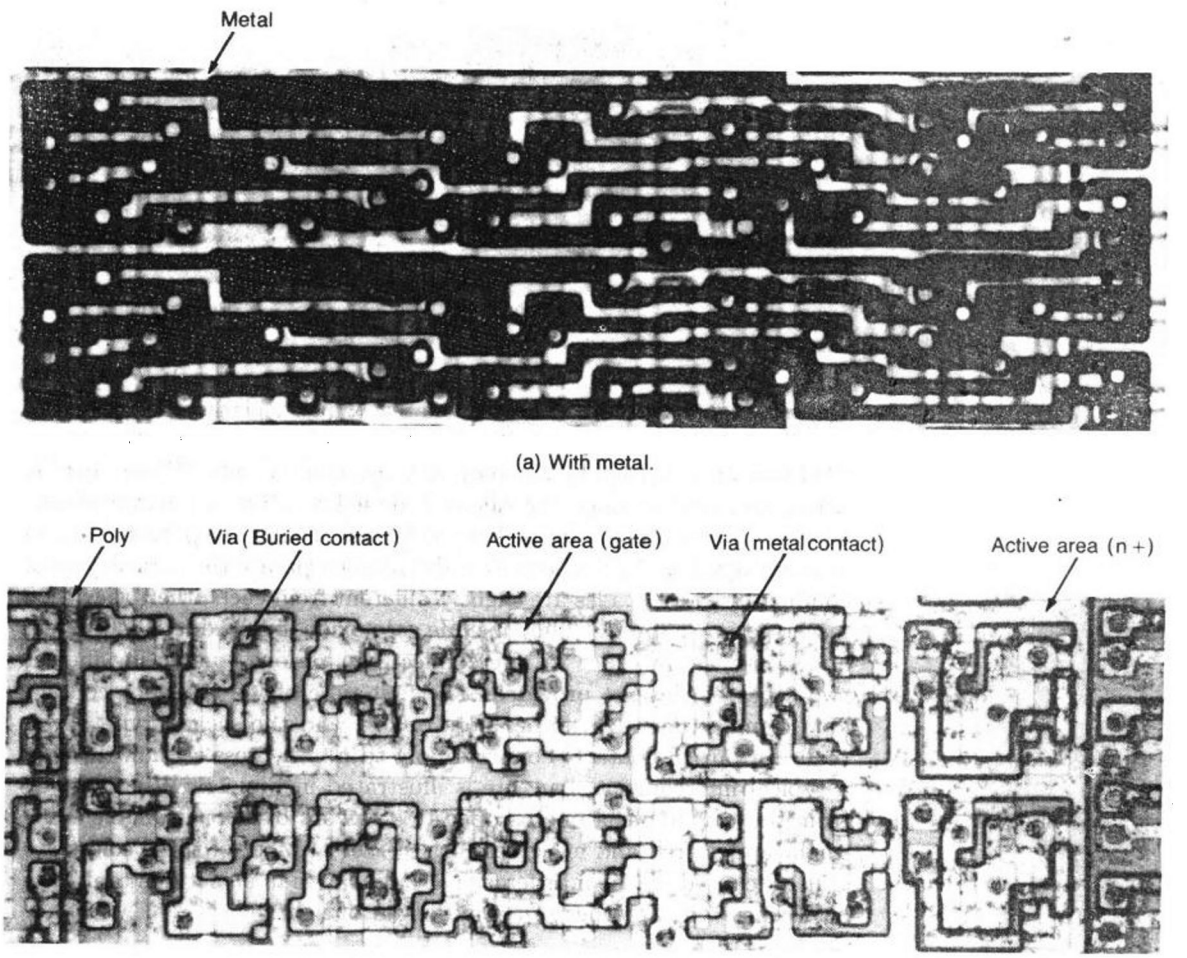


FIGURE 1.2 Close up photomicrographs of a single section of the T11: (a) with metal; (b) with metal removed. (Copyright ©Digital Equipment Corporation 1985. All rights reserved. Reprinted with permission.)

are free; it is the wire that is expensive. There are three layers of interconnect media on this particular chip. The speckled material is aluminum. The two other media are polycrystalline silicon and heavily doped, single-crystal silicon. These two materials have a very harmonious relationship with the transistors, as will be seen shortly.

Figure 1.3 shows the layout of the circuitry shown in Fig. 1.2. The various materials are labeled. The polycrystalline silicon (poly) and metal layers were deposited during the chip fabrication process. The metal acts only as wire while the poly plays the dual role of wire and

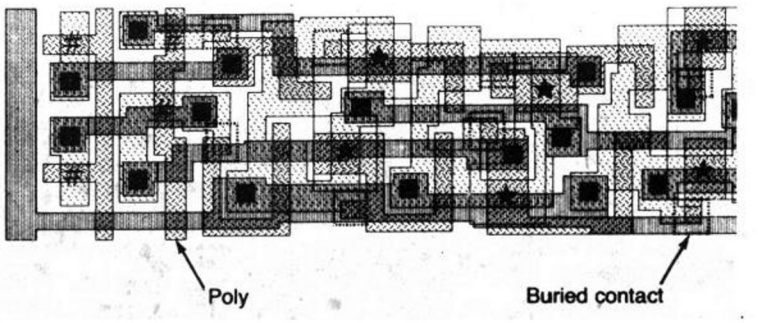
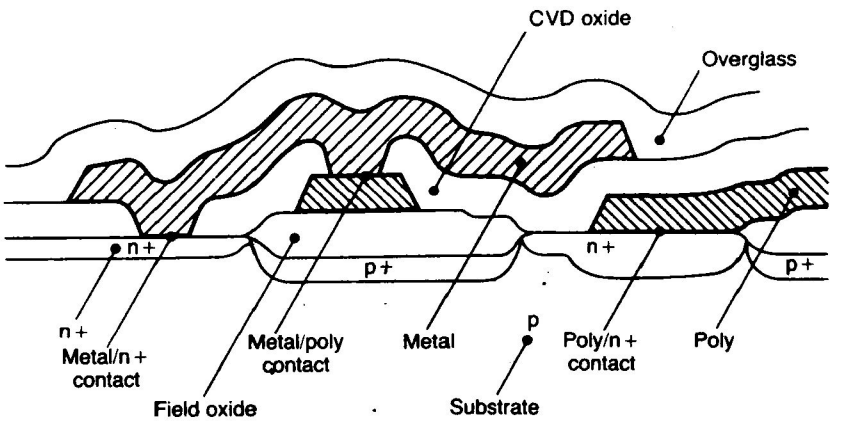
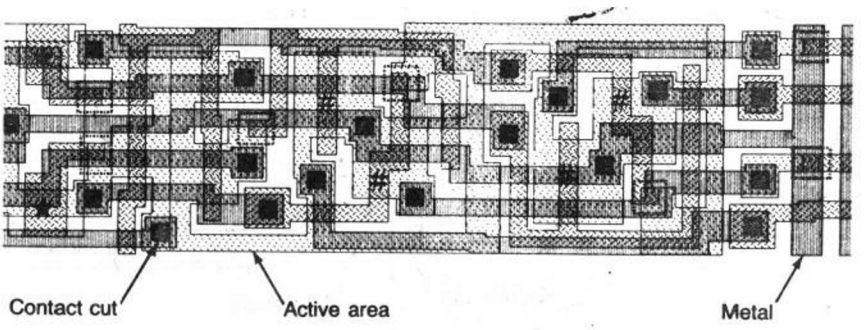


FIGURE 1.3 Layout (mask-specifications) of the portion of the T11 illustrated in Fig. 1.2.

transistor gate material. The active area, which includes the regions of heavily doped single-crystal silicon and transistor gate area, also plays a dual role. It is divided by the poly into two components. Where there is active area and no poly, the silicon is doped n+. The n+ material acts as wire. Transistors are formed at the intersection of the poly and active area regions. Layers of silicon dioxide (glass) separate the three layers of conductor. These oxides are slightly different from each other, as will be discussed in Chapter 3. They include gate oxide, field oxide, CVD oxide, and overglass. In order to interconnect the various conducting media, two types of vias are provided. The first type of via (called a contact cut) connects metal to either poly or n+, and the second type of via (called a buried contact) connects poly to n+. A cross section through a typical interconnect structure is illustrated in Fig. 1.4. When viewed from the top, under a microscope, a patchwork of color is visible. Poly might appear red and n+ green, or vice versa. Most of these colors are "false," caused by the interference of light waves in structures that have a thickness on the order of a wavelength of light.

FIGURE 1.4 Some contacts in nMOS technology.





The MOS[1] transistor is a four-terminal device. Under normal operating conditions the gate of the transistor controls the flow of charge carriers between the source[2] and the drain. The fourth terminal is the body that in pMOS and nMOS technologies cannot be used for performing useful logic. This is because in these technologies all of the body terminals are connected by a common substrate. Figure 1.5 illustrates the cross section of an nMOS transistor. The source and drain are composed of heavily doped n+ silicon. The gate is separated from the channel region by a thin layer of silicon dioxide only a few hundred atoms thick. The gate conductor is made of heavily doped, polycrystalline silicon. It is important to develop a clear mental picture of these geometries. Figure 1.6 shows three projections of an nMOS transistor. Illustrated in Fig. 1.7 are two nMOS devices in a common substrate. The sources and drains of these devices are isolated from each other by reverse-biased p–n junction diodes and the associated depletion regions. (A depletion region is a volume of semiconductor devoid of charge carriers.)

There are two types of nMOS transistors: normally on and normally off. In a normally off nMOS transistor there are no mobile charge carriers in the channel region under the gate when the input voltage is low. This type of transistor is called an enhancement-mode device because one must enhance the charge on the gate in order to achieve conduction between the source and the drain.

When a positive charge Q_G is placed on the gate of an nMOS transistor an amount of charge almost equal to $-Q_G$ is induced in the channel. This charge is composed of depleted acceptor ions and

[1] MOS stands for Metal Oxide Semiconductor and refers to the physical structure of the device. The term IGFET (Insulated Gate Field Effect Transistor) is also used. CMOS, pMOS and nMOS, refer to complementary, p-channel, and n-channel MOS, respectively. Despite the "M" in MOS, modern MOS devices do not really have metal gates but use a silicon gate in a similar role.

[2] The source is so called because it is the "source" of mobile charge carriers, which are electrons for n-channel devices and holes for p-channel devices.

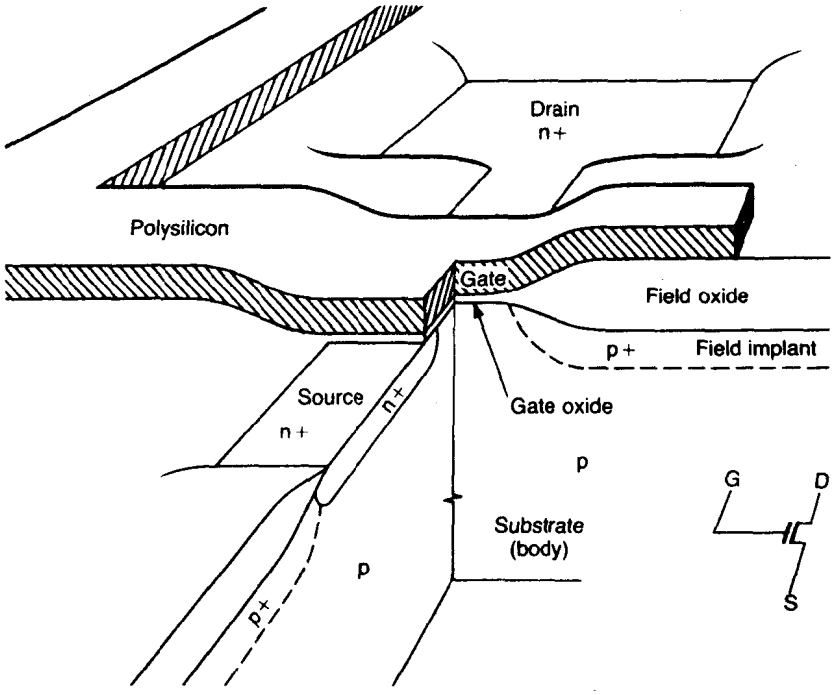
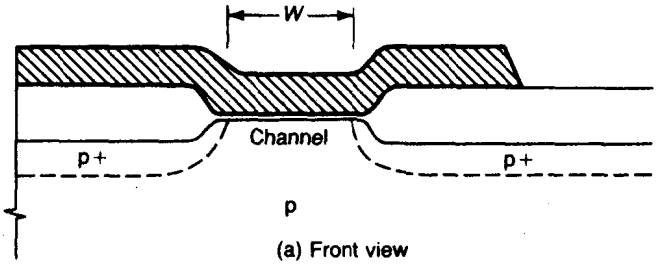


FIGURE 1.5 Cut-away view of an n-channel MOS transistor at the point in the processing after the source/drain implants.



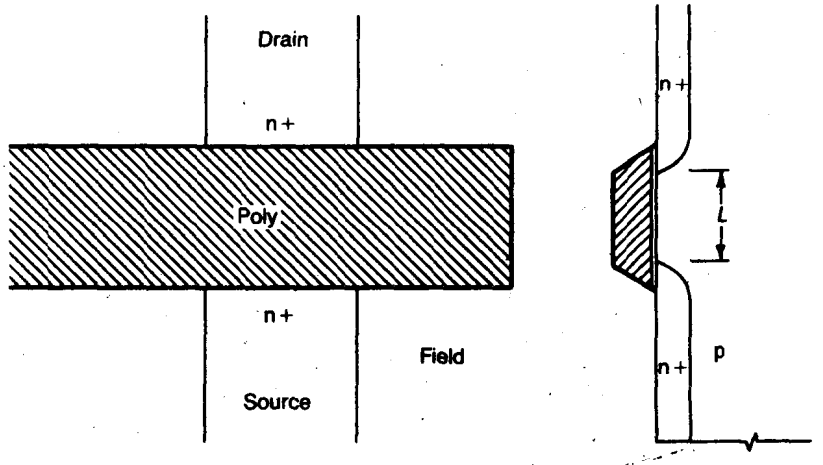


FIGURE 1.6 Three views of an n-channel MOS transistor: (a) front; (b) top; (c) side.

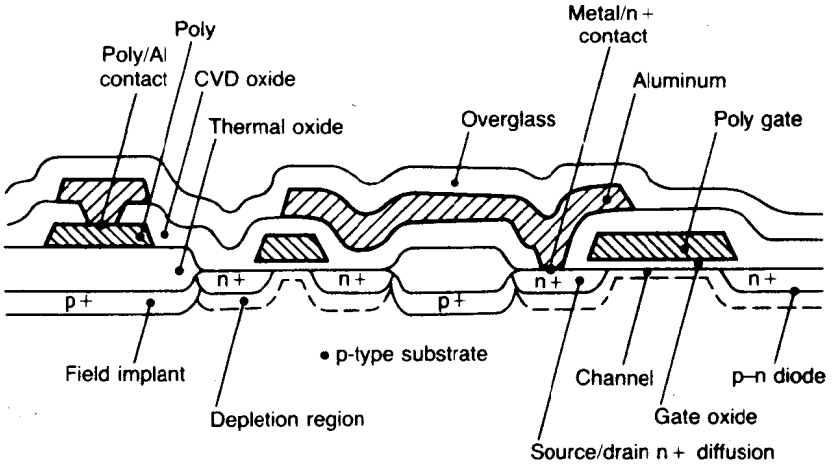


FIGURE 1.7 Two nMOS transistors in a p-type substrate. Isolation between transistors is provided by reverse biased p–n diodes.

free carriers, which flow in from the source and drain. Assume that the transistor has been designed such that when the gate is charged to the positive supply voltage V_{DD} the majority of channel charge is due to mobile charge carriers, that is, electrons. A positive drain-to-source voltage v_{DS} causes a stream of electrons to flow out of the source and be swept into the drain. The time it takes an electron to flow from the source to the drain is the transit time t_τ. It depends on the mobility μ of the charges in the channel, the strength of the electric field $\mathcal{E}$ (which is inducing the carriers to move), and the length of the channel L. One complete changeover or renewal of the channel charge occurs each transit time. The mobility relates the average velocity $\mathcal{V}$ of the carriers to the electric field. We have

$$\mathcal{V} = \mu\mathcal{E}. \tag{1.1}$$

The current i_{DS} is equal to Q_G/t_τ. Up to a point, the higher the drain-to-source voltage v_{DS}, the higher the drain current. The reason is that a higher drain-to-source voltage causes a larger electric field in the channel and hence faster carrier propagation. When the voltage on the gate v_{GS} is low (Q_G small) there is very little or no mobile charge mirrored in the channel. The gate voltage at which mobile charge is first induced in the channel is called the threshold voltage V_T. For gate-to-source voltages below V_T, the resistance between the source and drain is nearly infinite. For gate voltages above V_T, the resistance of a typical MOS transistor is on the order of 20 kΩ. The higher the gate voltage, the lower the effective resistance R because more mobile charges are induced in the channel, increasing its current-carrying efficacy. Thus, for a given drain-to-source voltage, higher gate voltages cause higher