GaAs IC SYMPOSIUM

IEEE GALLIUM ARSENIDE INTEGRATED CIRCUIT SYMPOSIUM
Co-Sponsored by The IEEE Electron Devices Society,
The IEEE Microwave Theory and Techniques Society, and
The IEEE Solid-State Circuits Society

22nd Annual

TECHNICAL DIGEST 2000

SEATTLE, WA

NOVEMBER 5-8, 2000

00CH37084

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GaAs IC Symposium - IEEE Gallium Arsenide Integrated Circuit Symposium

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Welcome to the 2000 IEEE GaAs IC Symposium

On behalf of the organizing committee and the IEEE EDS, MTT-S, and SSCS, I welcome you to the 22nd (2000) IEEE GaAs IC Symposium in the beautiful city of Seattle, Washington at the Westin Hotel.

Over the last 22 years, the IEEE GaAs IC Symposium has become the preeminent international forum on developments in integrated circuits using GaAs, InP, SiGe, GaN, SiC and other compound semiconductor devices. In 2000, the Symposium continues its tradition of presenting the best from around the world in high frequency microelectronics. This year's program continues to demonstrate the strong growth in commercial wireless and digital communications. Major focus areas of this year's GaAs IC Symposium, organized by John Sitch and the Technical Program Committee, include state-of-the-art circuits and technology for:

- Wireless and broadband communications
- Very high-speed digital communications
- Highly-efficient, linear, power amplifiers
- Interface electronics and signal processing
- Millimeter-wave systems

The technical sessions will highlight all aspects of technology: device development and fabrication, characterization and modeling, IC design and testing, high volume manufacturing, reliability, and system applications.

The 22nd IEEE GaAs IC Symposium continues our tradition of providing focused educational opportunities through our Short Course and Primer Course, both held on Sunday, November 5th. Tim Henderson has organized a very interesting and highly applicable one-day Short Course on "Linear Power Amplifiers" taught by five industry experts. In addition, Stephen Long and Donald Estreich will once again present our Primer Course on the "Basics of GaAs ICs" which is not only an excellent tutorial but is presented within the context of this year's symposium submissions.

You have the opportunity to learn of new products from the approximately 40 exhibitors in the GaAs IC Technology Exhibition and potential customers for the latest commercially available GaAs ICs can learn about these in the Vendor Product Forum.

To complement the full technical program, we have provided several social events to allow interactions with colleagues while catching up with the newest technology available on the market. These events include the Sunday evening Opening Reception, the Monday evening Technology Exhibition Reception, and the Tuesday evening Theme Party "A Northwest Experience" at Kiana Lodge, a six acre waterfront retreat on Puget Sound.

Finally, I want to announce the winner of our 3rd Outstanding Paper Award from the 1999 Symposium to C. R. Bolognesi, N. Matine, M. W. Dvorak, X G. Xu, S. P. Watkins from Simon Fraser University, Burnaby BC, Canada for their paper "InP/GaAsSb/InP DHBTs With High Ft and Fmax For Wireless Communication Applications." We are pleased you have chosen to join us in Seattle for the 22nd IEEE GaAs IC Symposium. We know that we have an outstanding technical and educational program to support our business.

Jim Komiak
Chairman
2000 IEEE GaAs IC Symposium

2000 IEEE GaAs IC Symposium Organizers

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1900 Fifth Avenue
Seattle, WA 98101-1281

SYMPOSIUM AT A GLANCE

SATURDAY, NOVEMBER 4, 2000	**Saturday**	
REGISTRATION (Short Course & Primer Course Only)	6:00 p.m.-8:00 p.m.	Cascade Foyer
SUNDAY, NOVEMBER 5, 2000	**Sunday**	
REGISTRATION (Short Course & Primer Course Only)	7:00 a.m.-8:00 a.m.	Cascade Foyer
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SHORT COURSE: "Linear Power Amplifiers for Voice and Data Communications"	8:00 a.m.-4:45 p.m.	Cascade 2
GaAs Reliability Workshop (Registration, Workshop, and Lunch)	8:00 a.m.-5:00 p.m.	TBD
Short Course Lunch	**12:20 a.m.-1:30 p.m.**	**Elliott Bay**
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PANEL SESSION 2: InP – Material for the New Economy	1:00 p.m.-2:30 p.m.	Grand 2
SESSION B: Advanced PA Technologies & Techniques	3:00 p.m.- 4:20 p.m	Grand 1
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Close of Symposium		

Visit us on the World-Wide Web at:
http://www.gaasic.org/

Coffee Breaks:

Primer Course and Short Course Registrants (only) –

Sunday, November 5th: Cascade Foyer

Symposium Registrants -

Monday, November 6th: Grand Foyer
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Chris Bozada, *US Air Force*

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PANEL SESSION 1

Monday, November 6, 2000 1:00 p.m. – 2:30 p.m.

E-MODE PHEMT'S ARE KILLING HBT'S

Organizers and Moderators:
Brad Nelson, Stanford Microdevices
Mitch Shifrin, Hittite Microwave

Handset power amplifiers have been dominated by GaAs HBT's in the past few years. Tomorrows 3G power amplifier suppliers are lining up to pitch their parts and E-mode PHEMT's have begun to take market share. This highly lucrative market has tremendous competition and excitement. When will PHEMT's squash the HBT's? The panelists will be encouraged to address the following issues and others of pertinence: linearity, DC switching / leakage, power control, integration capabilities, robustness to VSWR / over-voltage, low power output efficiency and the always illusive cost trades. Come listen and contribute to a hotly debated topic and find out where the money is going.

Panel Members:

Julio Costa	*Motorola*
Gene Tkachenko	*Alpha Industries*
Rob Christ	*TriQuint Semiconductor*
Dave Halchin	*RF Micro Devices*
TBD	*Anadigics*

PANEL SESSION 2

Monday, November 6, 2000 1:00 p.m. – 2:30 p.m.

InP TECHNOLOGY FOR THE NEW ECONOMY

Organizers and Moderators:
Bill Peatman, Motorola
Jim Sowers, Loral

As the wireless and optical telecommunications infrastructure continues the push to higher bandwidths (e.g. 40 Gb/s switches and >30GHz wireless links), volume manufacturing of very high performance InP technologies poses serious questions and tantalizing opportunities to those seeking to participate in this lucrative business.

This panel will focus primarily on two questions; 1) what substrate technology will provide the best performance/cost advantage (InP substrate or GaAs with metamorphic buffer), and 2) what device technology, HBT and/or HFET, will offer the best cost/performance advantage for a given application. This panel discussion is likely to set the stage for what will become one of the principal developments in compound semiconductor technology for the New Economy.

Panelists include:

Dave Cheskis	*Anadigics*
Ira Deyhimy	*Vitesse*
Steve Lardizabal	*Raytheon*
Amy Liu	*QED/IQE*
Pierre Mandeville	*Nortel*
Dominique Pons	*UMS*
Dwight Streit	*TRW*

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VENDOR PRODUCT FORUM
Low Noise? High Power? Low Cost? Or What?

Tuesday, November 7, 2000 - 1:30 p.m.

Organizer: Mohammad Madihian, *NEC USA Inc*
Moderators:
Mohammad Madihian, *NEC USA Inc*
Norman Chiang, *California Eastern Labs*
Mehran Mokhtari, *HRL*

Forum Members:

Javed Patel	*Anadigics*
Andreas Nitschke	*Infineon*
Warren Barabash	*RF Micro Devices*
Toshio Shino	*Toshiba*
Manny Quijije	*TRW*
Sanjiv L. Shah	*Raytheon*

New product introduction, technical specifications accompanied by actual performance data for RFIC, μ-wave/ *mm*-wave MMIC, Opto-electronic IC, and more. Manufacturability of these products in high volumes, reliability data, ease of use, faster time-to-market, customer re-use capability, excellent cost/performance ratio, price trends and availability. These products include: C-band 2-W high gain high efficiency MMICs, S-band low cost 1-W MMIC with SMD package for WLL residential and base station applications, S-band 3-W & 8-W MMICs for W-CDMA applications, InGaP HBT PA modules for GSM/DCS and linear wireless handsets, HBT based trans-impedance amplifiers for OC 48 and OC192 applications, mixers, switches, receivers, millimeter wave integrated transceivers and more for point-to-point and point-to-multipoint broadband systems.

PANEL SESSION 3

Tuesday, November 7, 2000 - 3:30 p.m. – 5:00 p.m.

INDUSTRY ROADMAP TO 40 GB/S

Organizers/Moderator:
Allan Armstrong, *Vitesse Semiconductor*
Tho Vu, *Top-Vu Technology*

To satisfy the never-ending thirst for bandwidth, the high-speed communications IC community is hard at work creating digital communications ICs to serialize data and transport across optical fiber at increasingly higher data rates. With 2.5 Gb/s physical layers well in hand and 10 Gb/s in volume production, R&D is now focusing on 40 Gb/s. How will such data rates be achieved? What process technologies will be successful? What circuit techniques will be used? When will such products be manufacturable and reliable? How will new technologies such as parallel optical interconnect, all-optical switching, and DWDM affect network architecture? How will IC opportunities be affected by these changes?

Panel Members:

K. C. Wang	*Conexant*
Seshadri Subbanna	*IBM*
John Sitch	*Nortel Networks*
Daniel Rosenthal	*Calient Networks*
Al Yuen	*Alvesta*
Alan Eli Willner	*USC*

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Wednesday, November 8, 2000 - 8:30 a.m.

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Chairpersons: Vincent Hietala, *Sandia National Labs.*
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Wednesday, November 8, 2000 - 8:30 a.m.

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(Invited Paper) Kenjiro Nishikawa, Katsuhiko Araki, NTT Network Innovation Laboratories, Japan; Kenji Kamogawa, NTT DoCoMo, Inc., Japan; Masami Tokumitsu, Suehiro Sugitani, NTT Photonics Laboratories, Japan; Ichihiko Toyoda, NTT Electronics Corp., Japan

I.2 **Power Flip-Chip Assembly for Space Application using HBT in Ku band 157**
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I.4 **KA-Band Planar Gunn Oscillators Using Flip-Chip GaAs Gunn Diodes Fabricated by Boron Ion Implantation 165**
Takashi Yoshida, Tadayoshi Deguchi, Kiyoshi Kawaguchi, Atsushi Nakagawa, New Japan Radio Co., Ltd., Japan

SESSION J

Wednesday, November 8, 2000 - 10:30 a.m.

MILLIMETERWAVE COMMUNICATION ICs

Chairpersons: Mohammad Madihian, *NEC USA Inc*
Steve Consolazio, *Northrop Grumman*

J.1 **A High IP3, Subharmonically Pumped Mixer for LMDS Applications 171**
Paul Blount, Charles Trantanella, Hittite Microwave Corporation, Chelmsford, MA

J.2 **A 60 GHz Integrated Sub-Harmonic Receiver MMIC 175**
C.A. Zelley, A.R. Barnes, D.C. Bannister, R.W. Ashcroft, DERA, Great Britain

J.3 **A 60GHz-band Coplanar-MMIC Chipset for 500Mbps ASK Transceivers 179**
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J.4 **A 77 GHz Coplanar Waveguide MMIC BPSK Vector Modulator Realised Using InP Technology 183**
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SESSION K

Wednesday, November 8, 2000 - 10:30 a.m.

FIBER LINK ICs

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Marko Sokolich, *HRL Laboratories*

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Vincent M. Hietala, QDI, Yorba Linda, CA; Carl Chun, Joy Laskar, Georgia Institute of Technology, Atlanta, GA; K.D. Choquette, University of Illinois, Urbana, IL; K.M. Geib, A.A. Allerman, J.J. Hindi, Sandia National Laboratories, Albuquerque, NM

K.2 **Auto Gain Control Transimpedance Amplifier with Low Noise and Wide Input Dynamic Range for 10Gbps Optical Communication Systems 193**
Hitoshi Ikeda, Tomoyuki Ohshima, Masanori Tsunotani, Shouhei Seki, Tamotsu Kimura, Oki Electric Industry Co., Ltd., Tokyo, Japan

K.3 **49-GHz Preamplifier with a Transimpedance Gain of 52 dBΩ Using InP HEMTs 197**
H. Shigematsu, M. Sato, T. Suzuki, T. Takahashi, K. Imanishi, N. Hara, H. Ohnishi, Y. Watanabe, Fujitsu Laboratories Ltd., Japan

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K.5 **A 10-Gb/s AlGaAs/InGaAs p-HEMT Distributed EA Driver with a D-Flip-Flop for Optical Fiber Links 205**
M. Miyashita, K. Yamamoto, K. Andoh, N. Okada, K. Motoshima, A. Takemoto, Mitsubishi Electric Corporation, Hyogo, Japan

PANEL SESSION 4

Wednesday, November 8, 2000 - 1:00 p.m. – 2:40 p.m.

TOMORROW'S SWITCH - FET OR MEMS?

Panel Organizers and Moderators:
Brad Krongard, *Tyco Electronics M/A-Com*
Malcolm Stubbs, *Communications Research Centre*

FET switches are common components in today's microwave subsystems, however, the emerging MEMs technology is attracting a lot of interest in the microwave community and has demonstrated significant performance advances in the switching arena. While FET technology has an established history, MEMs is the new "kid on the block" and therefore has a long way to go before it becomes accepted. This panel will try to shed some light on the future of the two technologies.

This panel will focus primarily on three questions:
1) what is the current state of FET and MEMs switch technologies;
2) what will be the cost/performance/reliability trade offs between the two technologies;
3) will one of the technologies disappear in the future, or is there a place for both?

Panel Members:

Jeffrey F. DeNatale	*Rockwell*
Karl Freidhoff	*Northrop Grumman*
David Johnson	*Alpha*
Mehran Mokhtari	*HRL*
Wayne Struble	*M/A-COM*

PANEL SESSION 5

Wednesday, November 8, 2000 - 1:00 p.m. – 2:40 p.m.

FAB OR FAB-U-LESS?

Panel Organizers and Moderators:
Mitchell Shifrin, *Hittite*
Norm Chiang, *California Eastern Laboratories*

Along with the exploding growth of the wireless industry there has also been a corresponding explosion of fabless semiconductor companies dedicated to wireless design. In fact fabless companies even have their own association! What is going on here? Are there more specifications then designers to address them? Is it better to separate designers from process folks since at times they tend to be at each other's throats? While this model is relatively common to the Silicon industry it is new to III-V's. Is this the trend of the future or a mere aberration? We have assembled a panel of industry experts that come from companies with vastly different structures. Let's hear what they have to say on the subject.

Panel Members:

Nan-Lei Larry Wang	*EiC*
Sanjay Moghe	*RF Solutions*
Derek Houghton	*SiGe Microsystems*
Wing Yau	*Global Communication Semiconductors*
Kin Tan	*Stanford Microdevices*
Brad Krongard	*Tyco Electronics M/A-Com*

SESSION L

Wednesday, November 8, 2000 - 3:10 p.m.

MICROWAVE & MMW POWER AMPLIFIERS

Chairpersons: Norman Chiang, *California Eastern Laboratories*
Doug Teeter, *RF Micro Devices*

L.1 **A 6W C-Band High Power MMIC Amplifier for a Space Radar Application 215**
Y. Butel, T. Adam, B. Cogo, M. Soulard, Alcatel Space Industries, Toulouse, France

L.2 **K-Band 76% PAE InP Double Heterojunction Bipolar Power Transistors and a 23-GHz Compact Linear Power Amplifier MMIC 219**
W. Okamura, A. Gutierrez-Aitken, E. Kaneshiro, J. Lester, D. Sawdai, P.C. Grossman, H.C. Chen, A. Oki, P. Chin, T. Block, TRW Electronics and Technology Division, Redondo Beach, CA; L.W. Yang, National Taiwan University, Taiwan; K. Kobayashi, Stanford Microdevices, CA

L.3 **Compact, 1 Watt, Power Amplifier MMICs for K-band Applications 223**
Steven A. Brown, James M. Carroll, TriQuint Semiconductor, Richardson, TX

L.4 **1-Watt KA-Band Coplanar High Power MMIC Amplifiers using 0.15 UM GaAs PHEMTs 227**
A. Bessemoulin, H. Massler, A. Hülsmann, M. Schlechtweg, Fraunhofer Institute for Applied Solid-State Physics (IAF), Germany

SESSION M

Wednesday, November 8, 2000 - 3:10 p.m.

HETEROSTRUCTURE BIPOLAR TRANSISTORS

Chairpersons: Tim Henderson, *TriQuint Semiconductor Texas*
Jan-Erik Mueller, *Infineon Technologies*

M.1 **200 GHz InP/GaAs$_x$ Sb $_{1-x}$ /InP Double Heterojunction Bipolar Transistors 233**
C.R. Bolognesi, M.W. Dvorak, O. Pitts, S.P. Watkins, Simon Fraser University, Canada

M.2 **Avalanche Breakdown in HBTs: Variation with Collector Current and Effect on Linearity 237**
Jonathan Scott, Tom Low, Agilent Technologies, Santa Rosa, CA

M.3 **Interaction of Degradation Mechanisms in BE-Doped GaAs HBTs 241**
Darrell Hill, John Parsey, Motorola DigitalDNA™ Laboratory, Tempe, AZ

M.4 **Current Gain Modulation and 1/f Noise Control of GaAs Based HBTs using On-Ledge Schottky Diodes 245**
Pingxi Ma, M.F. Chang, University of California, Los Angeles, CA; Yuefei Yang, R.T. Huang, Global Communication Semiconductor Inc., Torrance, CA; Peter Zampardi, Conexant Systems, Newbury Park, CA; Jerry Sheu, G.P. Li, University of California, Irvine, CA

SESSION N

Wednesday, November 8, 2000 - 3:10 p.m.

Late News Papers

Chairpersons: **TBD**

N.1 **An 18 GHz Continuous Time Σ – Δ Modulator Implemented in InP Transferred Substrate HBT Technology 251**
S. Jaganathan, T. Mathew, Y. Betser, S. Krishnan, Y. Wei, D. Scott, M. Urteaga, M. Rodwell, University of California, Santa Barbara, CA; D. Mensa, Gtran Inc., Westlake Village, CA

N.2 **High Efficiency Power Amplifier Module with Novel Enhancement-Mode Heterojunction FETs for Wide-Band CDMA Handsets 255**
Yasunori Bito, Takehiko Kato, Naotaka Iwata, NEC Corporation, Japan; Teruhisa Kato, Naito Densei Machida Mfg. Co. Ltd., Japan

N.3 **Low DC Power, High Gain-Bandwidth Product, Coplanar Darlington Feedback Amplifiers Using InAlAs/InGaAs Heterojunction Bipolar Transistors 259**
Delong Cui, Shawn Hsu, Dimitris Pavlidis, University of Michigan, Ann Arbor, MI; Donald Sawdai, TRW Electronics, Redondo Beach, CA; Patrick Chin, Tom Block, TRW Electronic Systems and Technology Division, Redondo Beach, CA

N.4 **Directions in TeraHertz Technology 263**
Derek Abbott, Adelaide University, Australia

SESSION A

Monday, November 6, 2000 – 8:30 a.m.

A

PLENARY SESSION

Chairpersons: Tony Immorlica, *Sanders, a Lockheed Martin Company*
Chris Bozada, *US Air Force*

A.1 **The International Technology Roadmap for Semiconductors: Past, Present and Future,** *(Invited Paper)*, Paolo Gargini, *Director Technology Strategy, Intel Fellow.*

A.2 **Review of Silicon-Germanium BICMOS Technology after 4 Years of Production and Future Directions,** *(Invited Paper)*, S. Subbanna, G. Freeman, D. Ahlgren, B. Jagannathan, D. Greenberg, R. Najarian, IBM Microelectronics, Hopewell Junction, NY; J. Johnson, IBM Microelectronics, Essex Junction, VT; P. Bacon, IBM Microelectronics RFIC Design Center, Lowell, MA; D. Herman, B. Meyerson, IBM Research Division, Yorktown Hts., NY

A.3 **GaN HFET Technology for RF Applications,** *(Invited Paper)*, Chanh Nguyen, Miroslav Micovic, Danny Wong, Ara Kurdoghlian, Paul Hashimoto, Paul Janke, Loren McCray & Jeong Moon. *HRL Laboratories., LLC., Malibu, CA*

A.5 **InP-HBT Optoelectronic Integrated Circuits for Photonic Analog-to-Digital Conversion,** *(Invited Paper),* T. Broekaert, W. Ng, J. Jensen, D. Yap, R Walden, HRL Laboratories, LLC., Malibu, CA

The International Technology for Semiconductors (ITRS): "Past, Present and Future"

A

Paolo Gargini

Director Technology Strategy

Intel Fellow

Chairman ITRS

Introduction

The semiconductor industry has continued to prosper and also to foster the growth of multiple industries since the early 1970s. The main advantage of the semiconductor industry, as compared with other industries, resides in one unique factor that has made the semiconductor industry successful: "Decreases in device feature size have provided improved functionality at a reduced cost." Device linear features have indeed decreased at the rate of about 70% every three years for most of the industry's history. Acceleration to a 2-year cycle has been experienced in the most recent years. Cost per function has simultaneously decreased at an average rate of about 25–30%/year/function. Silicon technology has played and continues to play a major role in sustaining the semiconductor industry growth.

How long will the semiconductor industry be able to sustain this growth?

The past

Since 1992, the Semiconductor Industry Association (SIA) has coordinated the efforts of producing what was originally named the *National Technology Roadmap for Semiconductors* (NTRS). This document of requirements and possible solutions was generated three times: in 1992, 1994, and 1997. The NTRS has provided, during this time, a 15-year outlook on the major trends of the semiconductor industry. As such, it has become a good reference document for all semiconductor manufacturers. Most of all, it has provided useful guidance for suppliers of equipment, materials and software. It has also provided clear targets for researchers in the outer years.

The semiconductor industry has become a global industry in the '90s, as many semiconductor suppliers have established manufacturing or assembly facilities in multiple regions of the world. Similarly, the suppliers to the semiconductor industry have established worldwide operations. Furthermore, alliances, joint ventures, and many forms of cooperation have been established among semiconductor manufactures as well as among equipment, materials, and software suppliers.

The above considerations have led to the realization that a document that provides guidance for the whole industry would benefit from inputs from all regions of the world that have leadership activities in the field of semiconductors.

The present

This realization has led to the creation of the *International Technology Roadmap for Semiconductors* (ITRS). The invitation to cooperate on the ITRS was extended by the SIA at the World Semiconductor Council in April of 1998. The offer was enthusiastically accepted by the trade organizations of Europe (EECA), Korea (KSIA), Japan (EIAJ), and Taiwan (TSIA). The initial collaboration of these five organizations produced the ITRS 1998 Update, which consisted of a comprehensive revision of the 1997 NTRS tables. Last year, the five regions have jointly produced a new edition of the semiconductor industry roadmap document—*The International Technology Roadmap for Semiconductors: 1999*. The 2000 ITRS Update is presently underway.

As reported in the 1999 ITRS, the number and the difficulty of the technical challenges that need to be overcome continue to increase as technology moves forward. The red areas, signifying "No solutions yet", are in most cases shown within a 5-year reach. Traditional scaling, which has been at the basis of the semiconductor industry for the last 30 years, is indeed beginning to show the fundamental limits of the materials constituting the building blocks of the planar CMOS process. However, it is clearly outlined in the 1999 ITRS that new materials can be introduced in the basic CMOS structure to replace and/or augment the existing ones to further extend the device scaling approach. Since the assimilation of these new materials into the modified CMOS process gives the device physicist and the circuit designer improved electrical performance similar to the historical trends, this new regime has been often identified as "Equivalent Scaling." It is expected that these new materials will provide a viable solution to extending the limit of the planar CMOS process for the next 5–10 years.

The future

Despite the use of these new materials, it will be challenging to maintain the historical rate of improvement in electrical performance of about 2× every two years in the high-performance components by relying exclusively on improvements in technology. Innovation in the techniques used in circuit and system design will be essential to maintain the historical trends in performance improvement. To achieve this result it is expected that the integration of multiple silicon technologies on the same chip and a closer integration of package and silicon technology will be necessary. This emerging product category is identified as Performance System-on-a-Chip (P-SoC).

On the other hand, cost-effective solutions will require an assessment of the silicon technology complexity that can be afforded for a given cost. Specifically, given a system cost target, what technology complexity can be afforded? This product category is identified as Cost-effective System-on-a-Chip (C-SoC).

Finally, as the ITRS looks 10–15 years in the future, it becomes evident that most of the known technological capabilities will be approaching or will have reached their limits by then. In order to continue providing the computer, communication, consumer, and other electronics industries with more efficient building blocks, it becomes necessary to investigate new devices that may provide a more cost-effective alternative to planar CMOS in this timeframe. Adequate preparation for this potential transition must include starting to identify the possible candidates as early as possible and, then, systematically testing their feasibility.

Conclusions

The planar CMOS silicon gate technology resulted from technical investigations initiated in the 1940s. However, these early studies did not lead to the start of the semiconductor industry, as we know it today, until the late 60s. It would be difficult for any single company to support the progressively increasing R&D investments necessary to evolve the technology from Traditional Scaling to Equivalent Scaling, and also provide the resources necessary to investigate and develop a set of new devices usable beyond the limits of CMOS. The contributors to the ITRS agree that much of the R&D activities can be carried on if multiple companies agree to jointly operate in the shared "pre-competitive domain."

It is the purpose of the 1999 ITRS, of the 2000 ITRS Update, and of future ITRS documents, to provide a set of up-to-date reference documents of requirements, potential solutions, and their timing for the semiconductor industry. These documents have already provided a common reference for international forums that have initiated discussions on cooperation among the leading silicon semiconductor manufacturers and the leading suppliers of equipment, materials, and software, as well as researchers from university and government laboratories. It is hoped that in the near future, through cooperative efforts among the various ITRS participants, the challenge of R&D investments will be more effectively and more uniformly shared by the whole semiconductor industry.

In addition, as the integration of multiple functions (e.g., voice, data, video etc) continues as driven by the recent growth of the Internet, it becomes necessary to also integrate multiple hardware and software technologies in order to provide the best cost-performance solutions to the users. Not all of these functions can be realized by simply using silicon technology alone. This has become apparent in the last few years as non-silicon semiconductor devices and also optical devices, for instance, have experienced an unprecedented growth. In an effort to better synchronize the availability of all these technologies and to also further reduce the cost of the overall solutions to the users, it would appear beneficial if silicon ad non-silicon semiconductor roadmaps could be more closely aligned.

I would like to take the opportunity of this presentation to encourage the non-silicon semiconductor experts to begin cooperating with the mostly silicon-oriented ITRS committees and working groups to explore the possibility of closer and continuously strengthening cooperation. I believe that both users and producers could benefit from this activity.