1998 IEEE GaAs IC SYMPOSIUM

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IEEE GALLIUM ARSENIDE INTEGRATED CIRCUIT SYMPOSIUM
Co-Sponsored by The IEEE Electron Devices Society,
The IEEE Microwave Theory and Techniques Society, and
The IEEE Solid-State Circuits Society

20th Annual

TECHNICAL DIGEST 1998

ATLANTA, GEORGIA

NOVEMBER 1 – 4, 1998

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WELCOME TO THE 1998 IEEE GaAs IC SYMPOSIUM

On behalf of the organizing committee and the IEEE EDS, MTT-S, and SSCS, I welcome you to the 20th Anniversary (1998) IEEE GaAs IC Symposium at Atlanta's beautiful Westin Peachtree Plaza Hotel.

This GaAs IC Symposium continues its tradition of presenting the best from around the world in GHz frequency microelectronics. Forty percent of this year's technical papers come from outside the US. This year's program is also indicative of the dramatic adoption over the past several years of GaAs technology for commercial applications in addition to the traditional government supported technology and applications. Major focus areas of this year's GaAs IC Symposium, organized by Mark Wilson and the Technical Program Committee, include state-of-the-art circuits and technology for: wireless and broadband communications; very high speed digital communications; highly efficient, linear, power amplifiers; interface electronics and signal processing; and mm-wave defense and automotive systems.

This 20th IEEE GaAs IC Symposium also continues our tradition of providing focused educational opportunities through our Short Course and Primer Course, both held on Sunday. Jim Komiak has organized a very interesting and highly applicable one-day Short Course on "Power Amplifiers: From Milliwatts to Kilowatts," taught by five experts in the industry. In addition, Stephen Long and Donald Estreich will once again present our Sunday evening Primer Course on the "Basics of GaAs ICs" which is not only tutorial but is presented within the context of this year's Symposium.

To complement the full technical program, we have provided several social events to provide opportunities to interact with colleagues while catching up with the newest technology available on the market. These events include the Sunday evening Opening Reception, the Monday evening Technology Exhibition Reception in the GaAs IC Technology Exhibition Hall, and the Tuesday evening 20th Birthday Party at Atlanta's Hard Rock Cafe. We hope to see you there.

We will also provide opportunities for you to learn of new products just hitting the market to help us in the III-V microelectronics business through approximately 40 exhibits at the GaAs IC Technology Exhibition. Additionally, potential customers for the latest commercially available GaAs ICs can learn about these in the Vendor Product Forums.

Finally, I want to mention two new features of the GaAs IC Symposium. We will be presenting our first "Outstanding Paper Award" from the 1997 Symposium to Taiichi Otsuji et al. from NTT for their paper titled: "An 80 Gbit/s Multiplexer IC Using InAlAs/InGaAs/InP HEMTs." In addition, we are entering our second Symposium with support from corporate benefactors. We gratefully acknowledge the support of Watkins-Johnson and Sumitomo Electric Co., USA, and we may be welcoming others at the Opening Session.

We're pleased you're here in Atlanta for this special 20th IEEE GaAs IC Symposium, and we hope that you enjoy this outstanding technical and educational program!

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Chairman, 1998 IEEE GaAs IC Symposium

1998 IEEE GaAs IC Symposium Organizers

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SYMPOSIUM HEADQUARTERS

The Westin Peachtree
Atlanta, Georgia

SYMPOSIUM AT A GLANCE

SATURDAY, OCTOBER 31, 1998

REGISTRATION (Short Course & Primer Course Only)	6:00 p.m.-8:00 p.m.	Mart Bridge – Level 6

SUNDAY, NOVEMBER 1, 1998

REGISTRATION (Short Course & Primer Course Only)	7:00 a.m.-8:00 a.m.	Mart Bridge – Level 6
Continental Breakfast for Short Course	**7:00 a.m.-7:45 a.m.**	**Six Flags Foyer**
SHORT COURSE: "Power Amplifiers: From Milliwatts to Kilowatts Cool Devices...with Hot Performance"	8:00 a.m.-4:45 p.m.	French/American
GaAs Reliability Workshop	8:00 a.m.-5:00 p.m.	TBA
Short Course Lunch	**12:00 p.m.-1:30 p.m.**	**English/Canadian**
REGISTRATION for Symposium (and Primer Course until 5:30)	5:00 p.m.-8:00 p.m.	Mart Bridge – Level 6
PRIMER COURSE: "Basics of GaAs ICs"	5:30 p.m.-8:30 p.m.	French/American
Symposium Opening Reception	**6:00 p.m.-9:00 p.m.**	**Peach State – Level 6**

MONDAY, NOVEMBER 2, 1998

REGISTRATION	7:00 a.m.-5:00 p.m.	Mart Bridge – Level 6
Continental Breakfast	**7:00 a.m.-8:00 a.m.**	**9th Level Terrace**
SYMPOSIUM OPENING	8:00 a.m.-8:30 a.m.	Plaza Ballroom – Level 9
SESSION A: Plenary Session	8:30 a.m.-11:30 a.m.	Plaza Ballroom – Level 9
Buffet Lunch	11:30 a.m.-12:30 p.m.	Peach State Room – Level 6
PANEL SESSION 1: Does Si Own the Communication Market?	12:30 p.m.-2:00 p.m.	Canadian/Spanish/Georgian
VENDOR PRODUCT FORUM 1	12:30 p.m.-2:10 p.m.	English/French/American
SESSION B: Millimeter Wave Amplifiers	2:35 p.m.-4:15 p.m.	Canadian/Spanish/Georgian
SESSION C: 40 Gb/s Mixed Signal and LSI Circuits	2:30 p.m.-4:10 p.m.	English/French/American
GaAs IC Technology Exhibition Opening Reception	**5:00 p.m.-7:00 p.m.**	**Atlanta Merchandise Mart**
SEMI Compound Semiconductor Standards Committee Meeting	8:00 p.m.-10:00 p.m.	TBA

TUESDAY, NOVEMBER 3, 1998

REGISTRATION	7:00 a.m.-5:00 p.m.	Mart Bridge – Level 6
Continental Breakfast	**7:00 a.m.-8:00 a.m.**	**Atlanta Merchandise Mart**
GaAs IC TECHNOLOGY EXHIBITION	7:00 a.m.-4:00 p.m.	Atlanta Merchandise Mart
SESSION D: Power Amplifiers	8:30 a.m.-10:05 a.m.	Canadian/Spanish/Georgian
SESSION E: Active Device Modeling	9:00 a.m.-11:30 a.m.	English/French/American
SESSION F: Ultra-High Speed ICs for Frequency	10:30 a.m.-12:05 p.m.	Canadian/Spanish/Georgian
Exhibition Luncheon	**12:00 noon-1:30 p.m.**	**Atlanta Merchandise Mart**
SESSION G: Frequency Translation Techniques	1:30 p.m.-2:55 p.m.	Canadian/Spanish/Georgian
SESSION H: Advances in HBT Technology	1:30 p.m.-3:05 p.m.	English/French/American
PANEL SESSION 2: Broadband Networking: Will you always be so wired?	3:30 p.m.-5:00 p.m.	English/French/American
Symposium Birthday Party	**7:00 p.m.-10:00 p.m.**	**Hard Rock Cafe**

WEDNESDAY, NOVEMBER 4, 1998

REGISTRATION	7:00 a.m.-12:00 noon	Mart Bridge – Level 6
Continental Breakfast	**7:00 a.m.-8:00 a.m.**	**9th Level Terrace**
SESSION I: Mobile and Automotive Technology	8:00 a.m.-9:25 a.m.	Canadian/Spanish/Georgian
SESSION J: Advanced FET Technology	8:00 a.m.-9:35 a.m.	English/French/American
SESSION K: High Integration Signal Processing	10:00 a.m.-11:05 a.m.	Canadian/Spanish/Georgian
PANEL SESSION 3: Are HBTs Reliable?	10:00 a.m.-11:30 a.m.	English/French/American
PANEL SESSION 4: Mixed Mode RF-MCM vs. Single Chip	12:30 p.m.-2:00 p.m.	Canadian/Spanish/Georgian
VENDOR PRODUCT FORUM 2	12:30 p.m.-2:10 p.m.	English/French/American
SESSION L: Novel High Performance Circuits	2:15 p.m.-4:00 p.m.	Canadian/Spanish/Georgian
SESSION M: Advances in Manufacturing Technology	2:15 p.m.-4:00 p.m.	English/French/American
Close of Symposium	**4:40 p.m.**	

Visit us on the World-Wide Web at: http://www.gaasic.org/

Coffee Breaks:

Primer Course and Short Course Registrants (only) –
Sunday, November 1: Six Flags Foyer, Level 7

Symposium Registrants -
Monday, November 2: 9th Level Terrace
Tuesday, November 3: Atlanta Merchandise Mart
Wednesday, November 4: 9th Level Terrace

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PROGRAM INDEX

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SESSION C

Monday, November 2, 1998 - 2:30 p.m.

40 GB/S MIXED SIGNAL AND LSI CIRCUITS

Chairpersons: Steve Long,
University of California, Santa Barbara
William Davenport,
TriQuint Semiconductor

SESSION D

Tuesday, November 3, 1998 - 8:30 a.m.

POWER AMPLIFIERS

Chairpersons: Jim Komiak,
Sanders, A Lockheed Martin Company
Dave Osika,
Anadigics

SESSION E

Tuesday, November 3, 1998 - 9:00 a.m.

ACTIVE DEVICE MODELING

Chairpersons: Marc Rocchi,
Phillips Microwave
Tim Henderson,
TriQuint Semiconductor

SESSION F

Tuesday, November 3, 1998 - 10:30 a.m.

ULTRA-HIGH SPEED IC's FOR FREQUENCY

Chairpersons: Mehran Mokhtari,
Royal Institute of Technology, Sweden
Chung-Yi Su,
Hewlett-Packard

SESSION G

Tuesday, November 3, 1998 - 1:30 p.m.

FREQUENCY TRANSLATION TECHNIQUES

Chairpersons: Brad Nelson,
Pacific Monolithics, Inc.
Mitch Shifrin,
Hittite Microwave Corporation

SESSION H

Tuesday, November 3, 1998 - 1:30 p.m.

ADVANCES IN HBT TECHNOLOGY

Chairpersons: Katerina Hur,
Hewlett-Packard
Jan-Erik Mueller,
Siemans AG

Tuesday, November 3, 1998 - 3:30 p.m. – 5:00 p.m.

BROADBAND NETWORKING:
Will you always be so wired?

Organizers/Moderators:
Mitch Shifrin, *Hittite Microwave Corporation*
Brad Nelson, *Pacific Monolithics Inc.*

Many technologies are competing for the emerging high speed data and telephony services in the business and consumer markets. This panel will address Local Multipoint Distribution Services (LMDS), Multi-channel Multipoint Distribution Services (MMDS), satellite services, Digital Subscriber Line (DSL) and wired hybrid fiber cable services. Circuit and network system issues will be discussed and their application to the GaAs community. The panelists will address the wired verses wireless technology trade-offs and their limitations. In order to surface the key issues the forum is encouraging energetic participation of the audience.

Panel Members:

Rick Compton	*Lucent*
Eric Wilson	*Pacific Monolithics*
Tom Quigley	*Broadcom*
J. Miller	*Teledesic*

SESSION I

Wednesday, November 4, 1998 - 8:00 a.m.

MOBILE AND AUTOMOTIVE TECHNOLOGY

Chairpersons: Mohammad Madihian, *NEC*
Kevin Kobayashi, *TRW*

SESSION J

Wednesday, November 4, 1998 - 8:00 a.m.

ADVANCED FET TECHNOLOGY

Chairpersons: Albert Baca, *Sandia National Laboratories*
Byung-Jong Moon, *Vitesse Semiconductor*

SESSION K

Wednesday, November 4, 1998 - 10:00 a.m.

HIGH INTEGRATION SIGNAL PROCESSING

Chairpersons: Zachary J. Lemnios, *MIT Lincoln Laboratory*
John Sitch, *Nortel Technology*

Wednesday, November 4, 1998 - 10:00 a.m. – 11:30 a.m.

ARE HBTs RELIABLE?

Organizer/Moderator: Robert Anholt, *Gateway Modeling*

This panel brings together HBT users and IC manufacturers to discuss AlGaAs HBT reliability.

We will address the following questions:

What are the characteristics of HBT degradation that are of concern to users?

How should we be measuring HBT reliability?

What physical evidence, such as TEM and optical observations, exists to support our ideas about HBT degradation?

Various solutions have been proposed in the literature to improve HBT reliability such as carbon-doped bases, relieving base stress and base hydrogen incorporation, ledge passivation, MBE vs MOCVD growth, and InGaAs contacts. What is the present experience implementing and verifying these ideas in the industry?

Panel Members:

Tim Henderson	*TriQuint Semiconductor*
Anant Dixit	*Qualcomm*
Aditya Gupta	*Northrop Grumman*
Chris Bozada	*AFRL Sensors Directorate*
Frank Yamada	*TRW*
Raj Sahai	*Rockwell*

SESSION A

Monday, November 2, 1998 - 8:30 a.m.

PLENARY SESSION

Chairpersons: John Sitch, *Nortel Technology*
Chris Bozada, *Air Force Research Laboratory*

A.1 **ROADMAPPING RFIC TEST** (Invited Paper), E. Strid, *Cascade Microtech, Inc., Beaverton, OR*

A.2 **BREAKDOWN IN MILLIMETER-WAVE POWER InP HEMTs: A COMPARISON WITH PHEMTs** (Invited Paper), J. del Alamo & M. Somerville, *Massachusetts Institute of Technology, Cambridge, MA*

A.3 **RF-TO DIGITAL RECEIVERS EMPLOYING BANDPASS MULTIBIT ΣΔ ADC ARCHITECTURES** (Invited Paper), L. Pellon, *Lockheed Martin Government Electronic Systems*

A.4 **EFFICIENCY AND LINEARITY IMPROVEMENT IN POWER AMPLIFIERS FOR WIRELESS COMMUNICATIONS** (Invited Paper), P. Asbeck, G. Hanington, P. Chen & L. Larson, *University of California, San Diego, La Jolla, CA*

A.5 **APPLICATIONS AND PERFORMANCE OF VCSELs** (Invited Paper), K. Choquette, A. Allerman, H. Hou, K. Geib & B. Hammons, *Sandia National Laboratories, Albuquerque, NM*

Roadmapping RFIC Test

Eric Strid
Cascade Microtech, Inc.

I. Introduction: Why all the roadmapping hype?

The Semiconductor Industry Association (SIA), The Institute for Interconnecting and Packaging Electronic Circuits (IPC), and the National Electronics Manufacturing Initiative (NEMI) have expanded US industry-wide consensus efforts to chart out the futures of everything from semiconductor lithography to factory automation technologies [1-3], including the first draft of a roadmap for RF components in the 1996 NEMI work. To the independent researcher, such roadmaps may seem like an unnecessary and perhaps harmful restriction of creative thinking; however, the silicon IC industry has shown industry roadmapping to be invaluable for ensuring that technologies and infrastructure are production-ready and affordable as new generations of IC's become available. Rather than a restraint on innovation, technology roadmaps give effective guidance to private, government, and academic R&D investment decision processes.

The more a new approach deviates from the industry technology roadmap, the larger the performance or cost benefit it must produce to be adopted. For example, researchers have prototyped improved-Q spiral inductors on Si by etching away the Si under the inductors; but anyone aware of the Si process technology roadmaps would know that such a process will never be adopted and therefore will have very limited impact. On the other hand, there is extremely high interest in RF circuit designs that are 100% compatible with mainstream 0.25- and 0.18-um CMOS processing, so that these may be integrated as blocks for system-on-a-chip (SOC) applications.

The GaAs industry grew up from technology pioneers who typically want to do their own thing, resulting in far too many incompatible processes, few second sources, and too many fragmented R&D efforts below critical mass. This in turn has been sub-optimal in a business sense for time to market or return on investments. The future of GaAs (or Si bipolar or SiGe or SOI) is doomed unless the rate of learning (as reflected in roadmap parameters of integration levels, performance, yields, and costs) can exceed that of the CMOS competitors.

This paper reviews recent RF industry practice in the areas of RFIC on-wafer and package testing, and predicts future trends in RFIC production testing. (RF IC's are generally referred to herein as any IC operating in the 1 to 100 GHz range.)

The testing and packaging issues for GaAs IC's are substantially the same as for Si IC's operating in the same frequency range and function. So while it is unlikely that there will be any inherent differential packaging or test advantages of GaAs over Si, it is similarly imperative to stay on or ahead of the industry roadmap to be competitive with the latest packaging and test technologies.

II. RF Packaging Trends

It is clear that commercial GaAs IC's have predominantly utilized the packaging infrastructure of the silicon IC industry, and that this will likely continue. Surface-mount leadframed packages like the small-outline package (SOP), shrunk SOP (SSOP), quarter-size SOP (QSOP), and thin shrunk SOP (TSSOP), in pitches from 50 to 25 mils, are most popular for 1 and 2 GHz RFIC's today (Fig. 1), with adaptations of BGA and MCM technologies up to 6 GHz emerging in 1998 (Fig. 2). In all cases, the drive for package size reduction has allowed lower parasitic inductances and higher frequency operation.

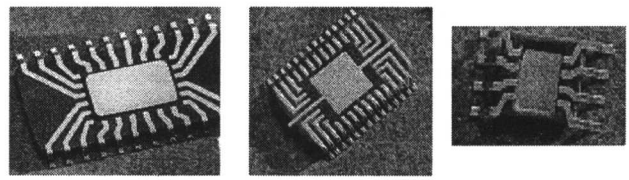

Fig. 1. Typical 24-, 28-, and 8-lead small-outline package (SOP) leadframe styles used for RFIC's.

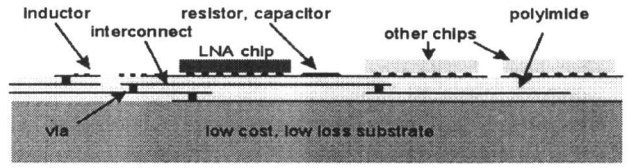

Fig. 2. Cross-section of one style of MCM being developed for RF applications [4].

The 1997 SIA roadmap predicts digital package pin or ball count up to 900 and off-chip clock rates up to 700 MHz, at a cost of 1.1 to 2.3 cents per pin, by 2001 [5]; using such technology, it is clear that L-band RFIC or integrated RF front-end functionality will be supportable, even if it requires the use of many package lines for RF isolation. These future packages will probably take the forms of various

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chip-scale packages (CSP) and/or use flip-chip IC attachment onto high-frequency module substrates or directly onto PCB's (Fig. 3).

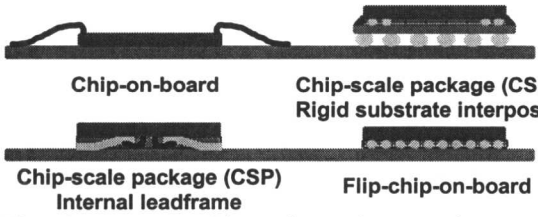


Fig. 3. Some chip-scale and no-package cross sections.

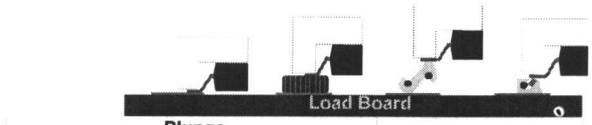
Millimeter-wave IC's will likely be flip-chip attached to high-precision printed substrates. R&D efforts on millimeter-wave packaging should focus on the high-frequency compatibility of a standard Si-developed flip-chip process and materials set, since any significant deviation in new materials or process schemes will likely never be adopted. For example, Hughes adapted Delco's flip-chip process for use on GaAs [6].

The shear quantity of different package types is a drain on test floor overhead costs. Each package type today requires a new handler kit and a new contactor, implying extra cost, leadtime, and setup times, while the diversity of package styles dilutes knowledge learned from other package types. Test, assembly and packaging vendors and technologies are now numerous and diverse (there are thousands of JEDEC package outlines), offering some ripe opportunities for integration and standardization.

III. Trends in RFIC Test

In addition to more traditional rack-and-stack programmable instruments, high-throughput RF ATE systems are now available from a variety of vendors. These systems are typically available with from 2 to 20 RF ports, with tester-per-pin capabilities except for synthesizer resources, and with a dc subsystem to provide bias and control signals. As chip integration levels increase, there will be more mixed-signal ATE that include RF test capabilities. These systems can be interfaced to either packaged-part handlers or wafer probers. One of the main challenges today is making contact consistently for millions of parts, while controlling fixture parasitics (mainly inductances) so that they don't impair the measurements. Consistent contact is especially problematic with packaged parts, since package mechanical tolerances are far less controlled than IC and wafer dimensions. Fig. 4 shows some contactors used for RFIC's today.

RF test capabilities for engineering applications



Parameter	Plunge to Board	Z-elastomers	Johnstech	HP
Common-lead Inductance	(reference)	~ 0.5 nH	1.2 nH	0.5 nH
Contact Life (cycles)	500 to 100,000*	~ 10,000	~ 100,000	~1,000,000
Compliance	(none)	~ 5 mils	~ 10 mils	~ 5 mils

* Poor repeatability

Fig. 4. Popular RF package contactor approaches.

will largely evolve from existing solutions, with tough issues potentially arising in the areas of very high isolation measurements across a chip or module, and integrated antenna measurements [3]. There is a need for a standard isolation test methodology, to promote industry-wide comparisons and learning. RF production test issues include faster measurements of adjacent channel power (ACP) for power amplifiers, how to test integrated passives (including antennae), and probes and contactors for increasingly dense and complex packages.

IV. The Cost of Test

Until processes routinely reach 100% yield on greater than 99% of all lots, test will be required to add value to IC's. The real cost of production IC test varies widely depending upon the device type, and this parameter mostly escapes consensus in the roadmaps, with only a constant cost per digital tester channel called out in the SIA roadmap. And yet overall test productivities must improve by 25-30% per year for any given function, in order to keep pace with other IC costs [7].

Test cost reduction strategies fall into three categories: test less, test earlier, or test faster. The "test less" approach cuts out test steps that are duplicated at other steps (such as wafer vs. package test), or are unnecessary as determined by correlation data; but customer AQL's will still require 100% functional test of some sort for the foreseeable future. To some extent, higher integration levels automatically test less, in that a whole string of cells can be tested end-to-end instead of each individually (indeed, the internal nodes become less accessible anyway). The "test earlier" strategy reduces other costs, such as package scrap, by more complete testing at an earlier stage; examples include more performance predictions from PCM measurements, or RF performance screen at the wafer level, followed by only continuity testing after packaging (see Fig. 5). The "test faster" strategy increases equipment throughput by increasing up time, by