ANALYSIS AND DESIGN OF DIGITAL INTEGRATED CIRCUITS

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PREFACE

This textbook deals with the analysis and design of digital integrated circuits (ICs). Although a large part of the book is concerned with the internal design of digital ICs, we also want it to be helpful to the user of digital ICs. In practice we find the design and use of digital ICs to be closely linked, and a knowledge of both is important to the designer and the user. There are, by far, many more users than designers, but it is our experience that a working knowledge of IC design is a great advantage to the IC user. This is particularly true when the user must choose from a number of competing designs to satisfy a particular requirement. An understanding of the IC structure is important in evaluating the relative merits of different designs in the presence of electric noise or variations in supply voltage. The user who understands the internal operation of integrated circuits is better able to interpret manufacturers' data sheets. He or she is also better prepared to anticipate the likely significance of progress in integrated circuit technology.

The book contains many worked-out examples. These are used to illustrate the principles of analysis and design, and also to impart some practical knowledge of digital ICs. Within most chapters, at the conclusion of main sections, there are exercise problems (with answers at the back of the book). Thus students are able to assure themselves that they comprehend the section before proceeding to the next. At the end of each chapter there are a number of problems covering the subject matter of the whole chapter. Solutions for these problems are included in a *Solutions Manual* available from the publisher.

A summary is given at the end of each chapter. It is intended to help the student review the material and to focus attention on the essential concepts developed in the chapter.

At the end of Chapters 2 through 8 two or three demonstrations or laboratory experiments are described. These are intended to stimulate understanding and retention of the material, and to illustrate the quality of agreement between design theory and experimental reality. In a small class these demonstrations may be incorporated into the lecture period. At Berkeley, students perform these experiments in weekly 3-hour laboratory sessions which are a required part of our course. We find that students profit from the experience of performing these experiments themselves, preferably following the coverage of the subject material in lectures. We believe that in engineering, theory alone is only half a loaf.

We expect that the third- and fourth-year electrical engineering students using this text will already have had an introductory course in electronic circuits and will have been introduced to the basic elements of logic design. Students who have completed a course on semiconductor devices will find that they can cover Chapters 2, 4, and 5 rather quickly. However, this material should not be omitted, because the important emphasis here is on directly measurable electrical characteristics, circuit properties of devices, and device model parameters for circuit simulation. Many semiconductor device courses, in contrast, place principal emphasis on semiconductor band structure and carrier transport phenomena.

For a 15-week semester course, with 3 hours of lecture and a 3-hour laboratory period each week, the text may be covered at the rate of about one chapter each week, with the exception that two weeks are required to cover each of Chapters 3 and 7. In a 10-week quarter course, only the first 8 chapters can be covered thoroughly.

A chapter-by-chapter outline of the topics covered is given below.

Chapter 1
INTRODUCTION TO DIGITAL ELECTRONICS

In this first chapter we briefly review important concepts of logic functions and Boolean identities. The essentials of integrated circuit fabrication technology are briefly described. Definitions of the various complexity levels up to very large scale integration (VLSI) are presented. We introduce the basic properties of a digital circuit and describe the ideal logic element in terms of its static input-output characteristics. We also define important characteristics of digital circuits such as noise margin and propagation delay time. The growing role of computer tools in analysis and design is noted. As a practical example of digital integrated circuit design, we introduce the programmable logic array.

Chapter 2
METAL-OXIDE-SEMICONDUCTOR (MOS) TRANSISTOR

The tremendous impact of the MOSFET in digital ICs is reflected in our early introduction of the subject. At the start of this chapter we briefly discuss some of the physical properties of the MOSFET, as well as the fabrication process for the device. We then give a detailed analysis of the static and then the dynamic characteristics of the MOS transistor. The SPICE model for the MOS transistor is described and means for measuring model parameters on a given device are presented.

Chapter 3
MOS INVERTERS AND GATE CIRCUITS

This is the core chapter on MOSFET digital circuits. We first describe the static properties of a simple MOSFET inverter, which is mainly concerned with obtaining the voltage transfer characteristics (V_{out} versus V_{in}) of the various inverter-load connections of the NMOS transistor. The analysis of dynamic properties, that is, the switching time, is then presented for NMOS inverters. Next the static and dynamic properties of a CMOS inverter are developed. We then describe the analysis and design of simple NMOS and CMOS gate circuits in terms of their static and dynamic properties. Circuit modeling and simulation using program SPICE, dynamic logic techniques, and the important topic of scaling in MOS circuits are also presented in this chapter.

Chapter 4
SEMICONDUCTOR DIODES

The topic now changes from unipolar to bipolar circuits. At the start of this chapter we briefly discuss some of the physical properties of the *pn* junction diode, including the equilibrium barrier potential and depletion region charge. The *I-V* characteristics describing the operation of the device with forward and reverse bias are then derived. The effect of temperature on these equations is also discussed. The dynamic characteristics of the *pn* junction are covered by an analysis of the diode switching times. For practical application we describe the properties of various diode configurations possible with integrated circuits. The Schottky-barrier diode is introduced and its static and dynamic properties described. The SPICE model of the diode and methods for measurement of the model parameters are included. Finally, the effect of voltage breakdown in the *pn* junction is briefly discussed.

Chapter 5
BIPOLAR JUNCTION TRANSISTOR

Following on from Chapter 4. in this chapter, after a brief description of transistor operation, we derive the basic static equations for the bipolar transistor. The various modes of operation of the transistor are then described and simpler equations derived. The SPICE model of the bipolar transistor and methods for measurement of the model parameters are presented.

Chapter 6
BIPOLAR TRANSISTOR INVERTER

The core material for the bipolar digital ICs is found in Chapters 6 and 7. We start this chapter with a development of the static characteristics of a simple bipolar inverter, namely, the voltage transfer characteristic. From this we obtain the noise margins and derive equations for the fan-out. The dynamic characteristics of the inverter are described in terms of the charge-control model. Simpler forms of the charge-control equations are then derived for each of the operating modes of the transistor. These equations are then used in an illustrative example to compute the switching times of the bipolar inverter. In a similar manner the static and dynamic properties of a Schottky-clamped inverter are covered. A comparison of the results of hand analysis and computer simulation using SPICE is also included.

Chapter 7
BIPOLAR DIGITAL GATE CIRCUITS

In this chapter we present a detailed study of the major types of IC digital gates, namely RTL, DTL, TTL, ECL, and I^2L. Especially emphasized are the latest developments in TTL, ECL, and I^2L. Both static and dynamic characteristics are covered in detail.

Chapter 8
REGENERATIVE LOGIC CIRCUITS

From strictly combinational circuits, in Chapter 8 we move our attention to sequential circuits. After describing the basic operation of a simple bistable circuit, the properties of the *SR* latch, the *JK* and *D* flip-flops are described with the aid of logic diagrams. Examples are then given of the implementation of these regenerative circuits in both MOS and bipolar technologies, specifically NMOS, CMOS, TTL, ECL, and I^2L. Also included in this chapter are descriptions of the Schmitt trigger circuit as well as monostable and astable multivibrator circuits. Examples of each of these circuits implemented with CMOS and bipolar technologies are presented.

Chapter 9
SEMICONDUCTOR MEMORIES

In Chapter 9 we enter the world of large-scale integration (LSI). Read-only memories (ROMs) are described in both MOS and bipolar technologies. Details of the cells in the array, as well as the peripheral circuits, are presented. The use of MOSFET and bipolar circuits in static read-write memories (SRAMs) are also described. Three-transistor (3T) and one-transistor (1T) cells, widely used in dynamic read-write memories (DRAMs), are explained, and information on application of standard dynamic RAMs is included. The chapter concludes with a short section on bucket-brigade and charge-coupled device (CCD) serial memories.

Chapter 10
CIRCUIT DESIGN FOR LSI AND VLSI

Several more advanced topics are covered in Chapter 10. Advantages and drawbacks of gate arrays, which are popular in the design of semi-custom digital ICs, are described for CMOS and bipolar technologies. More complex circuits of this form of design such as standard cells and programmable logic arrays are also described. The final section of this chapter is concerned with specialized examples of circuit design for VLSI.

We acknowledge with thanks the many comments and suggestions of students and colleagues that aided us in preparing this textbook. Professor Robert Dutton and Lanny Lewyn of Stanford University gave us very helpful, detailed suggestions on several chapters. We especially wish to thank Professor Donald O. Pederson of the University of California, Berkeley. He greatly influenced our planning of the organization and content of this text, and has been a continuous source of constructive criticism and encouragement. Our appreciation goes also to Ms. Bettye Fuller and Ms. Doris Simpson, who typed portions of the manuscript.

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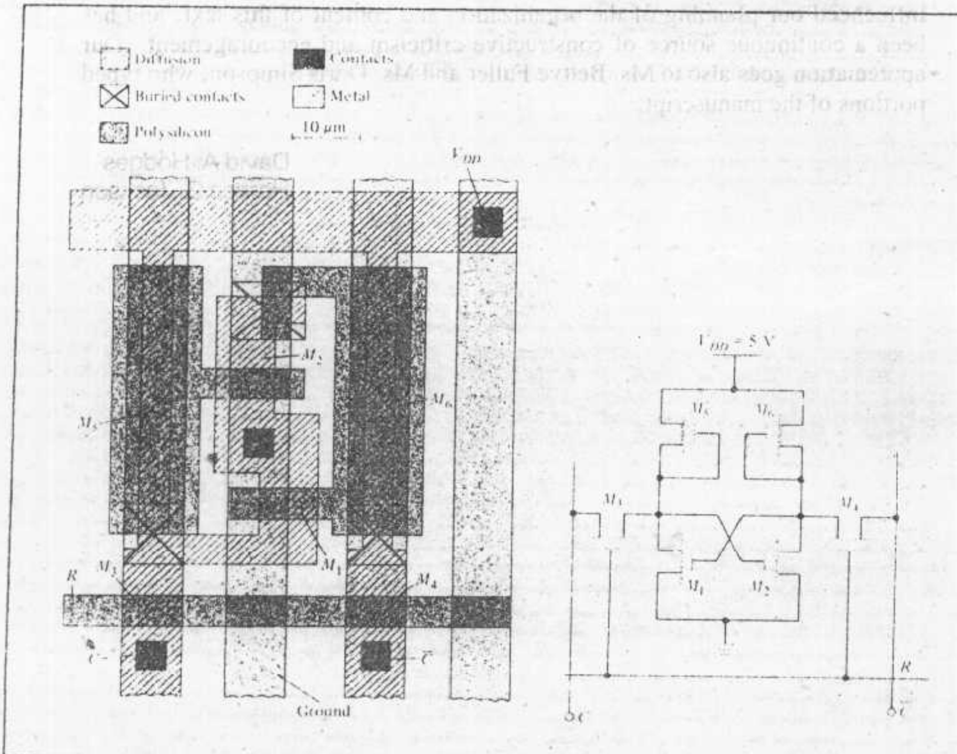

NMOS static RAM cell.

CONTENTS

*Denotes material which may be omitted without loss of continuity.

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INTRODUCTION TO DIGITAL ELECTRONICS 1

1.0 INTRODUCTION

The design of modern digital systems requires contributions from several engineering specialists. First, a *system designer*, or *system architect*, determines the desired characteristics for the final system and prepares a detailed specification that should define all inputs, outputs, environmental conditions, operating speeds, etc. A *logic designer* translates the system specification into a logic design that can meet the functional requirements. Some basic principles of logic design are briefly reviewed in Secs. 1.1 and 1.2.

The task of the *circuit engineer* is to design circuits that provide the required logic functions. The main subject for study in this book is digital circuit design. Whenever many copies of the desired system are to be manufactured, it is important to achieve high reliability of operation and a good balance among cost and performance characteristics. The chapters that follow address in depth the issues of electronic design that determine these characteristics. Hence in Secs. 1.4 and 1.5 we introduce some useful properties of digital circuits and characterize an ideal logic element. Some technical terms that describe the electrical performance of digital circuits are defined in Secs. 1.6 and 1.7.

Today, virtually all digital systems are based on integrated circuit technology. Various design options and trade-offs exist. Choices must be made of circuit family, level of integration (the number of circuits on a chip), and programmable versus fixed-function ("hard-wired") circuits.

The various integrated circuit technologies have widely differing characteristics. Integrated circuit *process and device engineers* continue to make improvements in these technologies. Some understanding of integrated circuit fabrication techniques is required to understand the relative characteristics of different circuit families, such as TTL, ECL, NMOS, and CMOS. An appreciation of the direction and rate of change in fabrication technology is important if product designs are to provide good possibilities for evolutionary improvements. Basic techniques for fabrication of integrated circuits are described briefly in Sec. 1.3, and the influence of fabrication technology on design is frequently mentioned in subsequent chapters.

Computer aids to design (CAD) are essential in analysis and design of digital integrated circuits. Section 1.8 presents a short introduction to this important subject, and describes the role these modern tools will have in our study of digital circuits. Manual analysis is used only for quick approximate calculations to compare different configurations.

Good system design requires that design decisions result in a good balance among system characteristics, logic design, circuit design, and fabrication technology. Since compromises must usually be made and alternatives evaluated, it is important that the various specialists mentioned above have some knowledge of the related fields.

1.1 LOGIC FUNCTIONS

In a digital system information is represented solely in discrete (or *quantized* or *digitized)* form. Most commonly a binary form is used, which means that only two discrete states are allowed, normally denoted as 0 and 1.

Logic design with binary quantities has some peculiarities, but it also presents some useful opportunities. For instance, the answer to a question can only be *yes* or *no*, it can never be *maybe*! A special algebra applicable to the binary system was invented by George Boole (1815–1864). This form of algebra can be useful to a logic and/or circuit designer, and some familiarity with it is essential in the analysis and design of digital integrated circuits.

The three basic operations performed with Boolean algebra are included in Table 1.1. The · symbol denotes the logic AND operation, although as the table shows, the · between the variables is usually omitted. The + symbol indicates a logic OR. A bar over the variable indicates the NOT operation, or logic inversion. That is, since only two states of the variable are permitted, if $A = 0$ then $\overline{A} = 1$.

TABLE 1.1

BASIC BOOLEAN OPERATIONS

Operation	Boolean expression
AND	$F = A \cdot B = AB$
OR	$F = A + B$
NOT	$F = \overline{A}$
NAND	$F = \overline{A \cdot B} = \overline{AB}$
NOR	$F = \overline{A + B}$

Consider first the AND function of the two binary variables A and B. Shown in Fig. 1.1*a* are two ways of expressing the AND function. A *truth table* is simply a systematic listing of the values of the dependent variable (F) in terms of all the possible values of the independent variables (A and B). Since we are working with a binary system there are 2^N combinations, where N

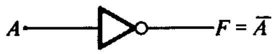
A	B	F
0	0	0
0	1	0
1	0	0
1	1	1

(*a*)

A	B	F
0	0	0
0	1	1
1	0	1
1	1	1

(*b*)

A	F
0	1
1	0



(*c*)

Figure 1.1 Truth table and standard symbol for the three basic logic operations. (*a*) AND function, $F = AB$. (*b*) OR function, $F = A + B$. (*c*) NOT function, $F = \overline{A}$.

is the number of independent variables being considered. Note that the AND statement is true (=1) only if $A = 1$ *and* $B = 1$. The standard logic symbol for a 2-input AND gate is also illustrated in Fig. 1.1*a*. The requirement here is that both the inputs (A and B) be at a 1 for the output (F) to be at a 1.

The OR function, more properly designated the inclusive-OR function, is illustrated in Fig. 1.1*b*. Notice from the truth table that the OR statement is true if *either* $A = 1$ *or* $B = 1$, but in addition to the either/or condition, there is an *or both* condition. It is this *or both* condition that leads to the name inclusive-OR. Also shown in Fig. 1.1*b* is the standard logic symbol for a 2-input inclusive-OR gate.

The truth table and logic symbol of the NOT function is illustrated in Fig. 1.1*c*. The small circle at the output of the symbol indicates logic inversion.

From these three basic logic operations, two other common logic functions may be derived. The inverter can be combined with the AND gate to form the NOT-AND, or NAND, function, illustrated in Fig. 1.2*a*. The inverter may also be combined with the OR gate to form the NOT-OR, or NOR, function, shown in Fig. 1.2*b*.

Two other useful logic functions are illustrated in Fig. 1.3. The exclusive-OR function excludes the *or both* condition of the inclusive-OR. Note from the truth table that the statement is true if either $A = 1$ or $B = 1$, but not with both at a 1. Combined with an inverter, the combination yields an exclusive-NOR function.

A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

A	B	F
0	0	1
0	1	0
1	0	0
1	1	0

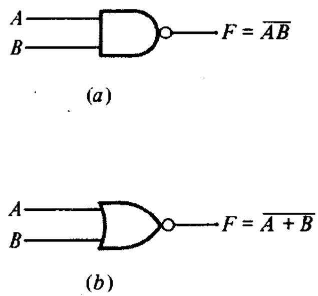


Figure 1.2 Truth table and standard logic symbol.
(*a*) NAND function, $F = \overline{AB}$. (*b*) NOR function, $F = \overline{A + B}$.

The basic logic functions have been described here with only two input variables. Gates with more than 2 inputs are also available, though in practice the limit is generally 4 or 8.

1.1.1 Boolean Identities

With the three basic operations (AND, OR, and NOT) it is possible to deduce a set of Boolean identities. These are listed in Table 1.2. These identities are useful in simplifying a complex logic expression for a clearer understanding of the logic to be performed. There may also be an economic benefit in the saving in silicon area when implementing the logic as an integrated circuit (IC).

TABLE 1.2

BOOLEAN IDENTITIES

1	$0 \cdot A = 0$	11	$A + B = B + A$
2	$0 + A = A$	12	$A(BC) = (AB)C$
3	$1 \cdot A = A$	13	$A + (B + C) = (A + B) + C$
4	$1 + A = 1$	14	$A(B + C) = AB + AC$
5	$A \cdot A = A$	15	$(A + B)(A + C) = A + BC$
6	$A + A = A$	16	$A + AB = A$
7	$A \cdot \bar{A} = 0$	17	$A + \bar{A}B = A + B$
8	$A + \bar{A} = 1$	18	$\overline{A + B} = \bar{A}\,\bar{B}$
9	$\bar{\bar{A}} = A$	19	$\overline{AB} = \bar{A} + \bar{B}$
10	$AB = BA$		

All the operations described in Table 1.2 may be proven with a truth table, but most of them are obvious. From the AND gate in Fig. 1.1 we see that with $B = 0$, always $F = 0$. Hence $0 \cdot A = 0$. From the OR gate in Fig. 1.1 we note that with $B = 0$, $F = A$, and $0 + A = A$ follows.

The last two identities in Table 1.2 are the DeMorgan theorems. These theorems are extremely useful in the reduction of complex Boolean expres-