1993 International Workshop On VLSI Process And Device Modeling

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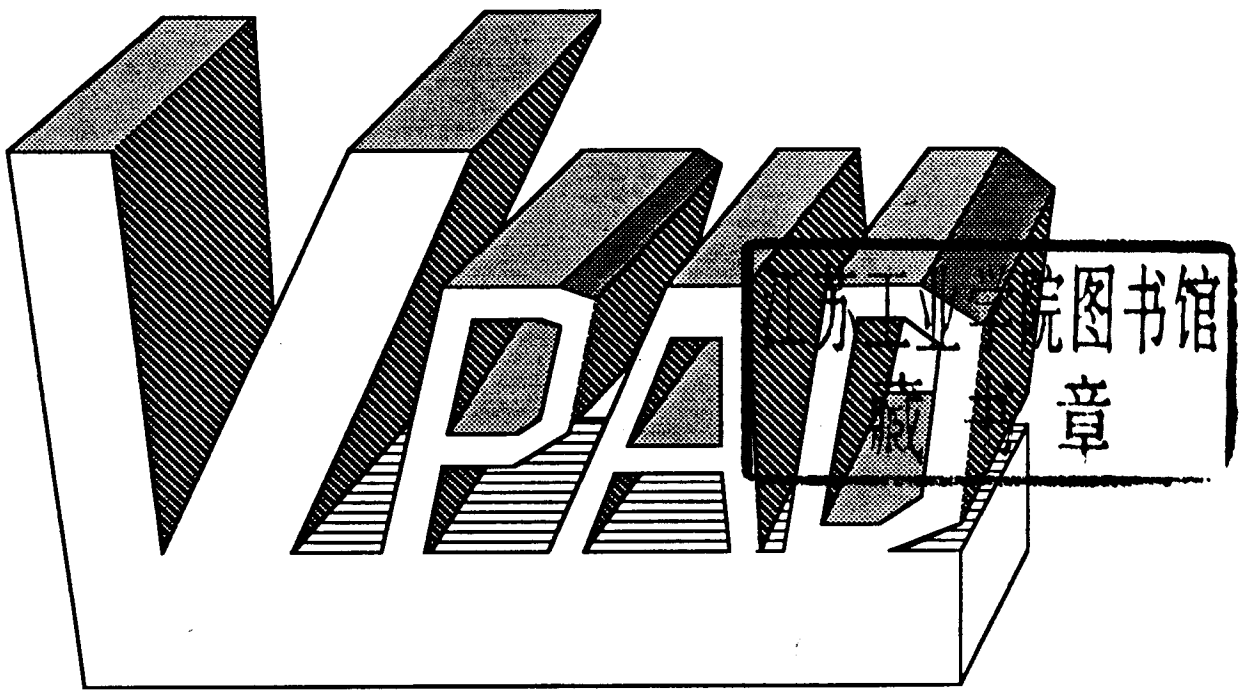
1993 International Workshop on VLSI Process and Device Modeling (1993 VPAD)

May 14 (Fri.) - May 15 (Sat.), 1993
Nara Ken - New Public Hall , Nara , Japan



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VPAD 93 Time Schedule

	Room A (Noh Theatre)	Room B (Conference Room 1&2)
May 14(Fri) 9:30- 9:40	Opening Remarks: T.Sugano & M.Fukuma	
9:40-10:40	Session A1 (Chairs: K.Asada & R.W.Dutton) 9:40-10:20 (A1-1) W.Fichtner (Plenary) 10:20-10:40 (A1-2) C.Werner (Invited)	
10:40-10:50	Break	
10:50-12:10	Session A2 (Chairs: W.Engl & K.Hane) Numerical Method and Parallel Computing 10:50-11:10 (A2-1) R.W.Dutton (Invited) 11:10-11:25 (A2-2) P.Conti 11:25-11:40 (A2-3) N.R.Aluru 11:40-11:55 (A2-4) A.Hiroki 11:55-12:10 (A2-5) E.Tomacruz	
12:10-13:40	Lunch	
13:40-16:45	Session A3 (Chairs: G.Baccarani & T.Toyabe) Device Simulation 13:40-14:00 (A3-1) M.R.Pinto (Invited) 14:00-14:15 (A3-2) A.Pierantoni 14:15-14:30 (A3-3) J.-G.Ahn 14:30-14:45 (A3-4) S.Ho 14:45-15:00 (A3-5) L.L.So 15:00-15:15 (A3-6) H.C.Read	Session B4 (Chairs:K.Taniguchi & R.W.Dutton) Process Simulation 13:40-14:00 (B4-1) S.T.Dunham (Invited) 14:00-14:15 (B4-2) N.E.B.Cowern 14:15-14:30 (B4-3) M.Hane 14:30-14:45 (B4-4) E.Strasser 14:45-15:00 (B4-5) E.W.Scheckler 15:00-15:15 (B4-6) F.A.Leon
	15:15-15:25 Break	15:15-15:25 Break
	15:25-15:45 (A3-7) U.Ravaioli (Invited) 15:45-16:00 (A3-8) T.Kunikiyo 16:00-16:15 (A3-9) C.-S.Yao 16:15-16:30 (A3-10) M.A.Stettler	15:25-15:45 (B4-7) H.Miura (Invited) 15:45-16:00 (B4-8) S.Matsuda 16:00-16:15 (B4-9) K.Kai 16:15-16:30 (B4-10) C.M.Li 16:30-16:45 (B4-11) T.-L.Tung
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17:00-18:30	Session A5 Rump Session (Moderators: N.E.B.Cowern & K.Nishi)	
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* Poster Preview & Poster Session

(P-1) J.Lorenz	(P-7) A.Schenk	(P-13) G.-H.Lee	(P-19) D.Yang	(P-25) J.H.Sim
(P-2) H.Sato	(P-8) Y.Tsuboi	(P-14) M.Ershov	(P-20) H.Stippel	(P-26) M.Miura-Mattausch
(P-3) T.Uchida	(P-9) K.Horio	(P-15) S.-W.Lee	(P-21) L.Colalongo	(P-27) W.T.Wongo
(P-4) S.Kuroda	(P-10) C.Fiegna	(P-16) N.Shigyo	(P-22) A.Kato	(P-28) H.Aoki
(P-5) D.Collard	(P-11) J.B.Kuo	(P-17) H.Brand	(P-23) S.Satoh	(P-29) J.-J.Yang
(P-6) R.H.Wang	(P-12) T.Iizuka	(P-18) K.Tanaka	(P-24) I.Kurachi	(P-30) R.Bauer
				(P-31) J.Poltz

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May 14, 1993

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T. Toyabe, Hitachi Ltd.

Session B4: Process Simulation <Room B>

Chairpersons: K. Taniguchi, Osaka Univ.
R.W. Dutton, Stanford Univ.

12:00-13:30 Lunch

Session BP8: Poster Session(13:30-15:00) **<Room B>**

Session A9: Circuit Model and Characterization <Room A>

Chairpersons: P.M. Lee, Hitachi Ltd.
D. Scharfetter, Intel Corp.

15:30-15:45 **Break**

Session A10: Carrier Transport for Device Simulation <Room A>

Chairpersons: J. Frey, Univ. of Maryland
M. Tomizawa, NTT Corp.

17:50-18:00 Closing Remarks: A. Yoshii, NTT <Room A>

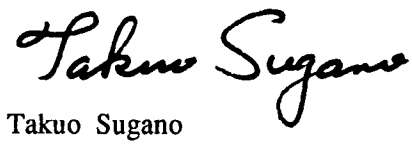
FOREWORD

The Conference Committee and I welcome you to the 1993 International Workshop on VLSI Process and Device Modeling(VPAD'93). This year the Workshop is held in Nara, an ancient capital and historic city of Japan.

The technical program of VPAD'93 attests to the fact that this Workshop is a leading forum for the presentation of the latest research and development in VLSI process and device modeling. The strong international nature of VPAD'93 is reflected in this year's exciting program which contains 78 technical papers, including 11 invited papers, and 67 papers selected from 100 submitted abstracts from 13 countries. They report on advances and achievements in Numerical Method and Parallel Computing, Device and Process Simulation, Carrier Transport for Device Simulation, and Circuit Model and Characterization. 27 and 25 papers to be presented originate from Japan and U.S.A., respectively and the remainder from Austria, Belgium, Canada, China, France, Germany, Italy, Korea, Netherlands, Russia, and Switzerland. The first technical session will feature *Professor W. Fichtner, Swiss Federal Institute of Technology,* who will deliver the keynote speech, and *Dr. C. Werner, Siemens AG,* who will discuss the state of the art and future challenges of equipment simulation.

The excellent program owes much to the dedicated efforts of the Technical Program Committee under the able leadership of the Program Chairman, *Professor Kunihiro Asada,* and the Program Cochairman, *Dr. K. Nishi.* I would very much like to appreciate all the members of the Conference Committee for various tasks to realize this Workshop, in particular, Workshop Committee Chairman, *Dr. M. Fukuma,* Cochairman, *Dr. N. Kotani,* Treasurer, *Dr. T. Toyabe,* Secretary, *Dr. H. Matsumoto,* Local Arrangement, *Dr. S. Odanaka,* and the Liaison Officers.

It is with great pleasure that I extend a hearty welcome to all of the speakers and the attendants of VPAD'93.



Takuo Sugano
Organizing Committee Chairman
1993 VLSI Process and
Device Modeling Workshop

From Layout to Circuit: Multi-Dimensional Process and Device Simulation – Current Status and Open Problems

W. Fichtner

Integrated Systems Laboratory, Swiss Federal Institute of Technology, Gloriastrasse 35, CH-8092 Zürich, Switzerland

Physical simulation of semiconductor processes and devices has become a widely accepted procedure in the development of new technologies and circuits, allowing more accurate prototype designs and time-efficient optimization cycles. Apart from its impact on the microelectronics industry, however, it has also established itself as an important field for academic and industrial research.

Over the past decades, simulation has undergone important developments on several fronts. While one-dimensional (1D) calculations dominated the early efforts in the 1960s and 1970s, two-dimensional (2D) investigations have become standard in the last decade for process and device analysis. Today, the simulation community is increasingly confronted with requests to optimize more complex merged 2D or even 3D structures. This enormous increase in simulation capabilities can be attributed to several factors such new numerical algorithms, improved physical understanding and more powerful computing platforms.

Looking at the simulation environment with a more critical eye, however, the positive remarks made above must be somewhat dampened in the light of reality. This is especially true is one would compare physical simulation to the more mature field of microelectronics CAD (i.e. IC design, simulation and test). The following paragraphs might illustrate this criticism. (In the following, let us assume a silicon "environment". Remarks much more critical must be made for III-V materials and devices).

To my knowledge, no complete system exists today that *really* allows an educated user to start at the layout and process flow level, to work upwards through process and device simulation and to end at the circuit level with a set of extracted parameters for CAD Models. Obviously, our dream system should be capable to handle more or less arbitrarily shaped devices of different dimensionality, it should contain all relevant physical models for process and device behavior, etc.

Looking in more detail, some answers can be given to explain this unsatisfactory state. While comprehensive 1D and 2D process simulators are available, these are essentially stand-alone tools requiring textual input. Apart from a few exceptions, transparent coupling to layout tools and process databases does not exist. 3D process simulators are only available for certain process steps. Interfacing process simulation results to device analysis has been solved only in one dimension. For complex 2D structures, major bottlenecks exist due to difficulties in structure recognition, mesh generation, and interpolation strategies.

On the device side, the situation is somewhat better, especially in 1D and 2D. The spectrum of available software ranges from simple drift-diffusion simulators to highly advanced software environments containing lattice and carrier heating or even Monte Carlo models. Even if the bottleneck of 3D structure generation and process simulation can be overcome, 3D device simulation restricts itself mainly to steady-state analysis due to the enormous CPU expenses involved. Nevertheless, the situation is not completely satisfactory. Most available software tools are restricted to only one level of dimensionality and cannot be embedded in a circuit environment.

Obviously, the shortcomings mentioned have been recognized for some time. Remedies are being studied and implemented in a variety a programs such as the US TCAD initiative and the European ESPRIT and JESSI projects. In the following, I would like to outline one possible attempt to attack several of the serious problems mentioned above. Over the past three years, we have been working on a "dream system" called *Ligament* jointly with several other groups. Figure 1 shows a flowchart of this system which today is fully operational in two dimensions. For complex 3D with nontrivial surface features (e.g. nonplanarities), crashes still occur on a regular basis due to structure generation problems (see below). Through the rest of this paper, examples from a

VLSI BiCMOS technology (18 masks) developed jointly by us and a major Swiss watch company will be used to illustrate salient points.

LIGAMENT combines the design representation of a technology (using design layout information) with a process representation to automatically generate 1D, 2D, and 3D structures to be transparently used in device simulation.

The three major inputs to the system are layout information (CIF files), a description of the process flow, and the electrical conditions for the device. The process flow is contained in a *semiconductor process representation* (SPR) which allows a detailed description of a complete fabrication sequence. Details can be found in [1].

DIOS process simulation [2] is performed automatically using simulation input generated from the supplied SPR and CIF descriptions of the device, employing sohisticated mesh adaption. For 2-D simulations, process simulation results can be directly used to generate a device grid [3]. As one representative example, Fig. 2 shows the doping profile for a vertically isolated BiCMOS pnp transistor. This structure was generated automatically from the layout and SPR information of the process (in nearly a CPU day on a Sparc 10). The final grid contains more than 100K triangles.

Looking at 3D structures, the nonavailability of 3D process simulation and the expense of obtaining multiple 2D cuts asks for a time efficient and pragmatic solution. For each unique combination of masks present on the layout, LIGAMENT performs a 1D simulation. The merged MOS-bipolar structure shown below required a total of 35 1D runs. When edge information is detected, 2D simulation is carried out (in this case a total of 11 2D simulations). These 2D simulations are restricted to small regions and CPU requirements are small. LIGAMENT splits simulation input decks with common initial stages into a tree to avaiod repetitive runs. The UNIX[1] programming facility make is used to ensure that simulation branches are executed correctly. Process simulation results are merged to form a 3D solid model using the ECHIDNA system[4]. Figure 3 shows the assembled "final" BiCMOS structure, that can be passed to the 3D grid generator OMEGA[5].

While a result like this is definitely encouraging, it was not obtained as elegantly as we are used to in 1D and 2D. Considerable difficulties remain to be solved, especially stability problems in underlying computational geometry algorithms.

Once grid and doping information is available, device simulation can be performed. We have developed a mixed-mode device and circuit simulator called SIMUL that allows to mix 1D, 2D and 3D devices [6]. By extending SIMUL to simulate more than one device as well as giving it access to the circuit simulator's functionalities it has been possible to combine both simulators' features into a single program (1D, 2D, 3D devices, extensive physical models for power devices, thermal-electric effects and all basic SPICE models). While other mixed-device and circuit simulators such as MEDUSA and CODECS have been presented, the originality of this work lies specifically in the possibility of a single code to simulate many devices of different dimensions together with the support of a full circuit simulator.

SIMUL was coded in the object-oriented language C++ allowing both fast prototyping and efficient execution. Our eperience with using a modern programming language has been extremely positive for many UNIX platforms ranging from Cray and NEC supercomputer to workstations.

The work reported here has been obtained through a joint effort by several people in the Integrated Systems Laboratory at ETHZ. Among others, I would like to mention K. Kells, J. Litsios and S. Müller (MESHBUILD and SIMUL), Nancy Hitschfeld (OMEGA), T. Feudel and N. Strecker (DIOS), A. Liegmann and C. Pommerell (linear solvers), C. Hegarty and P. Lamb LIGAMENT, and M. Westermann (PICASSO graphics system). Input (and criticism) is greatfully acknowledged from C. Lombardi (ST), G. Baccarani (Bologna), and P. von Staa (Bosch). This work was supported by the Swiss Lesit program, the Swiss National Science Foundation, and ESPRIT.

References

[1] C. Hegarty and W. Fichtner, "Semiconductor process representation," *IEEE Transactions on CAD*, vol. submitted, 1992.

[2] N. Strecker, "DIOS 3.0 user's guide," tech. rep., ETH Integrated Systems Laboratory, 1992.

[1] Unix is a trademark of AT&T Bell Laboratories