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1993 SYMPOSIUM ON VLSI TECHNOLOGY

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FOREWORD

WELCOME to KYOTO for the 1993 Symposium on VLSI Technology

With the impetus of an information-driven society continuing to press hard, VLSI keeps providing surges of innovation, for example, microprocessor chips running at clock rates above 100 MHz, and memory chips with a capacity of 256MB. Levels of integration have been increasing four fold every three years, and this often-quoted pace has not noticeably slowed down. Technology used in semiconductor products has become extremely complex, featuring line widths below half a micron and film thicknesses down to 5 nm. It involves an assortment of materials ranging from exotic dielectrics, new conductors and silicon of ever-improving quality, and comprises a wide variety of expensive chemical and physical processing tools. It is one thing to be at the leading edge of this highly specialized field of technology, and quite another to be able to put together and run an entire processing line for competitive products. These and other issues of advanced VLSI technology will be discussed in the informal atmosphere of this symposium.

This year, we have two distinguished speakers from the industry. Masahiko Ogirima of Hitachi will be addressing "Process Innovation for Future Semiconductor Industry," which is a matter of great concern to the industry. Specifically, he will discuss how much the feature size of semiconductor chips can be reduced while maintaining profitability, and what has to be done for that purpose. Craig Barrett of Intel will be discussing "Microprocessor Evolution and Technology Impact," the direction personal computer engines are being led to, and what that implies in terms of technology. This year 192 papers were submitted, of which 70 were accepted for presentation at the symposium. This resulted in an acceptance ratio of 36%. Selected papers have been carefully arranged into 18 stimulating sessions. Five topics of much current interest have been chosen for the evening rump sessions. All the credit for putting together this outstanding program goes to the program committee, cochaired by Masao Fukuma and Dick Chapman. Tadashi Nishimura and Rafael Reif have organized a workshop focused on the relevant issues of inspection and analysis, to be run on the Sunday preceding the symposium.

We greatly appreciate the efforts made by Eiji Takeda and Bill Siu, symposium secreatries, Katsutoshi Izumi and Ching-Te Chuang, publications/publicity, Taiji Ema and Youssef El-Mansy, treasurers, and last not but least, Nobuhiro Endo, Noboru Nomura and Wayne White, local arrangements.

This is the 13th meeting of this symposium, which has continued to serve as a discussion forum for engineers active in the area of Very Large-Scale Integrated circuits for all these years. We sincerely hope that this meeting will further build on this tradition, and that you will all have an enjoyable and rewarding time in Kyoto.

May 1993

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VLSI TECHNOLOGY WORKSHOP ON INSPECTION AND ANALYSIS TECHNOLOGIES FOR SCALED DOWN DEVICES

May 16, 1993

Organizers T. Nishimura *Mitsubishi Electric*
R. Reif *MIT*

SCHEDULE

TIME	TOPIC	SPEAKER
8:45	"State-of-the-art of Inspection and Analysis Technologies for Advanced VLSI Processing"	Steven A. Henck *Texas Instruments*
10:15	Coffee Break	
10:30	"Wet Cleaning Technology for High Integrity Gate Oxides"	Marc Heyns *IMEC*
12:00	Lunch	
13:15	"Detection and Analysis of Particles on Silicon Wafers"	Takeshi Hattori *Sony*
14:45	Coffee Break	
15:00	"Verification and Failure Analysis of the Device Chip"	Kiyoshi Nikawa *NEC*
16:30	Conclusion of Workshop	

Session 1 : Welcome and Plenary Session

Chairpersons:	M. Fukuma	NEC
	R. A. Chapman	Texas Instruments

Session 2 : Novel Characteristics of Hot Carrier Aging

Chairpersons:	E. Takeda	Hitachi
	J. Woo	UCLA

Session 3A: Next Generation DRAM Structures and Operation [Shunju I]

Chairpersons:	C.-G. Hwang	Samsung Electronics
	R. Reif	MIT

Session 3B: SOI and TFT [Shunju II]

Chairpersons:	M. Inuishi	Mitsubishi Electric
	E. Castel	National Semiconductor

Session 4A: Device Physics for Deep Submicron MOSFETs [Shunju I]

Chairpersons:	T. Kobayashi	NTT
	Y. Taur	IBM

Session 4B: Novel Dielectric Films [Shunju II]

Chairpersons:	E. Suzuki	Electrotechnical Lab.
	B. Siu	Intel

Session 5A: Non-Volatile Memory I [Shunju I]

Chairpersons:	S. Kimura	Hitachi
	K. Y. Chiu	Hewlett-Packard

Session 5B: Bipolar Technology I [Shunju II]

Chairpersons:	K. Terada	NEC
	A. Sinha	Applied Materials

Session 6A: Next Generation SRAM Structures and Operation [Shunju I]

Chairpersons:	J. Kudo	Sharp
	H. Muller	Siemens AG

Session 6B: Bipolar Technology II [Shunju II]

Chairpersons:	A. Kayanuma	Sony
	T. Alvarez	Cypress Semiconductor

Session 7A: Non-Volatile Memory II [Shunju I]

Chairpersons:	K. Yoshikawa	Toshiba
	J. R. Yeargain	Motorola

Session 7B: Sub 1/4 μm MOSFETs [Shunju II]

Chairpersons:	M. Kakumu	Toshiba
	B. Zetterlund	DEC

Session 8A: Process Technology for Deep Submicron MOSFETs [Shunju I]

Chairpersons:	S. Kawamura	Fujitsu
	W. White	Hughes Aircraft

Session 8B: Surface Preparation for Deep Submicron Devices [Shunju II]

Chairpersons:	R. Tsai	TSMC
	G. Declerck	IMEC

Session 9 : Advanced Interconnect Technology

Chairpersons:	K. Yoneda	Sanyo Electric
	R. Liu	AT&T Bell Labs.

Session 10: Manufacturing Science and Concurrent Engineering

Chairpersons:	H. Onoda	Oki Electric
	M. Moslehi	Texas Instruments

Session 11: Isolation for Deep Submicron and High Performance VLSIs

Chairpersons:	T. Shibata	Tohoku Univ.
	K. Saraswat	Stanford Univ.

Session 12: Advanced High Resolution Patterning

Chairpersons:	M. Sasago	Matsushita Electric
	J. R. Abernathey	IBM

CONTENTS

Session 4A: Device Physics for Deep Submicron MOSFETs [Shunju I]

Session 4B: Novel Dielectric Films [Shunju II]

Session 5A: Non-Volatile Memory I [Shunju I]

Session 5B: Bipolar Technology I [Shunju II]

Session 6A: Next Generation SRAM Structures and Operation [Shunju I]

Session 6B: Bipolar Technology II [Shunju II]

Session 7A: Non-Volatile Memory II [Shunju I]

Session 7B: Sub 1/4 μm MOSFETs [Shunju II]

Session 8A: Process Technology for Deep Submicron MOSFETs [Shunju I]

Session 8B: Surface Preparation for Deep Submicron Devices [Shunju II]

Rump Sessions

Session 9: Advanced Interconnect Technology

Session 10: Manufacturing Science and Concurrent Engineering

Session 11: Isolation for Deep Submicron and High Performance VLSIs

Session 12: Advanced High Resolution Patterning

1-2 (Invited)

Process Innovation for Future Semiconductor Industry

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Abstract

During the last few years, the semiconductor industry has been gradually deviating from its traditional course. This change seems to be due to the diversification of market needs and to technical difficulties. To break through to future technological generations, new device and process concepts must be introduced . This paper discusses several innovative processes for future developments in the semiconductor industry. It suggests that material innovation is important for simplifying device structure and lowering costs.

I. Introduction

Over the last two decades the semiconductor industry has made a remarkable progress supported by the development of semiconductor technologies. During this period, the integration of memory LSIs have increased by 4 times per generation and feature sizes have decreased by 0.7 times exactly followed a simple curve. But below ~1.0 μm feature sizes(1Mb- 4Mb DRAMs), the simple trend has gradually changed. This change indicates that the trend in chip price (constant, π -rule) has slowed down to a bi-rule. This might be the symptom of the slow-down in the progress of semiconductor technologies. So far, for the purpose of keeping this trend, many basic technologies have been investigated and many kinds of new technologies have been introduced for every generation.

In this sense, the new technologies introduced have been becoming more difficult generation by generation. Especially the technology transfer from research and development to production has been becoming more difficult because of the loss of margin.

On the other hand, needs from a system side have diversified and usual high integration-low cost alone can not keep up with the trend. These trends force the semiconductor industry to change its development strategy.

In the above context, this paper describes the expected innovations of process and material technologies which are necessary for future semiconductor industry. The selected items are

- Device trends
- Fine patterning technology
- Substrate engineering
- Simplified multi-level metallization
- Challenge to low-cost process

II .Device development trends and scaling strategies

The history of the development of LSI process technologies has been going along the same way as that of fine patterning technology. Fine patterning brings LSIs large integration and low-cost as well as high performance. Advanced process technologies which were developed for DRAM as a process driver have been applied step-by-step to many other devices such as microcomputers, ASICs and analog LSIs. But in the sub micron regime, the above trend has changed slightly. Finer patterning accompanies with process complexity, higher cost, and the slow down of bit cost improvement which used to go down to 1/4 every generation. Also large integration decreases flexibility of IC application and lowers the capability of response to the needs of market diversification. Beyond the 4Mb DRAMs generation, system needs cannot keep pace with technology development speed, which slows down the build-up of DRAM market. That is, the LSI market has been changing from a needs-driven one to a technology-driven one.

On the other hand, the system trend is heading towards " down-sizing" and " needs diversification" . The macro-trend of system needs for LSIs are

- Small size, value-added
- Low-voltage, low power-dissipation
- Large chip size/large integration
- High speed
- Low cost

Without a scaling effect, it is very difficult to satisfy these requirements, and in future, scaling will still be one of the most important problem for system LSIs.

User's requirements for the memories have become more diversified, such as byte-wide, synchronous high-speed DRAMs, flashEEPROMs and FRAMs, which need a variety of process and device technologies. In the sub-micron age, the prolonged DRAM generation (3~5years/generation) and difficulties with fine patterning have led to reconsideration of the traditional scaling factor (~ 0.65/generation). That is, the traditional generation of 3years has been divided into two or three steps, "step-by-step scaling". DRAMs of three or four generations coexist in a market at any time, and the original 4Mb DRAM (0.8 μm-rule) is scaled down stepwise to 0.7 μ m to 0.6 μ m and 0.5 μm.

At the last step, the older generation DRAM (4Mb) is produced using the newer generation (16Mb) technology (cut down version). This tendency is more conspicuous for logic LSI, and the progress of process technologies and design of logic LSI proceeds simultaneously-the age of concurrent engineering.

In the above background, close attention must be payed

for making development schedule of device and process technologies.

III .Macroscopic prospects of process technologies

Development scheme of process technology should be considered for long-term, middle-term, and short-term. In this paper, middle-and long-term prospects are mainly concerned.

In order to improve LSI performances, miniaturization is one of the most important technologies now and still in near future. However in the age of 16Mb DRAMs (0.5 μm), the limit of process technologies with scaling has been tangible gradually. Indeed, in a laboratory, devices with 0.1 μm rule are feasible, and 256Mb DRAM chips have been announced at conferences. Also, high-speed devices have shown remarkable progress such as silicon bipolar/CMOS devices of tpd<20ps.

But, because of the complexity of device structure, process margin is decreasing in the age of deep-sub micron, and yields are decreasing in the stage of mass production. For DRAMs from the generation of 1Mb, bit redundancy technology has been introduced, and as a result apparent yield of 4Mb is almost the same as 1Mb, though net yield obviously decreases, as indicated in Fig, 1. This tendency is thought to be due to the defect density and also to the decrease in process margin caused by the complexity of device structure and miniaturization.

Table 1, lists important problems in device and process technologies and feasible solutions. Improving the traditional technologies is not the best solution, and drastic changes in materials may be necessary. In the past, materials changes have included, such as Al-gate→ Si-gate, Al wiring →silicide(WSi_2/$MoSi_2$ etc.)→W, and SiO_2 → Si_3N_4. These materials breakthrough have uprooted the progress of the semiconductor industry. In the future, such materials innovations will be more and more important.

IV .Advanced Process technologies

4.1 Fine-Patterning Technology

As mentioned in Section I, the most important technology for improving LSI performance is still fine patterning. Although photolithography has been used for LSI production down to the 0.5 μm era, it is gradually becoming difficult to keep resolution as the pattern size approaches the wavelength of the ultraviolet light source. New technologies have been introduced every generation to improve resolution, and the life of photolithography has been repeatedly prolonged. For example, for 64Mb DRAMs (0.3-0.4 μm), new technologies such as phase-shift mask and off-axis exposure promise to keep fine resolution. Another approach is a new light source, and excimer lasers are considered to be most promising. There are three methods for raising the resolution of photo-lithography; shortening wavelength λ, increasing the numerical aperture (NA)of the lens, and improving process parameters as indicated Fig, 2. For lithography technology there is a trade-off between resolution and depth of focus (DOF), which is a very important factor. Therefore, fine patterning technology strongly depends on the other process technologies such as planarization.

Figure3 shows a feasible lithography scheme for 1Gb DRAMs(0.15 μm) taking all above improvements into consideration. Applying all these technologies to production will require improvements in other parameters such as alignment accuracy while maintaining process margins.

A cost analysis for these new technologies is also given in Fig, 3. This shows that fine patterning down to the 0.2 μm generation can be achieved using ultraviolet light, and beyond 0.2 μm new light sources such as electron beam and X-ray will be needed. The success or failure of X-ray lithography is thought to depend on the reduction optical system (reduction mirror) and strong X-ray source (Synchrotron Orbital Radiation).

Resist materials are also an important factor, and higher performance materials than the current chemical-amplification types are needed for quarter-micron lithography.

From the viewpoint of fine patterning, dry etching is very important as well as lithography. The problems of dry etching are

- Control of pattern size (~1/10 of minimum pattern size),
- Etching of new materials (high ϵ dielectrics, copper etc.),
- Sequential etching of multi-layered films,
- Selectivity,
- Etching rate uniformity of large diameter wafers.

So far, dry etching technologies are somewhat empirical and the plasma field cannot be completely controlled. More fundamental research and development of plasma physics are needed to solve the listed problems. The key factors of plasma physics are plasma density, ion energy, the issues in electric and magnetic fields, ion impinging angle, radical density and so on. The important point is how to control these parameters by reactor and system design.

4.2 Capacitor Technology.

In the deep-sub micron regime, the main problem in miniaturizing DRAMs is related to the capacitors. The capacitance required for 256Kb~1Mb DRAMs can be achieved with planar-type capacitor. For the 4Mb generation trench, STC, and fin-type capacitor cell have been proposed as listed in Fig, 4. The 64Mb DRAMs will require very complicated and sophisticated structures for the capacitor cells. All the proposed designs are three-dimensional and the difficulty and number of process-steps are close to limit. The complexity of the cell structure is due to the thin dielectric materials (SiO_2/Si_3N_4) which must be very reliable while having a low dielectric constant (ϵ).Breaking through the limit definitely requires some new dielectric (high ϵ) materials for capacitor cells.

The required capacitance of about 30fF for 256Mb DRAMs cannot be achieved using Ta_2O_5 for planar-like cell structures, and higher ϵ materials such as $SrTiO_3$ will be necessary. Usually the ϵ value of a thin film material is lower than that of the bulk material, and some margin of the ϵ value is needed for practical use.

Despite the intense R&D of the high ϵ materials for DRAM capacitors, many problems still remain unsolved for the film deposition process (CVD, sputtering), cell structure, stoichiometric control, and dielectric break-down, etc. Among these factors, break-down voltage (V)

is critical because of the relation, $\varepsilon \times V$=constant. It does not make sense to combine high ε materials with a trench/fin structure to solve cell complexity and cost problem. New dielectrics (ε >100) will be needed for the 256Mb generation .

4.3 Metallization Technology

Multi-layer metallization will be indispensable for system on-chip or high-speed design. Even now, 4-6 metal layers are used for high-speed bipolar LSI and CMOS/ASICs. The problems in multi-layer metallization are

- Planarization of the device (diffusion) layer and metallization layer,
- Refilling via-holes and contact-holes having high aspect ratios,
- New metallization materials (migration-immunity, easy-patterning, deposition process, adhesion properties),

Planalization is required for a DOF margin in lithography process, a dry-etch margin of metal layers and reduced capacitance between the metal layers. The projected future development for planarization is indicated schematically in Fig. 5. Device layers can be planarized by (B) PSG reflow and inter-metal layers by SOG film/CVD films with metal via-hole refilling. In this case, the problem is step difference between the memory area and logic area (absolute step-high) and also the space between metal wiring lines.

In general, planarization is easier for narrow lines/spaces than for wide ones, so some dummy patterns should be added for wide ones during the chip design. One advanced planarization technology that has been proposed is CMP (Chemical-Mechanical Polishing). This method is very simple and is thought to be effective for some devices, but might be unsuitable for conventional semiconductor process lines. It is effective for planarizing wide areas (global planarization) and refilling via-holes. It might also be effective for patterning some metal layer such as Cu or Au which are difficult to dry-etch.

Metallization of high aspect-ratio via-holes and contact holes was achieved by CVD-W refill (selective deposition or blanket/etching back) in the 0.5 μm age. New methods such as Al-reflow and collimated sputtering may improve step coverage.

The main problems with metallization materials are related to the guaranteed electro/stress migration immunity. Higher step coverage has been achieved using refractory metals (W/WSi_2, $MoSi_2$) which can be deposited by CVD. Good electromigration immunity has been achieved using TiW (TiN) or W/Al(Cu-Si)/TiW(TiN) or W multi-layered metallization for half-μm devices, but these metal wiring systems are not inherently suitable for electromigration. The limit of electromigraton immunity is estimated to be 1×10^6 A/cm^2, so finer metal patterns will need Cu or Au, which are hard to pattern by dry etching. In this case, new patterning technologies such as ion-milling or CMP may be necessary.

In any case, higher integration increases the burden on metallization technology, and it will become vital to simplify the metallization processes to reduce the cost of LSI chips. Basically, it is very important to planarize diffused layers and to process all the layers in the same manner and sequentially in the same equipment.

4.4 Substrate Technology

The quality of bulk silicon substrate has been improved in many ways such as flatness (LTV/TTV), periphery treatment, control of oxygen (carbon) content and defect density. The higher device performance needs the use of SOI substrates. SOS (silicon on sapphire) has not yet attained practical use because of crystalline defects. It needs greater effort to apply SOI (Silicon on Insulator) to the half-μm regime, in order to break through problems such as α -particle immunity and switching speed limit. Two methods proposed for making SOI are SIMOX and a bonded wafer. Both methods can form thin silicon layers less than 0.5 μm thick. Both have advantages and disadvantages related to film thickness uniformity, warpage, and wafer cost. SIMOX substrates suffer from heavy-metal contamination and crystalline defects.

Although devices fabricated on SOI substrates have some problems with hot-carrier immunity, source/drain break-down voltage, and heat diffusion, device performances have greatly improved;

- reduced α-particle noise
- improved switching speed (especially at low-voltage operation),
- less process steps.

Besides SOI, high-energy ion implantation might be applied to conventional process technology to reduce the cost of devices.

4.5 Reduction of Process Cost

One of the most serious problems for continuous growth of semiconductor industries is cost. To take DRAM as an example, it is well known that the bit cost of DRAMs (and SRAMs) has been reduced to 1/4 every generation, known as the π -rule, has shifted to bi-rule recently. There are many factors in costs, (1)chip area ($\times$1.4/generation), (2)process steps ($\times$1.3/generation.), (3)equipment cost/throughput, (4)development cost ($\times$1.5/generation.), (5)yield, etc. So far, the increase in chip area has been compensated for by an increase in wafer diameter. The other factors are not dependent on wafer diameter and must be recovered by other measures.

The investment for process equipment has increased by 1.8～2 times every generation and is expected to be one billion dollars to produce two million 64Mb chips per month excluding the clean rooms. (Fig. 6) The development of complex and large-scale chips takes a huge amount of human resources and facilities. Even one breakthrough requires investigating numerous possibilities.

Net probe yields have steadily declined since 1Mb DRAM generation, although gross yields have kept almost constant due to the use of redundancy circuits. (Fig. 1) This is the warning that semiconductor process technologies have entered danger zone. For the deep sub-μm generation to be possible the yield problem must be solved especially for logic devices. The two major causes of low yield are reduced process margin and contamination including particles.

Measures devised to deal with above-mentioned five factors of rising costs are listed in Table 2. Among these, ultra-clean technology for better yield and cheaper process equipment must be reconsidered from scratch. Especially, reducing the particle contamination in process equipment and controlling surface contamination directly