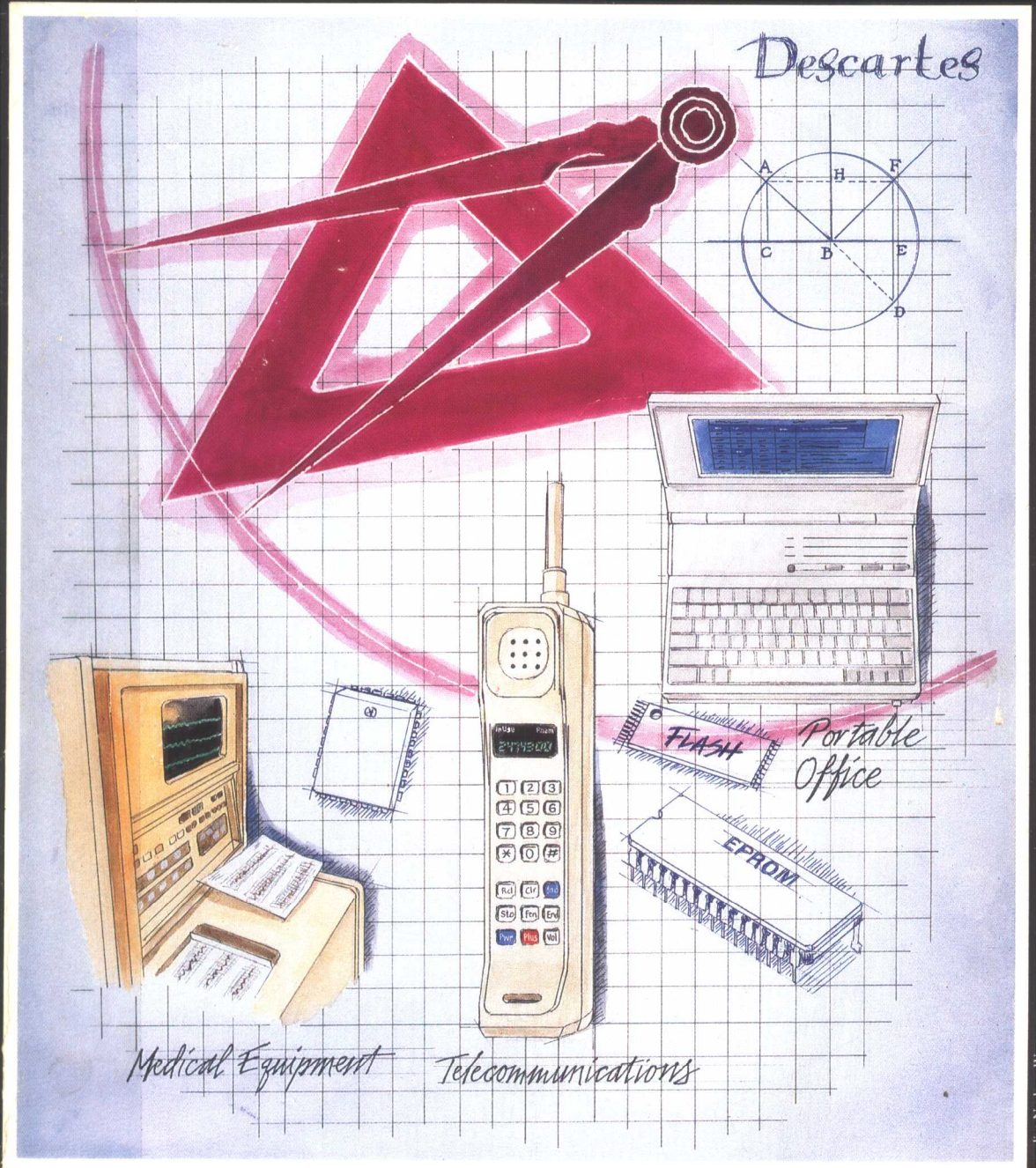
Memory Products



Benedict Norbert Wong

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MEMORY PRODUCTS

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Table of Contents

Alphanumeric Index xi

CHAPTER 1

Memory Overview

Memory Overview 1-1

CHAPTER 2

Memory Technologies

Intel Memory Technologies 2-1

CHAPTER 3

Dynamic RAMs (Random Access Memories)

DATA SHEETS

21256 262,144 x 1-Bit Dynamic RAM with Page Mode 3-1
21464 65,536 x 4-Bit Dynamic RAM with Page Mode 3-19
21010 1,048,576 x 1-Bit Dynamic RAM with Page Mode 3-37
21014 262,144 x 4-Bit Dynamic RAM with Page Mode 3-53
21040 4,194,304 x 1-Bit Dynamic RAM with Page Mode 3-69
2D2569 256K x 9-Bit High Density Dynamic RAM Memory Module with Page Mode 3-90
21019 1,048,576 x 9-Bit Dynamic RAM Memory Module with Page Mode 3-107
225636 256K x 36-Bit Dynamic RAM Memory Module with Page Mode 3-124
251236 512K x 36-Bit Dynamic RAM Memory Module with Page Mode 3-141

RELIABILITY REPORT

RR-62 Dynamic RAM Reliability Report 3-158

CHAPTER 4

Static RAMs (Random Access Memories)

DATA SHEETS

5116S/L 2K x 8-Bit CMOS Static RAM 4-1
5164S/L 8K x 8-Bit CMOS Static RAM 4-9
51256S/L 32K x 8-Bit CMOS Static RAM 4-18
51C68 High Speed CHMOS 4096 x 4-Bit Static RAM 4-26
51C98 High Speed CHMOS 16,384 x 4-Bit Static RAM 4-32
5164 High Speed 8192 x 8-Bit Static RAM 4-39
51256 High Speed 32K x 8-Bit Static RAM 4-47
51258 High Speed 64K x 4-Bit Static RAM 4-56

RELIABILITY REPORT

RR-63 Static RAM Reliability Report 4-63

CHAPTER 5

EPROMs (Erasable Programmable Read Only Memories)

DATA SHEETS

2716 16K (2K x 8) UV Erasable PROM 5-1
2732A 32K (4K x 8) UV Erasable PROMs 5-9
2764A 64K (8K x 8) UV Erasable PROMs 5-18
27128A 128K (16K x 8) Production and UV Erasable PROMs 5-28
27256 256K (32K x 8) Production and UV Erasable PROMs 5-38
27C256 256K (32K x 8) CHMOS EPROM 5-50
27C512 512K (64K x 8) CHMOS EPROM 5-62
27513 Page-Addressed 512K (4 x 16K x 8) UV Erasable PROM 5-72
27C513 Page-Addressed 512K (4 x 16K x 8) UV Erasable PROM 5-85
27C011 Page-Addressed 1M (8 x 16K x 8) EPROM 5-100
27C010 1M (128K x 8) CHMOS EPROM 5-113
27C100 1M (128K x 8) CHMOS EPROM 5-124
27C020 2M (256K x 8) CHMOS EPROM 5-134
27C040 4M (512K x 8) CHMOS EPROM 5-144

Table of Contents (Continued)

27C210 1M (64K x 16) CHMOS EPROM 5-154
27C220 2M (128K x 16) CHMOS EPROM 5-164
27C240 4M (256K x 16) CHMOS EPROM 5-173
27C400 4M (256K x 16 or 512K x 8) CHMOS EPROM 5-182
27960CX Pipelined Burst Access 1M (128K x 8) CHMOS EPROM 5-192
27960KX Burst Access 1M (128K x 8) CHMOS EPROM 5-213
APPLICATION NOTES
AP-329 68030/27960CX Burst EPROM Interface 5-232
AP-346 29000/27960CX Burst EPROM Interface 5-260
RELIABILITY REPORTS
RR-35 EPROM Reliability Data Summary 5-287
RR-67 EPROM Reliability Data Summary CHMOS III-E 5-341
ARTICLE REPRINTS
AR-414 Marriage of CMOS and PLCC Sparking Rapid Change in Mounting Memories 5-390
AR-455 One Time Programmable EPROMs 5-392
AR-458 OTP EPROMs with Quick-Pulse Programming Offer Ideal Mass Production Firmware Storage 5-395
AR-468 Keeping Data Safe with Nonvolatile Memory 5-398

CHAPTER 6
Flash Memories (Electrically Erasable and Reprogrammable Non-Volatile Memories)
Flash: A New Way to Deal with Memory 6-1
DATA SHEETS
28F256A 256K (32K x 8) CMOS Flash Memory 6-5
28F512 512K (64K x 8) CMOS Flash Memory 6-30
28F010 1024K (128K x 8) CMOS Flash Memory 6-55
28F020 2048K (256K x 8) CMOS Flash Memory 6-81
iSM001 FLKA 1 Mbyte (512K x 16) CMOS Flash SIMM 6-109
iMC001FLKA 1-Megabyte Flash Memory Card 6-143
iMC004FLKA 4-Megabyte Flash Memory Card 6-173
APPLICATION NOTES
AP-316 Using Flash Memory for In-System Reprogrammable Nonvolatile Storage 6-203
AP-341 Designing An Updatable BIOS Using Flash Memory 6-248
AP-343 Solutions for High Density Applications Using Intel Flash Memory 6-297
APPLICATION BRIEF
AB-25 Designing in Flexibility with a Universal Memory Site 6-365
ENGINEERING REPORTS
ER-20 ETOX II Flash Memory Technology 6-371
ER-24 The Intel 28F010 Flash Memory 6-376
ARTICLE REPRINTS
AR-463 Don't Write Off the U.S. in Memory Chips 6-390
AR-466 Nonvolatility: Semi vs. Mag 6-393
AR-470 A 90 ns 100K Erase/Program Cycle Megabit Flash Memory 6-395
AR-472 The Memory Driver 6-399
AR-474 Memory Life-Cycle Cost 6-400
AR-478 Flash, Best of Two Worlds 6-401
AR-484 PC Standard in the Cards 6-406
AR-486 Flash Outshines ROM & EPROM 6-411
AR-490 Flash Memory Operates 10–20 Times Longer 6-417
AR-491 Memory Breakthrough Drives Miniaturization 6-419

Alphanumeric Index

21010 1,048,576 x 1-Bit Dynamic RAM with Page Mode 3-37
21014 262,144 x 4-Bit Dynamic RAM with Page Mode 3-53
21019 1,048,576 x 9-Bit Dynamic RAM Memory Module with Page Mode 3-107
21040 4,194,304 x 1-Bit Dynamic RAM with Page Mode 3-69
21256 262,144 x 1-Bit Dynamic RAM with Page Mode 3-1
21464 65,536 x 4-Bit Dynamic RAM with Page Mode 3-19
225636 256K x 36-Bit Dynamic RAM Memory Module with Page Mode 3-124
251236 512K x 36-Bit Dynamic RAM Memory Module with Page Mode 3-141
27128A 128K (16K x 8) Production and UV Erasable PROMs 5-28
2716 16K (2K x 8) UV Erasable PROM 5-1
27256 256K (32K x 8) Production and UV Erasable PROMs 5-38
2732A 32K (4K x 8) UV Erasable PROMs 5-9
27513 Page-Addressed 512K (4 x 16K x 8) UV Erasable PROM 5-72
2764A 64K (8K x 8) UV Erasable PROMs 5-18
27960CX Pipelined Burst Access 1M (128K x 8) CHMOS EPROM 5-192
27960KX Burst Access 1M (128K x 8) CHMOS EPROM 5-213
27C010 1M (128K x 8) CHMOS EPROM 5-113
27C011 Page-Addressed 1M (8 x 16K x 8) EPROM 5-100
27C020 2M (256K x 8) CHMOS EPROM 5-134
27C040 4M (512K x 8) CHMOS EPROM 5-144
27C100 1M (128K x 8) CHMOS EPROM 5-124
27C210 1M (64K x 16) CHMOS EPROM 5-154
27C220 2M (128K x 16) CHMOS EPROM 5-164
27C240 4M (256K x 16) CHMOS EPROM 5-173
27C256 256K (32K x 8) CHMOS EPROM 5-50
27C400 4M (256K x 16 or 512K x 8) CHMOS EPROM 5-182
27C512 512K (64K x 8) CHMOS EPROM 5-62
27C513 Page-Addressed 512K (4 x 16K x 8) UV Erasable PROM 5-85
28F010 1024K (128K x 8) CMOS Flash Memory 6-55
28F020 2048K (256K x 8) CMOS Flash Memory 6-81
28F256A 256K (32K x 8) CMOS Flash Memory 6-5
28F512 512K (64K x 8) CMOS Flash Memory 6-30
2D2569 256K x 9-Bit High Density Dynamic RAM Memory Module with Page Mode 3-90
5116S/L 2K x 8-Bit CMOS Static RAM 4-1
51256 High Speed 32K x 8-Bit Static RAM 4-47
51256S/L 32K x 8-Bit CMOS Static RAM 4-18
51258 High Speed 64K x 4-Bit Static RAM 4-56
5164 High Speed 8192 x 8-Bit Static RAM 4-39
5164S/L 8K x 8-Bit CMOS Static RAM 4-9
51C68 High Speed CHMOS 4096 x 4-Bit Static RAM 4-26
51C98 High Speed CHMOS 16,384 x 4-Bit Static RAM 4-32
AB-25 Designing in Flexibility with a Universal Memory Site 6-365
AP-316 Using Flash Memory for In-System Reprogrammable Nonvolatile Storage 6-203
AP-329 68030/27960CX Burst EPROM Interface 5-232
AP-341 Designing An Updatable BIOS Using Flash Memory 6-248
AP-343 Solutions for High Density Applications Using Intel Flash Memory 6-297
AP-346 29000/27960CX Burst EPROM Interface 5-260
AR-414 Marriage of CMOS and PLCC Sparking Rapid Change in Mounting Memories 5-390
AR-455 One Time Programmable EPROMs 5-392
AR-458 OTP EPROMs with Quick-Pulse Programming Offer Ideal Mass Production Firmware Storage 5-395
AR-463 Don't Write Off the U.S. in Memory Chips 6-390
AR-466 Nonvolatility: Semi vs. Mag 6-393
AR-468 Keeping Data Safe with Nonvolatile Memory 5-398

Alphanumeric Index (Continued)

AR-470 A 90 ns 100K Erase/Program Cycle Megabit Flash Memory 6-395
AR-472 The Memory Driver 6-399
AR-474 Memory Life-Cycle Cost 6-400
AR-478 Flash, Best of Two Worlds 6-401
AR-484 PC Standard in the Cards 6-406
AR-486 Flash Outshines ROM & EPROM 6-411
AR-490 Flash Memory Operates 10–20 Times Longer 6-417
AR-491 Memory Breakthrough Drives Miniaturization 6-419
ER-20 ETOX II Flash Memory Technology 6-371
ER-24 The Intel 28F010 Flash Memory 6-376
Flash: A New Way to Deal with Memory 6-1
iMC001FLKA 1-Megabyte Flash Memory Card 6-143
iMC004FLKA 4-Megabyte Flash Memory Card 6-173
Intel Memory Technologies 2-1
iSM001 FLKA 1 Mbyte (512K x 16) CMOS Flash SIMM 6-109
Memory Overview 1-1
RR-35 EPROM Reliability Data Summary 5-287
RR-62 Dynamic RAM Reliability Report 3-158
RR-63 Static RAM Reliability Report 4-63
RR-67 EPROM Reliability Data Summary CHMOS III-E 5-341

MEMORY BACKGROUND AND DEVELOPMENT

Years ago, MOS LSI memories were little more than laboratory curiosities. Any engineer brave enough to design with semiconductor memories had a simple choice of which memory type to use. The 2102 Static RAM for ease of use or the 1103 Dynamic RAM for low power were the only two devices available. Since then, the memory market has come a long way, the types of memory devices have proliferated, and more than 3,000 different memory devices are now available. Consequently, the designer has many to choose from but the choice is more difficult, and therefore, effective memory selection is based on matching memory characteristics to the application.

Memory devices can be divided into two main categories: volatile and nonvolatile. Volatile memories retain their data only as long as power is applied. In a great many applications this limitation presents no problem. The generic term random access memory (RAM) has come to be almost synonymous with a volatile memory in which there is a constant rewriting of stored data.

Nonvolatile memories retain their data whether or not power is applied. In some situations it is critical that a nonvolatile device be used. An example of this requirement would be retaining data during a power failure. (Tape and disk storage are also non-volatile memories but are not included within the scope of this book, which confines itself to solid-state technologies in IC form.)

Thus, when considering memory devices, it's helpful to see how the memory in computer systems is segmented by applications and then look at the state-of-the-art in these cases.

Volatile Read/Write Memory

First examine read/write memory, which permits the access of stored memory (reading) and the ability to alter the stored data (writing).

Before the advent of solid-state read/write memory, active data (data being processed) was stored and retrieved from nonvolatile core memory (a magnetic-storage technology). Solid-state RAMs solved the size and power consumption problems associated with core, but added the element of volatility. Because RAMS lose their memory when you turn off their power, you must leave systems on all the time, add battery backup or store important data on a nonvolatile medium before the power goes down.

Despite their volatility, RAMs have become very popular, and an industry was born that primarily fed computer systems' insatiable appetites for higher bit capacities and faster access speeds.

RAM Types

Two basic RAM types have evolved since 1970. Dynamic RAMs are noted for high capacity, moderate speeds and low power consumption. Their memory cells are basically charge-storage capacitors with driver transistors. The presence or absence of charge in a capacitor is interpreted by the RAM's sense line as a logical 1 or 0. Because of the charge's natural tendency to distribute itself into a lower energy-state configuration, however, dynamic RAMs require periodic charge refreshing to maintain data storage.

Traditionally, this requirement has meant that system designers had to implement added circuitry to handle the dynamic RAM subsystem refresh. And at certain times, when refresh procedures made the RAM unavailable for writing and reading; the memory's control circuitry had to arbitrate access. LSI dynamic memory controllers reduce the refresh requirement to a minimal design by offering a monolithic controller solution.

Where users are less concerned with space and cost than with speed and reduced complexity, the second RAM type—static RAMs—generally prove best. Unlike their dynamic counterparts, static RAMs store ones and zeros using traditional flip-flop logic-gate configurations. They are faster and require no refresh. A user simply addresses the static RAM, and after a very brief delay, obtains the bit stored in that location. Static devices are also simpler to design with than dynamic RAMs, but the static cell's complexity puts these volatile chips far behind dynamics in bit capacity per square mil of silicon.

Nonvolatile Read-Only Memory

Another memory class, read-only memory (ROM), is similar to RAM in that a computer addresses it and then retrieves data stored at that address. However, ROM includes no mechanism for altering the data stored at that address—hence, the term read only.

ROM is basically used for storing information that isn't subject to change—at least not frequently. Unlike RAM, when system power goes down, ROM retains its contents.

ROM devices became very popular with the advent of microprocessors. Most early microprocessor applications were dedicated systems; the system's program was fixed and stored in ROM. Manipulated data could vary and was therefore stored in RAM. This application split caused ROM to be commonly called program storage, and RAM, data storage.

The first ROMs contained cell arrays in which the sequence of ones and zeros was established by a metallization interconnect mask step during fabrication. Thus, users had to supply a ROM vendor with an interconnect program so the vendor could complete the mask and build the ROMs. Set-up charges were quite high—in fact, even prohibitive unless users planned for large volumes of the same ROM.

To offset this high set-up charge, manufacturers developed a user-programmable ROM (or PROM). The first such devices used fusible links that could be melted or programmed with a special hardware system.

Once programmed, a PROM was just like a ROM. If the program was faulty, the chip had to be discarded. But, PROMs furnished a more cost-effective way to develop program memory or firmware for low-volume purposes than did ROMs.

As one alternative to fusable-link programming, Intel pioneered an erasable MOS-technology PROM (termed an EPROM) that used charge-storage programming. It came in a standard ceramic DIP package but had a window that permitted die exposure to light. When the chip was exposed to ultraviolet light, high energy photons could collide with the EPROM's electrons and scatter them at random, thus erasing the memory.

The EPROM was not intended for use in read/write applications, but it proved very useful in research and development for prototypes, where the need to alter the program several times is quite common. Indeed, the EPROM market originally consisted almost exclusively of development labs. As the fabrication process became mature, and volumes increased, EPROM's lower prices made them attractive even for medium-volume production-system applications. Today, millions of EPROMs are used in systems which require only periodic, off-line updates of information and parameters.

Nonvolatile Read/Write Memory

Technology advances have blurred the traditional lines drawn between read-only memories (ROMs) and read/write memories (RAMs). The first alternative was the EPROM, which required removal from the host system, placing it under ultraviolet light for erasure, and subsequent reprogramming and reinstallation into the host system.

The next advancement was the introduction of a nonvolatile memory that was electrically erasable and user rewritable on a byte-by-byte basis, called the EEPROM. The byte erase capability and high-level of feature integration of the EEPROM came with two penalties—density and cost. Cell and periphery complexity places EEPROM far behind EPROM or DRAM in bit capacity per square millimeter of silicon and the resulting lack of cost-effectiveness and density has caused it to lag behind other memory technologies.

The latest advancement is Flash memory. Flash memories combine the electrical erase capability of the EEPROM with the simplicity, density and cost-effectiveness of EPROM cell layout. Modification to the EPROM cell replaces block UV-erasure with block electrical erasure, which can be accomplished while the device is still installed in the host system. Flash memory can also be randomly read or written by the local system microprocessor or microcontroller.

The cost effectiveness and flexibility of Flash memory makes it applicable in code storage applications. Code can be quickly and easily updated during prototyping, incoming test, assembly or in the field, quickly and easily. High density and nonvolatile read/write capability also make Flash memory an innovative alternative for mass storage, and integrating main memory and backup storage functions into directly executable Flash memory boosts system performance, shrinks system size, reduces power requirements and increases reliability over that of electromechanical media, especially in extreme environmental conditions.

APPLICATIONS OF MEMORY DEVICES

Besides the particular characteristics of each device that has been discussed, there are a number of other factors to consider when choosing a memory product, such as cost, power consumption, performance, memory architecture and organization, and size of the memory. Each of these factors plays an important role in the final selection process.

Performance

Generally, the term performance relates to how fast the device can operate in a given system environment. This parameter is usually rated in terms of the access time. Fast SRAMs can provide access times as fast as 20 ns, while the fastest DRAM cannot go much beyond the 100 ns mark. A bipolar PROM has an access time of 35 ns. RAM and PROM access is usually controlled by a signal most often referred to as Chip Select ($\overline{CS}$). $\overline{CS}$ often appears in device specifications. In discussing access times, it is important to remember that in SRAMs and PROMs, the access time equals the cycle time of the system whereas in DRAMs, the access time is always less than the cycle time.

Cost

There are many ramifications to consider when evaluating cost. Often the cost of the physical device used is the smallest portion of the total cost of using a particular device. Total cost must comprehend other factors such as design-in time, test expense, update costs, as well as cost per bit, size of memory power consumption, etc.

Cost of design time is proportional to design complexity. For example, SRAMs generally require less design-in time than DRAMs because there is no refresh circuitry to consider. Conversely, the DRAM provides the lowest cost per bit because of its higher packing density. The cost of a service call to exchange or reprogram a ROM/PROM/EPROM versus an in-system update of a Flash memory costs orders of magnitude more than the device itself.

Memory Size

Memory size is generally specified in the number of bytes (a byte is a group of eight bits). The memory size of a system is usually segmented depending upon the general equipment category. Computer mainframes and most of today's minicomputers use blocks of read/write substantially beyond 64K bytes—usually in the hundreds of thousands to millions of bytes.

The microprocessor user generally requires memory sizes ranging from 2K bytes up to 64K bytes. In memories of this size, the universal site concept allows maximum flexibility in memory design.

Power Consumption

Power consumption is important because the total power required for a system directly affects overall cost. Higher power consumption requires bigger power supplies, more cooling, and reduced device density per board—all affecting cost and reliability. All things considered, the usual goal is to minimize power. Many memories now provide automatic power-down. With today's emphasis on saving energy and reducing cost, the memories that provide these features will gain an increasingly larger share of the market.

In some applications, extremely low power consumption is required, such as battery operation. For these applications, the use of devices made by the CMOS technology have a distinct advantage over the NMOS products. CMOS devices offer power savings of several magnitudes over NMOS. Non-volatile devices such as EPROMs or Flash memories are usually independent of power problems in these applications.

Power consumption also depends upon the organization of the device in the system. Organization usually refers to the width of the memory word. At the time of their inception, memory devices were organized as nK x 1 bits. Today, they are available in various configurations such as 4K x 1, 16K x 1, 64K x 1, 1K x 4, 2K x 8, etc. As the device width increases, fewer devices are required to configure a given memory word—although the total number of bits remains constant. The wider organization can provide significant savings in power consumption, because a fewer number of devices are required to be powered up for access to a given memory word. In addition, the board layout design is simpler due to fewer traces and better layout advantages. The wider width is of particular advantage in microprocessors and bit-slice processors because most microprocessors are organized in 8-bit or 16-bit architectures. A memory chip configured in the nK x 8 organization can confer a definite advantage—especially in universal site applications. Conversely, there is usually a small speed penalty, at the device level for a x8 or x16 organization.

Types of Memories

The first step to narrowing down your choice is to determine the type of memory you are designing—data store or program store. After this has been done, the next step is to prioritize the following factors:

Performance
Power Consumption
Density
Cost

SUMMARY

Global Memory

Generally, a global memory is greater than 64K bytes and serves as a main memory for a microprocessor system. Here, the use of dynamic RAMs or Flash memory for read/write memory is dictated to provide the highest density and lowest cost per bit. The cost of providing refresh circuitry for the dynamic RAMs is spread over a large number of memory bits, thus minimizing the cost impact.

Local Memory

Local memories are usually less than 64K bytes and reside in the proximity of the processor itself—usually on the same PC board. Types of memories often used in local memory applications are SRAM, EPROM, Flash memory, and EEPROM.

Memory Technologies 2

INTEL MEMORY TECHNOLOGIES

Most of this handbook is devoted to techniques and information to help you design and implement semiconductor memory in your application or system. In this section, however, the memory chip itself will be examined and the processing technology required to turn a bare slice of silicon into high performance memory devices is described. The discussion has been limited to the basics of MOS (Metal Oxide Semiconductor) technologies as they are responsible for the majority of memory devices manufactured at Intel.

There are three major MOS technology families—PMOS, NMOS, and CMOS (Figure 1). They refer to the channel type of the MOS transistors made with the technology. PMOS technologies implement p-channel transistors by diffusing p-type dopants (usually boron) into an n-type silicon substrate to form the source and drain. P-channel is so named because the channel is comprised of positively charged carriers. NMOS technologies are similar, but use n-type dopants (normally phosphorus or arsenic) to make n-channel transistors in p-type silicon substrates. N-channel is so named because the channel is comprised of negatively charged carriers. CMOS or Complementary MOS technologies combine both p-channel and n-channel devices on the same silicon. Either p- or n-type silicon substrates can be used, however, deep areas of the opposite doping type (called wells) must be defined to allow fabrication of the complementary transistor type.

Most of the early semiconductor memory devices, like Intel's pioneering 1103 dynamic RAM and 1702 EPROM were made with PMOS technologies. As higher speeds and greater densities were needed, most new devices were implemented with NMOS. This was due to the inherently higher speed of n-channel charge carriers (electrons) in silicon along with improved process margins. CMOS technology has begun to see widespread commercial use in memory devices. It allows for very low power devices used for battery operated or battery back-up applications. Historically, CMOS has been slower than any NMOS device. However, CMOS technology has been improved to produce higher speed devices. The extra cost of processing required to make both transistor types had kept CMOS memories limited to those areas where the technology's special characteristics would justify the extra cost. In the future, the learning curve for high performance CMOS costs are making a larger number of memory devices practical in CMOS.

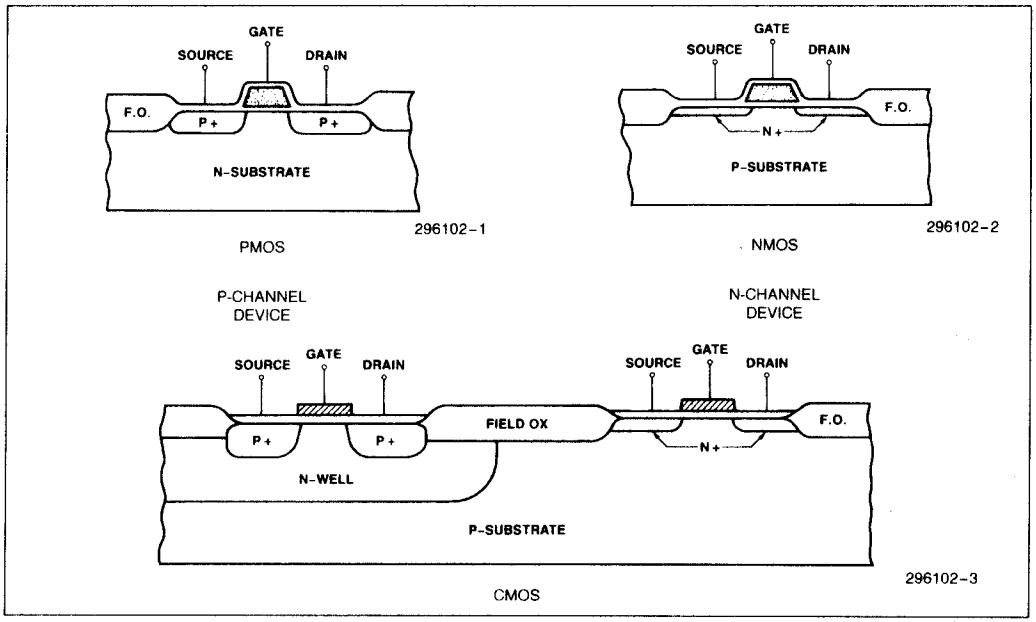

Figure 1. MOS Process Cross-sections

In the following section, the basic fabrication sequence for an HMOS circuit will be described. HMOS is a high performance n-channel MOS process developed by Intel for 5V single supply circuits. HMOS, and CHMOS, CHMOS-E (EPROM) and ETOX™ (Flash Memory), along with their evolutionary counterparts comprise the process family responsible for most of the memory components produced by Intel today.

The MOS IC fabrication process begins with a slice (or wafer) of single crystal silicon. Typically, it's 100 or 150 millimeter in diameter, about a half millimeter thick, and uniformly doped p-type. The wafer is then oxidized in a furnace at around 1000°C to grow a thin layer of silicon dioxide (SiO_2) on the surface. Silicon nitride is then deposited on the oxidized wafer in a gas phase chemical reactor. The wafer is now ready to receive the first pattern of what is to become a many layered complex circuit. The pattern is etched into the silicon nitride using a process known as photolithography, which will be described in a later section. This first pattern (Figure 2) defines the boundaries of the active regions of the IC, where transistors, capacitors, diffused resistors, and first level interconnects will be made.

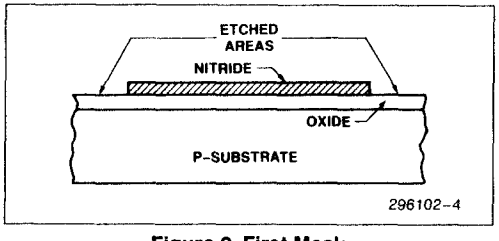

Figure 2. First Mask

The patterned and etched wafer is then implanted with additional boron atoms accelerated at high energy. The boron will only reach the silicon substrate where the nitride and oxide was etched away, providing areas doped strongly p-type that will electrically separate active areas. After implanting, the wafers are oxidized again and this time a thick oxide is grown. The oxide only grows in the etched areas due to silicon nitride's properties as an oxidation barrier. When the oxide is grown, some of the silicon substrate is consumed and this gives a physical as well as electrical isolation for adjacent devices as can be seen in Figure 3.

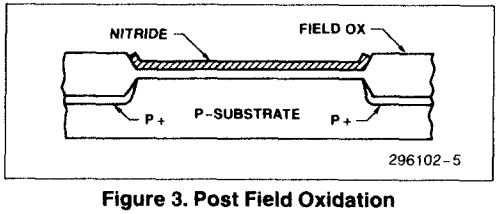

Figure 3. Post Field Oxidation

Having fulfilled its purpose, the remaining silicon nitride layer is removed. A light oxide etch follows taking with it the underlying first oxide but leaving the thick (field) oxide.

Now that the areas for active transistors have been defined and isolated, the transistor types needed can be determined. The wafer is again patterned and then if special characteristics (such as depletion mode operation) are required, it is implanted with dopant atoms. The energy and dose at which the dopant atoms are implanted determines much of the transistor's characteristics. The type of the dopant provides for depletion mode (n-type) or enhancement mode (p-type) operation.

The transistor types defined, the gate oxide of the active transistors are grown in a high temperature furnace. Special care must be taken to prevent contamination or inclusion of defects in the oxide and to ensure uniform consistent thickness. This is important to provide precise, reliable device characteristics. The gate oxide layer is then masked and holes are etched to provide for direct gate to diffusion ("buried") contacts where needed.

The wafers are now deposited with a layer of gate material. This is typically poly crystaline silicon ("poly") which is deposited in a gas phase chemical reactor similar to that used for silicon nitride. The poly is then doped (usually with phosphorus) to bring the sheet resistance down to 10–20 Ω/square. This layer is also used for circuit interconnects and if a lower resistance is required, a refractory metal/polysilicon composite or refractory metal silicide can be used instead. The gate layer is then patterned to define the actual transistor gates and interconnect paths (Figure 4).

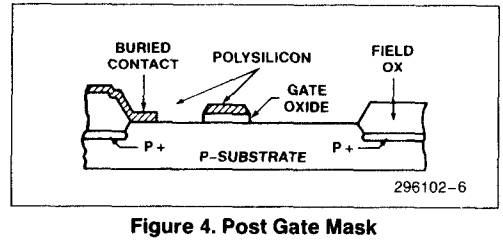

Figure 4. Post Gate Mask

The wafer is next diffused with n-type dopant (typically arsenic or phosphorus) to form the source and drain junctions. The transistor gate material acts as a barrier to the dopant providing an undiffused channel self-aligned to the two junctions. The wafer is then oxidized to seal the junctions from contamination with a layer of SiO_2 (Figure 5).

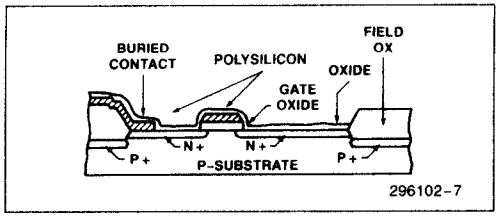

Figure 5. Post Oxidation

A thick layer glass is then deposited over the wafer to provide for insulation and sufficiently low capacitance between the underlying layers and the metal interconnect signals. (The lower the capacitance, the higher the inherent speed of the device.) The glass layer is then patterned with contact holes and placed in a high temperature furnace. This furnace step smooths the glass surface and rounds the contact edges to provide uniform metal coverage. Metal (usually aluminum or aluminum/silicon) is then deposited on the wafer and the interconnect patterns and external bonding pads are defined and etched (Figure 6). The wafers then receive a low temperature (approximately 500°C) alloy that insures good ohmic contact between the aluminum and diffusion or poly.

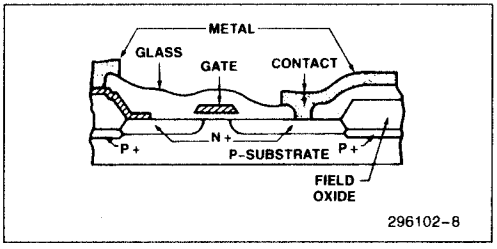

Figure 6. Complete Circuit (without passivation)

At this point the circuit is fully operational, however, the top metal layer is very soft and easily damaged by handling. The device is also susceptible to contamination or attack from moisture. To prevent this the wafers are sealed with a passivation layer of silicon nitride or a silicon and phosphorus oxide composite. Patterning is done for the last time opening up windows only over the bond pads where external connections will be made.

This completes basic fabrication sequence for a single poly layer process. Double poly processes such as those used for high density Dynamic RAMs, EPROMs, flash memories, and EEPROMs follow the same general process flow with the addition of gate, poly deposition, doping, and interlayer dielectric process modules required for the additional poly layer (Figure 7). These steps are performed right after the active areas have been defined (Figure 3) providing the capacitor or floating gate storage nodes on those devices.

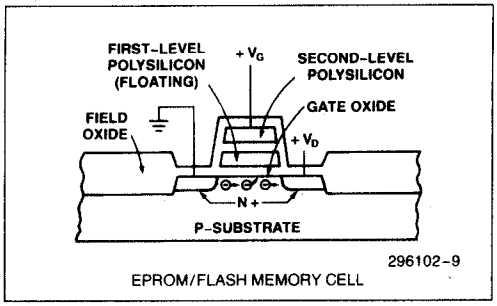

Figure 7. Double Poly Structure

After fabrication is complete, the wafers are sent for testing. Each circuit is tested individually under conditions designed to determine which circuits will operate properly both at low temperature and at conditions found in actual operation. Circuits that fail these tests are inked to distinguish them from good circuits. From here the wafers are sent from assembly where they are sawed into individual circuits with a paper-thin diamond blade. The inked circuits are then separated out and the good circuits are sent on for packaging.

Packages fall into two categories—hermetic and non-hermetic. Hermetic packages are Cerdip, where two ceramic halves are sealed with a glass fritt, or ceramic with soldered metal lids. An example of hermetic package assembly is shown in Table 1. Non-hermetic packages are molded plastics.

The ceramic package has two parts, the base, which has the leads and die (or circuit) cavity, and the metal lid. The base is placed on a heater block and a metal alloy preform is inserted. The die is placed on top of the preform which bonds it to the package. Once attached, wires are bonded to the circuit and then connected to the leads. Finally the package is placed in a dry inert atmosphere and the lid is soldered on.

The cerdip package consists of a base, lead frame, and lid. The base is placed on a heater block and the lead frame placed on top. This sets the lead frame in glass attached to the base. The die is then attached and bonded to the leads. Finally the lid is placed on the package and it is inserted in a seal furnace where the glass on the two halves melt together making a hermetic package.

In a plastic package, the key component is the lead frame. The die is attached to a pad on the lead frame and bonded out to the leads with gold wires. The frame then goes to an injection molding machine and the package is formed around the lead frame. After mold the excess plastic is removed and the leads trimmed.