BCTM PROCEEDINGS

PROCEEDINGS OF THE 1995 BIPOLAR/BiCMOS CIRCUITS AND TECHNOLOGY MEETING

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PROCEEDINGS OF THE 1995 BIPOLAR/BiCMOS CIRCUITS AND TECHNOLOGY MEETING

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Welcome from the General Chairman

Robert A. Pease

General Chairman

Krishna Shenai

Technical Program Chairman

The Conference Committee and I welcome you to the 1995 IEEE Bipolar/BiCMOS Circuits and Technology Meeting. At this year's meeting in Minneapolis, MN we celebrate the 10th Anniversary of BCTM. The conference reflects the strong international nature of activities in this field. This year, we accepted a total of 41 contributed papers from over 70 submissions.

For the first time, we have introduced a short course at BCTM. This year's short course is on technologies for wireless and high-speed communication systems and is taught by three internationally-respected authorities in the field. In addition, beginning with the 1995 BCTM, we have formed a separate subcommittee on Power Devices. As a result, two complete sessions dealing with state-of-the-art papers on advanced power device and integrated circuit technologies will be presented in this year's technical program.

Another new feature of this year's BCTM is the presentation of the Best Student Paper award for an outstanding student presentation made at the 1994 BCTM. This award will be given to Mr. Hsin-Hua Li of the University of Wisconsin - Madison.

This year's keynote speaker is Ken Sodomsky who will deliver a speech on positive future opportunities for bipolar technologies. The luncheon speaker is Charlie Sporck who will enlighten the audience with his insights on the early days of Silicon Valley.

The technical program consists of a total of 13 sessions. A total of five invited papers will be presented in these sessions. On Monday night, two panel sessions are planned. The first is entitled "High-Performance BiCMOS vs. Bipolar and/or CMOS". The second session is "Power Integrated Circuits: BiCMOS vs. CMOS vs. Bipolar".

In all, this year's BCTM promises to be an exciting and innovative meeting. On behalf of the IEEE Electron Devices Society, which sponsors the BCTM, and Krishna Shenai, Technical Program Chairman, I wish to express my sincere appreciation and congratulations to the members of the Conference Committee for the outstanding job they have done in planning and organizing the 1995 BCTM. The authors are to be commended for their efforts in preparing and presenting the high-quality papers that form the foundation of this conference. It is with great pleasure that I extend a hearty welcome to them and all of the attendees of the 1995 IEEE Bipolar/BiCMOS Circuits and Technology Meeting.

Robert A. Pease

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ON LOG DOMAIN FILTERING FOR RF APPLICATIONS

Prof. Douglas Frey
EECS Department
19 Memorial Drive West
Lehigh University
Bethlehem, PA 18015

ABSTRACT: The design concept of log filters is reviewed. A new second order filter topology which is particularly useful for RF signal processing is introduced with a discussion of its features which meet the needs of RF design.

I. INTRODUCTION:

In [1] the class of log filters was fully articulated for the first time. In [2], [3], and [4] further aspects of the design of such filters were explored. The main benefits available through the use of these filters are that the circuit realizations are integrable, useful to very high frequencies, and require relatively few parts to implement them. Recent examples of other research in the area of integrable high frequency filters are given in [5] and [6]. An interesting aspect of these filters is that signals are processed quite nonlinearly within the filter despite the fact that the overall transfer characteristics are linear. This nonlinearity may be exploited in mixing signals. Simulations presented in [1], [3], and [4] suggest that the lack of pure log conformity in the transistors used to realize the filters does not preclude large dynamic range. In the present paper the design of log filters is further explored in the context of radio frequency (RF) signal processing. The basic circuitry needed in this context includes filters, mixers, and oscillators--in this case, current controlled oscillators (ICOs). A new second order log filter is presented here that uses only NPN transistors in the gain path and operates with a single power supply of under 3 volts. This filter is shown to be widely tunable and generally useful at frequencies up to 500MHz using the AT&T CBIC-V2 process.

By way of introduction it is useful to review the basic log filter design approach. As described elsewhere [1,3] one designs a log filter by finding an appropriate state space realization for a desired transfer function. Following this, an exponential mapping is applied to the state variables and input and output quantities. Then a simple manipulation of the transformed state equations produces a set of nodal equations that can be implemented via transistors, current sources, and grounded capacitors. The resulting "log filter" effectively takes the natural logarithm of the input signal (assumed to be a current), processes this log signal with a log domain filter, and recovers the output via an exponentiation operation. For the sake of clarity, let us consider the design procedure necessary to create a log filter version of a first order lowpass filter. The first step requires that a state space description of this filter be found. Equation 1 shows such a description.

$$\dot{X} = -\omega_0 X + \omega_0 U \quad ; \quad Y = X \tag{1}$$

Now suppose that the quantities, U and X are replaced via $I_s\exp(V_{in}/V_t)$ and $I_0\exp(V_1/V_t)$, respectively. These substitutions define nonlinear mappings on the variables. Substitution of these expressions followed by scaling the state equation by $CV_t\exp(-V_1/V_t)$, where C is a positive real constant, results in the following equation:

$$C\dot{V}_1 = -I_0 + I_s e^{(V_{in}-V_1)/V_t}$$
$$Y = I_0 e^{V_1/V_t} = I_s e^{(V_1+V_D)/V_t}$$
$$\text{where} \quad I_0 = \omega_0 C V_t \quad , \quad V_D = V_t \ln\left(\frac{I_0}{I_s}\right) \tag{2}$$

The differential equation above can be thought of as a nodal equation, where the current in a grounded capacitor of value, C, is equal to the current in a current source combined with that flowing in a diode junction connected between a pair of nodes, having respective potentials, V_{in} and V_1. Note that V_t and I_s are assumed equal to the thermal voltage and the reverse saturation current of the junctions, respectively. The full interpretation is explored in [1] and [4]. A simplified design of this circuit is shown in Figure 1. By following the analysis outlined above, one may prove that the output current is in fact a lowpass filtered version of the input current, where it should be noted that DC must be added to the input to ensure that it remains positive at all times. Higher order filters may be created in the same way, as in [1].

In the next section a new second order section will be described that is useful for general RF filtering and oscillator design. The design of RF circuitry presents several important constraints. First, the signal processing circuitry must be low noise. At the same time the circuitry must be highly linear, especially regarding third order distortion, which creates in-band IM products of particular concern. Another important issue in the present design environment is that the circuitry should be capable of operating at low supply voltage--for example, 3 volts or less. Finally, one hopes to consume a minimum of supply current at the same time. Reconciling these constraints is a major problem.

Log filters have several properties that make them appropriate in this context. The impedance levels are inherently low, which improves noise performance and high frequency response. At least in principle, these filters have perfect linearity. In practice, however, achievable linearity is limited by the lack of pure log conformity and the finite beta of the transistors. Nevertheless, due to the design philosophy, one can argue that these effects are handled in, at least, a suboptimal way. Observe that standard circuitry based upon differential pairs is nonlinear even in theory, and still suffers from finite gain effects. Regarding power supply operation, it has been shown in [3] that log filters with exceptional frequency behavior can be designed to operate at 3.3 volts. Below a design will be shown which operates at 2.7 volts. Furthermore, the speed of the circuitry is such that supply currents can be minimized.

Log filters possess other features which make them useful in RF applications. These features arise from the logarithmic signal processing. Specifically, since multiplication can be achieved via addition in the log domain, then log domain filters allow for particularly economical mixing of signals. Furthermore, the gain of log domain circuitry can be controlled via the application of varying

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DC input currents. This is, of course, nothing more than the multiplication of a signal with a constant input signal. Hence the AGC function is easily implemented in log domain circuit architectures.

II. A NEW LOG DOMAIN CIRCUIT DESIGN

Given that log filters possess the right qualities for RF design, let us consider a basic design useful for typical RF circuits. In the discussion below, we will focus on an all-NPN circuit topology. The reasons for this are twofold. First, it appears that all-NPN topologies will be the fastest, especially in consideration of the fact that most "fast" IC processes have optimized NPN transistors. Slower devices on a given technology can be used to implement current sources if desired. Secondly, all-NPN designs offer, in the author's opinion, operation using the lowest possible supply rail; however, this remains an open issue, since complementary topologies could use very small supplies if the difference between PNP and NPN V_{be}s could be managed.

Let us begin by considering the problem of creating a log domain second order filter which would be useful in making image rejection filters, and in some tuner applications. With minor modifications this circuit will also provide a quadrature oscillator and mixer. We will consider a multiple-input, multiple-output state variable filter whose Q and center frequency, ω_0, are programmable--the programmability being one of the advantages of log filters. Let us start from the following state space description for this filter:

$$\begin{aligned} \dot{x}_1 &= -\frac{\omega_0}{Q}x_1 - \omega_0 x_2 + (1+\frac{1}{Q})\omega_0 u_1 \\ \dot{x}_2 &= \omega_0 x_1 - \omega_0 u_2 \\ y_1 &= x_1 \quad , \quad y_2 = x_2 \ , \end{aligned} \tag{3}$$

where u_1 and u_2 are inputs, y_1 and y_2 denote the outputs, and x_1 and x_2 are the state variables. The value of the scale factor, 1 + 1/Q, on the u_1 input is that it allows for a balanced DC equilibrium in the final circuit implementation. This issue is addressed in [1]. For the present purposes we assume that the inputs and the outputs will be currents in the circuit realization of this filter. Typically, only one of the inputs is driven with the external input to the filter, while the other is used as a "dummy" input driven by a constant positive input. For example, if the actual filter input is applied as u_1, then y_1 will be a bandpass filtered version of u_1. Alternatively, a lowpass response is obtained at y_1 by applying the filter input via u_2. It is a simple matter to show that,

$$\begin{aligned} H_1(s) &= \frac{y_1}{u_1} = (1+\frac{1}{Q})\frac{\omega_0 s}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2} \qquad (u_2 = 0) \\ H_2(s) &= \frac{y_1}{u_2} = (1+\frac{1}{Q})\frac{\omega_0^2}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2} \qquad (u_1 = 0) \end{aligned} \tag{4}$$

As suggested above the use of exponential mappings on the inputs and state variables results in a set of nodal equations corresponding to each of the differential equations in equation 3. These nodal equations may be realized with capacitors, transistors, and current sources. Specifically, suppose the following mappings are used on the quantities in equation 3:

$$\begin{aligned} x_1 &= I_{st}e^{V_1/V_t} \ ; \ x_2 = I_{st}e^{V_2/V_t} \\ u_1 &= I_{st}e^{V_{01}/V_t} \ ; \ u_2 = I_{st}e^{V_{02}/V_t} \end{aligned} \quad \text{where } I_{st} = \frac{I_s^2}{I_0} \tag{5}$$

where V_t is the thermal voltage, q/KT, and I_s is the reverse saturation current, both from the diode law (assumed to govern the transistor junctions of the devices which realize the filter), and all other quantities are positive voltages and currents denoted by subscripted variables V and I, respectively. I_0 is a positive constant which is defined below in equation 6. That all currents are positive is an issue dealt with in [1], where it is shown that this constraint is met with reasonable care in the design. Note that these mappings are similar to constitutive relations between voltages and currents in what amount to ideal transistor junctions in forward bias, as discussed in more detail in [1]. Applying these mappings to equation 3, and scaling (note that the positive constant, C, is introduced in the scaling of the state equations) we get the following:

$$\begin{aligned} C\dot{V}_1 &= -\frac{I_0}{Q} - I_0 e^{(V_2-V_1)/V_t} + I_0 e^{(V_{01}-V_1)/V_t} \\ C\dot{V}_2 &= I_0 e^{(V_1-V_2)/V_t} - I_0 e^{(V_{02}-V_2)/V_t} \\ y_1 &= I_{st}e^{V_1/V_t} \ , \ y_2 = I_{st}e^{V_2/V_t} \end{aligned} \tag{6}$$

$$\text{where} \quad I_0 = C\omega_0 V_t \quad \text{and} \quad I_{st} = \frac{I_s^2}{I_0}$$

A simple manipulation of equation 6 results in the following:

$$\begin{aligned} C\dot{V}_1 &= -\frac{I_0}{Q} - I_0 e^{(V_2-V_1)/V_t} + I_s e^{(V_{01}+V_Q-V_1)/V_t} \\ C\dot{V}_2 &= I_s e^{(V_1+V_0-V_2)/V_t} - I_0 e^{(V_{02}-V_2)/V_t} \\ y_1 &= I_s e^{(V_1-V_0)/V_t} \ , \ y_2 = I_s e^{(V_2-V_0)/V_t} \end{aligned} \tag{7}$$

$$\text{where} \quad V_0 = V_t \ln(\frac{I_0}{I_s}) \qquad V_Q = V_t \ln(\frac{I_0(1+1/Q)}{I_s})$$

Now the dynamical equations of equation 3 have been transformed into a set of equations that may be interpreted as nodal equations. Specifically, the currents in a pair of grounded capacitors (both of value C), having respective voltages V_1 and V_2 across them, are given by a combination of currents through forward biased transistor junctions and currents sources. That this is so will be addressed directly. The voltages, V_{01} and V_{02}, are obtained via a "logging" operation by forcing always positive currents through diode junctions as discussed below.

Before discussing applications, the circuit design will be addressed. The positive exponential term in the second nodal equation of equation 7 can be realized using a level shifter and voltage follower as shown in Figure 2a. It is a simple matter to show that the emitter current of Q_2 is $I_s\exp((V_1+V_0-V_2)/V_t)$. The analogous term in the first nodal equation is realized with a level shift in the input logging circuitry described below. An interesting new circuit for the

implementation of the negative exponential terms is shown in Figure 2b, where we focus attention on the term in the first nodal equation. With the help of Q_2 and Q_3, a current of I_0 amps is forced to flow in Q_1. Using this fact, it follows that the collector current of Q_4 is given by $I_0\exp((V_2-V_1)/V_t)$. Tying this collector to a node (V_1) pulls current which results in the negative sign.

Now consider the generation of the voltages, V_{01} and V_{02}. Figure 3 shows circuits for this purpose. The indicated connection of transistors causes currents of I_0 to flow in the emitters of Q_1 and Q_4, $I_0(1+1/Q)$ to flow in the emitter of Q_3, and u_1 and u_2 to flow in the emitters of Q_2 and Q_5, respectively. As a result, the voltages, V_{01} and V_{02}, are given by,

$$V_{01} = V_t\ln(\frac{I_0}{I_s}) + V_t\ln(\frac{u_1}{I_s}) \rightarrow u_1 = I_s e^{V_{01}/V_t}$$
$$V_{02} = V_t\ln(\frac{I_0}{I_s}) + V_t\ln(\frac{u_2}{I_s}) \rightarrow u_2 = I_s e^{V_{02}/V_t} \qquad (8)$$
$$V_Q = V_t\ln(\frac{I_0(1+1/Q)}{I_s})$$

Note that the voltage at the base of Q_3 is level shifted up by V_Q volts from the voltage V_{01}. This is the voltage required to implement the positive exponential term in the first nodal equation of equation 7. Observe that the output currents, y_1 and y_2, are obtained, using equation 7, by level shifting V_1 and V_2, respectively, down by V_0 volts, and applying this voltage to the base emitter junctions of output exponentiating transistors. The voltage, V_3, labelled in Figure 2b, is the necessary voltage relative to V_1 for the purpose of output exponentiation. Putting the circuits of Figures 2 and 3 together results in the complete second order multiple-input, multiple-output log filter shown in Figure 4, which implements the linear system described by equation 3.

This circuit can be used to provide bandpass and lowpass filter functions. Since no node is more than 3 diode drops away from ground, this circuit will operate with a supply voltage of under 3 volts. Since ω_0 is proportional to I_0 (equation 6), the filter is widely tunable, having performance similar to that reported in [3]. The input nodes where u_1 and u_2 are applied are AC virtual grounds. As a result, a 50 Ohm resistor in series with a blocking capacitor may be connected to these nodes providing not only a 50 Ohm input impedance but also a useful voltage to current converter. The outputs of the circuit may also be made into 50 Ohm equivalent sources by mirroring the output currents, y_1 and y_2 , into 50 Ohm grounded resistors. In systems where signals are in current form these additions are not necessary. Nevertheless, in the simulations presented in the next section the 50 Ohm input and output terminations were used to allow easier comparison to other circuit topologies.

The circuit of Figure 4 can be augmented with limiting circuitry and used to make a quadrature oscillator. Oscillation is achieved by using a negative value for Q. It is easily shown that y_1 and y_2 produce quadrature outputs in a way typical of the state variable topology. The intrinsic speed of the devices permits rapid frequency shifting which may be useful in frequency-hopped spread spectrum systems.

A final aspect of the circuit of Figure 4 is that it accomplishes the mixing function at both inputs, simultaneously if desired. Specifically, by injecting signal components as part of the current sources labelled, u_{1x} and u_{2x}, the voltages, V_{01} and V_{02}, applied to the filter correspond to those which would be obtained by multiplying the respective pairs of inputs--i.e., u_1 and u_{1x}, and u_2 and u_{2x}--and applying these mixed signals as the respective inputs. This fact can be proven easily from equation 8 with the appropriate substitutions. Notice that the logging operation permits multiplication to be performed as addition. Hence, the front end circuitry of the circuit in Figure 4 accomplishes mixing essentially for free. The circuit shown, however, is not a balanced mixer. A balanced mixer can be made by adding a copy of the input circuits of Figure 3 and driving the new inputs with an inverted version of the signal input.

III. SIMULATION RESULTS

The circuit of Figure 4 was optimized as described below and simulations were performed on two versions of the circuit using both ideal transistor models and AT&T CBIC-V2 models. The first version of the circuit was designed to operate between 10MHz and 100MHz, while the second was designed to operate between 100MHz and 500MHz. Unless otherwise stated only the bandpass function from input u_1 to output y_1 was investigated.

A new idea was used in the optimization of both filters. The finite bandwidth of the "real" (AT&T) models causes both degradation in the distortion performance and in the frequency response. Both problems were found to be mitigated by including a series resistance with the grounded capacitors. This addition seemed natural since some parasitic resistance is always associated with integrated capacitors. It was found that by making the RC product of the ideal grounded capacitor and the series reistance equal to approximately 0.8×10^{-10}, the distortion was reduced at the output and Q-enhancement was virtually eliminated up to 500MHz. This idea has not been reported elsewhere, and at the present time is presented as a heuristic which requires analytical justification. Nevertheless, the results were sufficiently good that all results using "real" models incorporated the RC combination. It should be noted that using process models that reflect the variations one could expect in manufacture the performance of the filters were only modestly changed, indicating a low sensitivity to process variation. It was concluded that the RC combination represents a fairly robust improvement that could be reasonably tuned to a given process.

The first filter version was designed with 40 pF capacitors in series with 2 Ohm resistors using AT&T models. The set current, I_0, was varied from 80μA to 800μA, which caused the center frequency of the filter to vary from approximately 10MHz to 100MHz. 50 pF capacitors were required to achieve the same frequency range using the ideal transistor models. The Q was set to 4 by design. The input bias current, I_{DC}, was set to 1mA. This is the current added to the AC signal at the input to ensure always positive input current. Using ideal NPN transistor models having beta equal to 100,000 the frequency response was exactly as predeicted. The IMD using two tones separated by 1MHz was at the lower limit of accuracy--that is, less than .01%. The beta was changed to 100 which caused the Q of the filter to drop slightly, from 4 to 3.2. The IMD incresed to 0.35% with signals at 6dB below the clip point.

Next, the filter was simulated using the AT&T models. The frequency response was within 1dB of that using ideal models. As shown in figure 5, the filter performance is extremely stable with changes in the center frequency. Figure 6 shows the frequency performance with the Q set to infinity by design. While some Q degradation is observed the frequency response is extremely stable over the wide tuning range. IMD was measured to be 1% with the Q equal to 4, a center frequnency of 50MHz and a pair of tones causing the output to be 6dB below clipping. The Noise Figure relative to a 50 Ohm source was 17dB and 11dB for the AT&T and ideal models,

respectively, with the center frequency set to 100MHz.

The performance of the lowpass output was investigated for completeness. Using all component values and settings as above with the exception of the Q setting, the lowpass filter response was noted. In this case the Q was designed to be 0.707, corresponding to a Butterworth filter. Using ideal models the response was essentially ideal. Using the AT&T models the response characteristics shown in Figure 7 were obtained. IMD under the same circumstances as above was found to be 0.3% using the AT&T models, and the noise was unchanged.

A second version of the circuit was optimized for operation between 100MHz and 500MHz using grounded capacitors equal to 10 pF in series with 8 Ohm resistors for the case where AT&T models were used. The input bias current, I_{DC}, was set to 1 mA. I_0 was varied from 240 μA to 1200 μA causing the center frequency to vary between 100MHz and 500MHz. With ideal transistors, however, 15 pF capacitors were necessary to achieve the same tuning range. The Q was set by design at a target value of 4. Ideal transistors produced the same results as in the earlier case since the frequency of operation is irrelevant using ideal models. Using the AT&T models, the results shown in Figure 8 were obtained. IMD was measured with a pair of tones separated by 5MHz and the center frequency set to 200MHz. At 6dB below clipping the IMD was 1.44%. The same test performed at 400MHz yielded a 2% IMD result. The Noise Figure relative to a 50 Ohm source was 17dB and 11dB for the AT&T and ideal models, respectively, with the center frequency set to 400MHz.

IV. CONCLUSION

The design concept behind log filters has been reviewed. These filters have many of the desirable properties needed for RF applications. A new second order multiple-input, multiple-output log filter has been introduced that may find use in RF applications. The wide frequency and Q tunability of this filter in addition to its low power supply operation are particularly interesting. Simulation results suggest that this new topology has very good performance for frequencies as high as 500MHz. The circuit shown possesses the ability to mix signals, filter the result, and with additional circuitry can be used as a quadrature phase sinusoidal oscillator.

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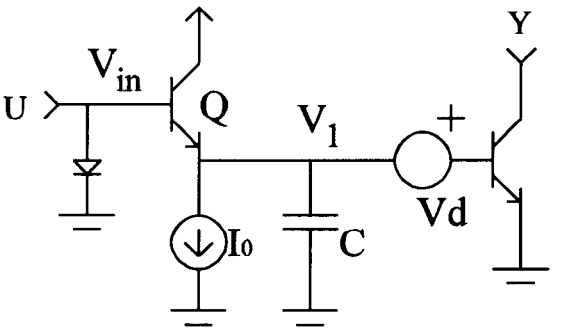

Figure 1: Simplified first order log filter.

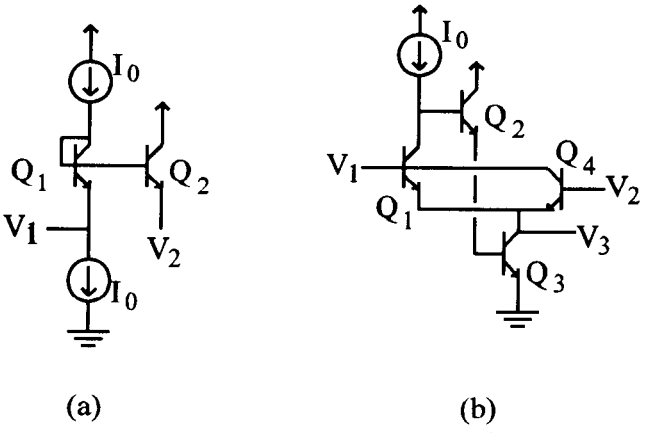

Figure 2: Exponential transconductance circuits.