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JUNE 2-4, 1992/**SEATTLE**

1992 SYMPOSIUM ON VLSI TECHNOLOGY

DIGEST OF TECHNICAL PAPERS

☐ The IEEE Electron Devices Society

☐ The Japan Society of Applied Physics

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ACKNOWLEDGEMENT

Walter Kosonocky

Shoji Tanaka

Over a decade ago, Professor Kosonocky and Professor Tanaka had a vision. They conceived a forum that could bring together engineers and scientists from the U.S. and Japan to provide cooperation and sharing of leading-edge technical information in an informal setting. Out of this, grew the VLSI Symposia which have become very successful international forums, stimulating and encouraging the exchange of knowledge and experiences in VLSI technology and design, enhancing mutual understanding.

Both Professor Kosonocky and Professor Tanaka have decided to retire as chairmen of the Japan and U.S. Executive Committees. We are grateful for their vision and guidance through the last decade.

We sincerely thank Professor Kosonocky and Professor Tanaka for a decade of leadership and wish to acknowledge their efforts and contributions in the establishment of the VLSI Symposia as a leading world-wide forum in the VLSI field. We have requested they continue their association with the Symposia as Senior Advisors.

We will extend our best efforts to continue the momentum of the VLSI Symposia as we go forward with advice from Professor Kosonocky and Professor Tanaka.

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FOREWORD

WELCOME to Seattle for the 12th Symposium on VLSI Technology

The spread of multi-national alliances in business and technology serves to indicate the extent to which the world has shrunk and, as expected, deep-submicron VLSI technology is amongst the leaders in this trend. Yet, alliances are only one example of structural changes taking place that cut to the core of our business. The escalating cost of process R&D can only be satisfied if our technology continues to penetrate broader applications with value-added products. Thus, as always, R&D drives the reduction in cost per function which in turn simulates the market. But, as process technology gains become more difficult to realize, we, as leaders in the selection of future technologies, need to be sure that the cost-per-function improvement opens new markets at the required rate. To this end, it has been recognized that the Symposium on VLSI Technology provides a prime forum for the discussions of issues relating to process technology options in the light of the international market place. The Symposium is co-sponsored by the IEEE Electron Devices Society and the Japan Society of Applied Physics.

The Symposium will begin with two invited papers that illustrate the close relationship between detailed technology issues and broad business implications. The first, by R. Doering of TI, explores major changes in the approach to IC manufacturing under title: "Trends in Single Wafer Processing." The second, by F. Masuoka of Toshiba, takes an equally challenging view of the incumbent DRAM business in: "Technology Trend of Flash-EEPROM: Can Flash-EEPROM overcome DRAM?"

The remainder of the Technical Program continues our excellent record of quality papers and interesting Rump Sessions. We are indebted to the program committees serving in the U.S. and Japan under the able leadership of Jim Clemens and Masao Fukuma. These committees reviewed 128 papers, of which 52 papers were selected, for an acceptance ratio of about 40%. As in recent years, we have a minimum of overlapping sessions which are confined to just Wednesday afternoon.

With the growing emphasis on technology for high-speed signals passing between transistors, the Workshop this year is appropriately entitled: "VLSI Interconnection and Packaging Technology." We thank S. Wong and T. Nishimura for arranging an excellent program on Monday. We also want to thank especially the members of the Symposium Committee who have worked so hard in bringing this Symposium together: Dick Chapman and Eiji Takeda, secretary, Hans Stork and Katsu Izumi, publications, Youssef El-Mansy and Taiji Ema, treasurer, and last but not least Bill Siu and Nobuhiro Endo, local arrangements.

The 1993 Symposia on VLSI Technology and VLSI Circuits will be held May 16 to 21 at the now permanent site of Kyoto. Please note that the Workshop is on Sunday.

Again, welcome to the 1992 Symposium. We hope that your stay in Seattle will be enjoyable and rewarding. As always, your comments and suggestions will be greatly appreciated.

Dirk Bartelink	Shojiro Asai
Symposium Chairman	Symposium Co-Chairman

Trends in Single-Wafer Processing

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Abstract **– One of the most significant trends in semiconductor manufacturing over the past three decades has been the gradual replacement of batch processing with single-wafer processing. Two other trends, the use of larger silicon wafers (to reduce manufacturing cost) and the necessity for more demanding process-performance specifications (to allow continued device/circuit scaling) have driven this move to single-wafer equipment for many processes. It is now technically feasible to produce silicon integrated circuits with 100% single-wafer processing. In the next decade, it may also become economically feasible to do so.**

INTRODUCTION – the Trend Toward Single-Wafer Processing

Commercial integrated circuit manufacturing began 30 years ago with batch processing for almost all steps. Processing many wafers simultaneously in relatively inexpensive equipment provided low-cost manufacturing for the simple commodity circuits of the SSI and MSI eras. However, for a variety of reasons, single-wafer processes have been gradually displacing their batch counterparts. Today, diffusion and wet-clean operations remain the major hold-outs for batch processing. This move toward single-wafer processing is associated with many other trends in the integrated circuit industry, e.g.: larger wafers, device/circuit scaling, more dry processes, tool "clustering," increased automation of process and factory control, and differentiated products.

The well-known trends toward smaller features, larger circuits, and larger wafers are shown in Table 1. Since 1967, the available lithographic resolution has improved approximately 20X, which indicates that a given area of silicon should now contain about 400X as many (scaled) IC components. However, the circuit complexity (as measured by random-access memory size) has actually increased 64,000X over the same period. The extra factor of 160 is partly the result of more efficient memory-cell/circuit design and partly due to the use of more silicon area for the larger memory chips.

TABLE 1
IC INDUSTRY HISTORICAL TRENDS

YEAR	MINIMUM PATTERN	MEMORY SIZE	WAFER DIAMETER
1962	20 um	--	25 mm
1967	10	256 bit	25
1970	6	1 Kbit	50
1973	4	4 K	75
1976	3	16 K	75
1979	2	64 K	100
1982	1.5	256 K	125
1985	1.0	1 Mbit	150
1988	0.8	4 M	150
1991	0.5	16 M	200

To minimize the cost of the larger chips, wafer area has been increased 64X over the past 25 years. By the end of the 1990s, wafer area should quadruple again as 300-mm diameter becomes available. However, the increase in wafer diameter tends to adversely affect process equipment cost, partially offsetting the potential savings. The main contributors to this cost increase are:

1. lower tool throughput (e.g., fewer wafers per batch),
2. larger tool size, and/or
3. increased tool complexity (e.g., to maintain process uniformity across the larger wafers).

The last factor is further exacerbated by the minimum-feature scaling trend -- the process uniformity specifications get tighter even as the wafers are getting larger. One way of looking at the general trend toward single-wafer processing is to regard it as a tool optimization which tends to sacrifice the first factor in an attempt to minimize the other two cost factors. By designing a tool to process only a single wafer at a time, it becomes practical to have a small process "chamber" with very uniform distributions of reactants, energies, etc. across the face of the wafer. Particularly in the last decade, this approach has led to a succession of high-performance single-wafer tools which have contributed significantly to continued device/circuit scaling.

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THERMAL PROCESSING

The development of vertical furnace tubes has helped prolong the use of large-batch hot-wall tools into the era of 200-mm wafers and 0.5-um geometries. However, the advent of 300-mm wafers and sub-0.25-um devices will probably require mini-batch or even single-wafer equipment for sufficient control of thermally-driven processes. Several vendors already offer Rapid Thermal Processing (RTP) tools which provide direct radiant heating of single wafers, eliminating the long push/pull times required with hot-wall tubes. RTP has been experimented with for years, principally for gate oxidation and junction annealing, but has thus far been limited in IC production to "non-critical operations" (e.g., BPSG reflow) by the lack of adequate techniques for achieving good temperature uniformity across the wafer. In particular, the RTP tools commercially available today are not capable of adjusting the radiant energy distribution delivered across the wafer to compensate for the temperature- and position-dependent heat losses. However, recent advances in temperature sensors and multi-zone heat sources should allow RTP to fulfill its potential in time for 300-mm wafers.

In general, processes are not considered practical until rates of at least 10-20 wafers per hour are achieved. This is a significant challenge for single-wafer LPCVD and oxidation of relatively thick films and for single-wafer "drive" of deep diffusions (e.g., bipolar DUF and CMOS wells). Nevertheless, good progress is being made on adequate single-wafer RTP rates for LPCVD silicon, silicon dioxide, silicon nitride, and tungsten. It has also been shown that 900°C steam oxidation rates continue to increase significantly with pressure up to at least 70 atmospheres, which is practical in a small single-wafer chamber, and that device-quality thick isolation oxides can be grown at rates up to at least 3000 angstroms/min. The same type of single-wafer very-high-pressure chamber has also been used to rapidly reflow BPSG in steam or nitrogen ambients at temperatures as low as 720°C, replacing yet another conventional batch hot-wall process, but, perhaps more importantly, providing new process integration capability (e.g., enhanced compatibility of BPSG reflow with underlying silicides, shallow junctions, etc.). Technically, the most difficult type of process in which to obtain a respectable single-wafer rate is a simple, purely thermal, "deep-diffusion drive." Such processes are already usually performed at temperatures close to material limits in batch hot-wall furnaces. In some instances, the ambient has a significant effect on rate. For example, wells suitable for 0.35-um CMOS have been demonstrated via enhanced diffusion in ammonia at 1100°C for only 5 minutes in a single-wafer RTP reactor. This process and all of the other single-wafer examples in this paragraph were used in an experiment in which double-level-metal (DLM) 0.35-um CMOS circuits were fabricated entirely without hot-wall processes of any kind and in cycle-times as short as 8 days [1].

DRY VS. WET PROCESSES

For the purpose of this discussion, let's divide wet processing into the following categories:

1. patterned etching
2. blanket etching (unpatterned removal of a sacrificial film),
3. cleanup (removal of contamination),
4. photoresist development, and
5. spin coating.

Of these, patterned etching is the only one which has almost entirely been converted to dry processing in state-of-the-art manufacturing. This is primarily due to the ability of plasma etches to provide superior line-width control through a combination of anisotropy, uniformity, and end-point detection. In general, the trend toward single-wafer processing has also been greatly enhanced by the development of plasma processes, which have replaced not only many wet etches, but some purely-thermal (LPCVD and APCVD) depositions as well. The early plasma processes were performed in batch parallel-plate reactors, but the plasma technology is well-suited for scaling to single-wafer reaction chambers, which first became popular for the critical patterned etches.

New plasma techniques, such as "remote microwave," low-temperature substrate, and high-density plasmas (e.g., ECR and ICP) are enabling dry processes which produce less device/material damage while improving speed and etch selectivity. These properties are allowing plasma blanket etches to compete with wet chemistries in reliably stripping sacrificial films of photoresist, silicon nitride, silicon dioxide, and polysilicon. Several vendors are also offering dry "vapor-phase" equipment for processes such as blanket etch of silicon dioxide via anhydrous HF. Figure 1 shows a comparison of breakdown-voltage distributions for MOS capacitors fabricated with anhydrous HF vs. conventional aqueous HF deglaze of the sacrificial oxide removed in the pre-gate-oxidation cleanup sequence [2]. Comparisons of other parameters also indicate that the dry process performs at least as well as its wet counterpart. Work is presently underway to extend the scope of vapor-phase processing through the use of other reagents (e.g., HCl and ozone) as well as additional energy sources (e.g., UV light). It is possible that such equipment will provide dry cleanups, at least for organic contamination.

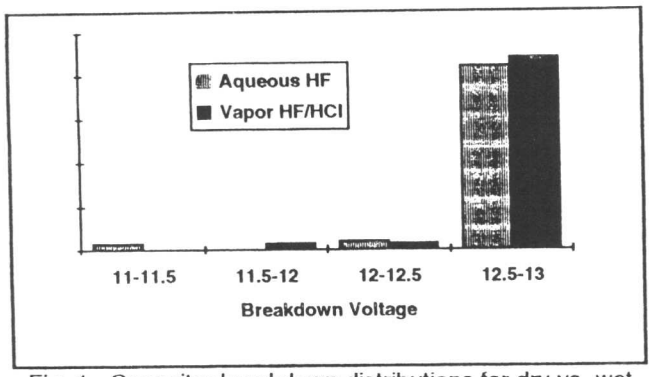

Fig. 1. Capacitor breakdown distributions for dry vs. wet deglaze of the sacrificial oxide

The removal of trace-metal and particulate contamination is perhaps the greatest technical challenge for dry processing. Some progress is being made on metal removal with vapor-phase and photo-assisted-plasma processes, but there is a long way to go. In particular, the photo-assisted processes investigated thus far tend to focus on one element at a time, which would require a long sequence of specialized cleanups. Some promising university research on "dry" particle removal has employed condensation of water vapor around particles which are then removed from the wafer surface by freezing and sublimation or laser-induced evaporation. Before these or other exotic dry techniques are perfected, it is possible to replace batch cleanups with relatively straight-forward single-wafer wet processing, which is just now becoming available for operations like post-ash photoresist cleanup. The main challenge in single-wafer wet processing, as in many single-wafer processes, is to achieve adequate throughput. At present, 20 wafers/hour appears feasible.

Dry photoresist development is also already commercially available -- in the form of the "DESIRE" process, which involves selective silylation and subsequent plasma "etching" of a specially formulated photoresist. Because of its inherent surface-imaging qualities this process is generally useful for extending optical lithography. However, it is presently competing with other extension techniques, such as Deep-Ultra-Violet (DUV) exposure, phase-shift masks, and anti-reflection coatings (ARC). It is always difficult to forecast "market-share" for such competing technologies, especially since the early technical evaluation is so difficult that the outcome may ultimately be determined by subtle factors in development investment decisions. Fortunately, the advantages of dry photoresist development are complementary to those of phase-shift masks and DUV exposure [it has been demonstrated at KrF (248-nm) and ArF (193-nm) excimer-laser wavelengths as well as g-line (436-nm), and i-line (365-nm) mercury-lamp . Thus, even if it's wide-spread use is delayed by these other techniques, it may eventually be used in conjunction with them to push optical lithography to its ultimate limits.

Wet spin coating is primarily used in IC manufacturing to deposit photoresist and "spin-on-glass" (SOG) films. SOG is good for low-temperature filling of crevices, but will almost certainly become obsolete as dry techniques for depositing dielectrics continue to improve. Spin coating of photoresist has been dominant for so long that it's hard to imagine its replacement with a dry process. However, an eventual move to 193-nm lithography could provide an opportunity for CVD photoresist, since at such short wavelengths some inorganic materials (e.g., WO_3) can be exposed and "developed."

CLUSTER TOOLS

As more single-wafer operations become available, especially in dry form, it is increasingly attractive to "cluster" these processes via single-wafer modules which share wafer-handling and computer-control systems provided by a "host" machine. Not only does this reduce the overall cost of equipment (including maintenance), it also allows an efficient "pipelining" of wafers, especially through critical process sequences. A few years ago there was widespread concern about the reliability of tools which shared subsystems between modules. Recent sales trends indicate that many customers are now comfortable with at least up to three modules per cluster, and there are now hosts on the market which can support ten or more process chambers.

PROCESS AND FACTORY CONTROL

Cluster tools provide excellent platforms for in-situ sensors and real-time process control, as well as for real-time factory control through "seamless" interfaces to sophisticated Computer Integrated Manufacturing (CIM) systems. In fact, the main potential benefit of single-wafer processing is improved process control -- resulting not just from particular process hardware advantages such as have been mentioned in the previous sections, but also from the opportunity to use information collected from individual wafers processed rapidly and sequentially through a "single position" in each chamber. It's obviously possible, and valuable, to gather wafer-level data correlated with the multiple positions in batch tools; however, the "information density in both time and space" will typically be much lower than for single-wafer processing. As wafers continue to get larger and, in more instances, bear application-specific circuits of greater value, the risk of committing a large number of wafers simultaneously to a batch process, especially late in the process flow, becomes very significant.

Ideally, a process-control engineer would like processes with in-situ sensors measuring all of the important process-state and wafer-state parameters in real time. This will probably present an open-ended challenge for integrated-circuit manufacturing, but significant progress is being made, particularly for single-wafer processes which provide better access for sensors and smaller volumes to characterize. The design of such sensors should be an integral part of an overall chamber/process design based on models of gas flow, heat flow, chemical reactions, etc. A few under-utilized CAD tools are now available in this area, but better tools and chemical models are needed. In some cases where it is not yet feasible to measure a wafer-state parameter during the process, it will continue to be desirable to make between-process measurements. Today such measurements are performed almost exclusively in separate metrology tools, but in the future, they may be available from sensors mounted in the load-locks or "auxiliary chambers" of cluster tools, so that they add little if anything to the overall cycle-time for a process flow.

There is still some controversy over how best to use real-time or between-process data. The "conservative" view is that it should be reserved for purely diagnostic purposes and that process hardware should only be improved/repaired, not guided to a process target by "tweaking recipes." However, the minimum-cost solution to keeping up with the twin challenges of larger wafers and continued device/circuit scaling will almost certainly contain a large component of automated "control-to-target" methodology, going beyond today's manual "control-limit" approach. In fact, end-point control of plasma etch is already a well-accepted step in this direction.

MANUFACTURING CYCLE-TIME

One of the most interesting potential uses of single-wafer processing is to achieve very fast manufacturing cycle times on small lots. This can be used in process-development, circuit prototyping, small-volume ASIC runs, or other applications where short cycle time is more valuable than lowest possible wafer cost. Figure 2 shows a comparison of hypothetical "conventional" (today's typical mix of batch and single-wafer tools) and "cluster" (all single-wafer tools) fabs of about 5000 wafer/month capacity [3]. At maximum throughput, the minimum wafer costs are comparable (the difference shown is less than the uncertainties in the assumptions of the models). However, the "cluster" fab is clearly much more economical for operation at short cycle times.

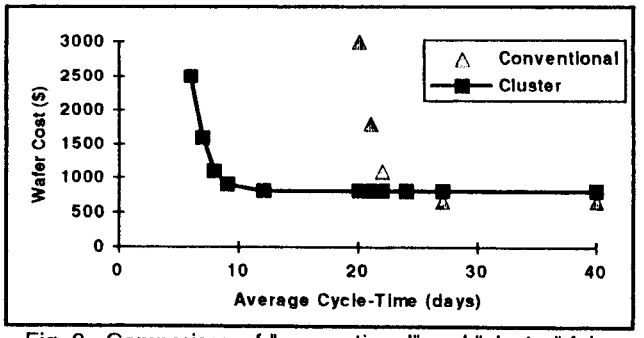

Fig. 2. Comparison of "conventional" and "cluster" fabs

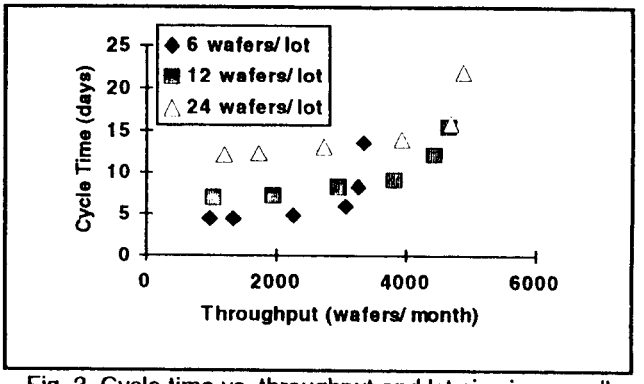

Fig. 3. Cycle-time vs. throughput and lot size in a small "cluster-tool fab"

Even though the "cluster" fab uses all single wafer tools, its operating characteristics are still very sensitive to "lot size," which determines the degree of "pipelining" as the wafers are processed through the individual steps. Figure 3 illustrates the influence of lot size on the tradeoff between throughput and cycle-time. All of the tools required for such a fab are not yet commercially available. However, the trends in single-wafer processing are consistent with the opportunity for such facilities within this decade.

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1-3 (Invited)

Technology Trend of Flash-EEPROM
— Can Flash-EEPROM overcome DRAM? —

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ABSTRACT

Flash EEPROMs will stir additional progress in semiconductor memories.While DRAMs play a key role in computer memories,they cannot replace hard and floppy disks-but Flash EEPROMs can,so markets for these devices may grow larger than DRAM markets.

INTRODUCTION

In 1971,Intel of the UNITED STATES introduced the i-1103 1k-bit DRAM as the first semiconductor memory to replace magnetic core memories. Before then, computor main memories always consisted of magnetic memories, but Intel's DRAM featured dramatically better performance than magnetic core memories. With access speeds thousands of times faster than magnetic core memories, the 1k-bit DRAM occupied hundreds of times less space and suffered hundreds of times less power loss. Within several years, DRAMs completely replaced magnetic core memories in computors. In 1991, 20 years after Intel released the 1k-bit DRAM, the semiconductor industry began mass-producing 4M-bit DRAMs.

Figure 1 illustrates the market scale for different kinds of memory devices along the horizontal axis and the performance of each device along the vertical axis. As the main memory device, DRAMs reach an international market scale of ¥ 1 trillion.

The progress in DRAM technology from 1k-bit in 1971 to 4M-bits in 1991 substantially affects everyday life.

Applications Among Magnetic Disks

Compared with the DRAM market,the markets for hard and floppy disks are several times larger.Magnetic storage media remains a compelling force in the memory industry because this format offers two crucial features not available with

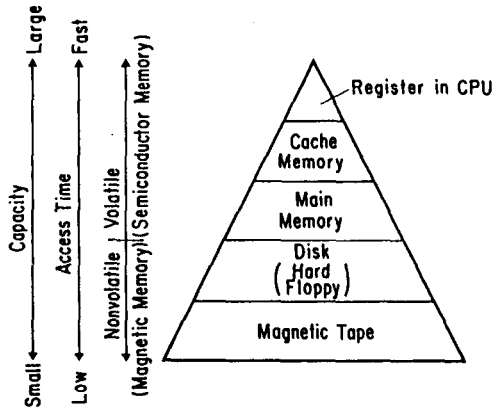

Fig.1 Hierarchy of the memories in a computer system

semiconductor memories.First,magnetic media memories are nonvolatile:they retain stored data even when the power goes off.DRAMs are a volatile medium,losing data when the power shuts down. Secondly,magnetic media products offer a low cost-per-bit.

In an attempt to develop a non-volatile semiconductor memory. F.Masuoka presented Flash-EEPROM at IEDM in 1984. Flash EEPROMs can replace hard and floppy magnetic disks.As the first general-use memory device from Japanese manufacturers,flash EEPROMs hold the key to enormous market expansion.

FLASH EEPROM

In 1971, Intel introduced an EPROM that used ultraviolet processes for the erase function; this model was known as FAMOS. Since then, as Figure 2 shows,manufacturers have developed a number of non-volatile memories with floating gates. The top portion of Fig.2 outlines Intel developments, while the bottom portion depicts Toshiba developments. In 1972,Toshiba offered a two-layer, polysilicon EPROM it called SAMOS. This model contrasted with the one-layer polysilicon FAMOS.

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