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ICMTS 94

PROCEEDINGS OF THE 1994 INTERNATIONAL CONFERENCE ON MICROELECTRONIC TEST STRUCTURES

March 22-25, 1994

San Diego, California

SPONSORED BY THE IEEE ELECTRON DEVICES SOCIETY

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CHAIRMAN'S LETTER

Dear Colleagues:

It is my pleasure to welcome you to the 1994 International Conference on Microelectronic Test Structures (ICMTS'94) sponsored by the IEEE Electron Devices Society.

This conference brings together designers and users of test chips from all over the world to discuss recent developments and future directions regarding the design, measurement, and application of microelectronic test structures.

The technical program chaired by Robert Ashton of AT&T Bell Labs is comprised of 42 papers, divided into nine sessions. The poster session chaired by Anthony Walton of the University of Edinburgh will include an oral summary of each poster paper. This year's exhibit program chaired by Jim Reedholm of Reedholm Instruments will be different from other ICMTS Conferences in that each company will give a 5 minute oral presentation following session IV describing their recent products and technology in addition to the equipment exhibition in the Aviary Ballroom.

Martin Buehler of JPL will chair the one day Tutorial Short Course that will overview the main topics in the field of microelectronic test structures.

The conference banquet on Wednesday evening will be a Mexican Fiesta aboard the William D. Evans cruising Mission Bay with the wonderful sound of Mariachis providing everyone an opportunity to renew old friendships and make new ones.

The 1994 IEEE ICMTS Conference Committee sincerely looks forward to seeing you in beautiful San Diego and we hope you enjoy the 1994 IEEE ICMTS Conference.

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General Conference Chairman

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IEEE INTERNATIONAL CONFERENCE ON MICROELECTRONIC TEST STRUCTURES

Nara, Japan **March 23-25, 1995**

IEEE

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The IEEE Electron Devices Society is sponsoring the 1995 International Conference on Microelectronic Test Structures to be held in cooperation with The Institute of Electronics, Information and Communication Engineers, and The Japan Society of Applied Physics. The purpose is to bring together designers and users of test structures to discuss recent developments and future directions. The Conference will be held at the New Public Hall in Nara on March 23-25, 1995. The Conference will be preceded by a one-day Tutorial Short Course on Microelectronic Test Structures on March 22. There will be an equipment exhibition relating to test structure measurements. Original papers presenting new developments in both silicon and gallium arsenide microelectronic test structure research, implementation, and application are solicited. A Best Paper Award will be presented by the Technical Program Committee. Suggested topics include:

Test Structures for Material & Process Characterization
- Carrier Transport Parameters
- Silicon-On-Insulator Material Evaluation
- GaAs Wafer Fabrication
- Polysilicon and Amorphous Silicon Films

Dimensional & Electrical Integrity of Replicated Features
- MOS Effective Gate Length
- Level-to-Level Registration
- Interconnect System Functionality
- Non-Electrical Techniques

Test Structures for Device & Circuit Modeling
- Modeling Parameter Extraction
- Radiation Hardness Modeling
- Monolithic Microwave Integrated Circuits
- High Frequency Measurement Techniques

Product Failure Analysis from Test Structure Data
- Failure Identification and Mapping
- Machine-Assisted Diagnostics
- Latchup, Soft Error, and Total Dose Effects

Test Structures for Reliability Analysis
- Time-Dependent Dielectric Breakdown
- Wafer-Level Fast Tests
- Electromigration
- Hot-Carrier Injection
- Thermal Monitoring and Analysis

Wafer Fabrication Process Control Test Structures
- Process Uniformity and Worst-Case Analysis
- Wafer Screening and Yield Enhancement
- Experimental Design
- Yield Modeling and Statistical Process Control

Test Structure Measurement Utilization Strategy
- Database Management
- Test Equipment and Programmable Testing
- Expert System and Related Techniques
- Test Structures for Quality Assurance

Paper Submission

Authors are asked to submit for review 36 copies of a 500- to 1000-word summary, a title page, major figures, and data. These should reach the ICMTS95 secretariat by Thursday, **August 18, 1994**. The title page must include a five-line abstract, the full address and FAX number of the lead author, and author preference for oral or poster session presentation. The selection process will be based on technical merit and will be highly weighted in favor of papers that include measurement data and their analysis. Notices of paper acceptance with instructions for manuscript preparation will be sent to authors of papers selected for presentation by Friday, **October 28, 1994**. Camera-ready copy will be required from the authors for inclusion in the Conference Proceedings by Monday, **January 9, 1995**.

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A Global Optimization of Bipolar Model Parameters Using Simulated Diffusion

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Abstract **- In this paper, a novel parameter extraction algorithm based on the modified simulated diffusion (SD) is presented. The utility of this program is demonstrated by applying it to the parameter extraction of a 40V bipolar transistor and a 2 um polysilicon emitter bipolar transistor. It is the first time that dc and ac bipolar model parameters have been extracted simultaneously via the global optimization methodology using the SD. Indeed this tool, supported by an excellent agreement between the measured and simulated data, is a powerful means for the modeling of any devices.**

I. INTRODUCTION

Traditionally the bipolar SPICE model parameters used for circuit simulations have directly been extracted as proposed by I. Getreu [1]; the linear curve fitting to the measured data is performed based on the approximation of model equations. As device models have been evolved to account for nonclassical effects such as the emitter crowding, non-ideal base current, and quasi-saturation, the direct extraction of the model parameters has become almost impossible. For these sophisticated device models, the nonlinear least-squares optimization techniques such as the gradient-based Levenberg-Marquardt (L-M) method have typically been used in the commercially available parameter extraction tools like TECAP and UTMOST. However they have raised the tackling problems that they can easily be trapped in local minima unless good initial values are available and thus give nonphysical or nonunique values even though the fittings are relatively good for all measured data. In these tools the step by step procedures to find good initial values for each model parameters have been pursued to overcome these disadvantages.

Recently a method called simulated diffusion (SD), inspired by simulated annealing (SA) [2], has been proposed as a highly reliable one to seek the global minimum [3],[4]. Simulated annealing, a combinatorial optimization method successfully used in image processing and standard cell placement in integrated circuit layout, has been introduced to extract the SPICE model parameters [5]. Although SD does not require any initial values inherently, it always yields the consistent results. Therefore SD is a promising choice for statistical modeling, in which the model parameters are required to be statistically consistent and physically reasonable. Even though SD approach takes a longer CPU time than L-M method, It is comparable to L-M because L-M method requires a lot of time to search good initial values. Sakurai *et al* [6] proposed the fast simulated diffusion (FSD) algorithm to improve speed, which was demonstrated by the application to MOS transistors.

In this paper, the modified SD algorithm is presented to improve the efficiency. Basically we adopted the fast SD algorithm and modified it by introducing the equilibrium condition and the one dimensional gradient search routine to further improve the efficiency. This modified SD has been implemented into CASPER (Characterization And Spice Parameter Extraction pRogram), which is operated in UNIX environment and has X-window/Motif graphic routines to show data. It is interfaced to HSPICE [7] with IPC (Inter-Process Communication). We applied it to the parameter extraction of a 40V bipolar transistor and a 2 um polysilicon emitter bipolar transistor, based on the extended Gummel-Poon model (HSPICE Level 2) accounting for quasi-saturation effects predicted by Kull *et al* [8]. For a 2 um polysilicon emitter bipolar transistor both dc and ac model parameters have been extracted simultaneously via the global optimization methodology using SD.

II. THE MODIFIED SIMULATED DIFFUSION ALGORITHM

The goal in this optimization is to minimize the objective function, which is defined as

$$f(x) = \sum_{i=1}^{n} weight * \frac{| D_m - D_s |}{min (D_m , D_s)} \qquad (1)$$

where x is the model parameter; n is the number of the measured data; *weight* is a weighting factor, which can be selectively defined; D_m and D_s are the measured and simulated data. The SD employs a stochastic approach to describe a diffusion process of a particle with Brownian motion, which can be expressed as

$$dx = -\nabla f(x)\, dt + \sqrt{2T}\, dw \qquad (2)$$

where t is time; x is the model parameter; $f(x)$ is a objective function; dw is a Brownian motion; and T is temperature. At each iteration the gradient and the random terms in (2) are alternately selected. Gauss-Newton method, an one dimensional gradient search algorithm with first derivatives, is adopted in calculating the gradients of the function because it is simple and fast. For generating the random term, one parameter is arbitrarily selected and then modified by sampli-

ng a random number from the Cauchy probability density function (PDF) instead of the Gaussian PDF. It is known that the tails of the Cauchy distribution are asymptotically much larger than any corresponding Gaussian. This means that the Cauchy distribution can give the higher possibility of long jumps to escape from local minima.

The modified parameter set is then tested. The decreasing set of the objective function is always accepted, while the increasing set is conditionally accepted depending on the probabilistic evaluation result of the Boltzman distribution function. The probability of acceptance is determined by the temperature T, a control parameter at the iteration steps, which is gradually decreasing by the temperature cooling schedule [9]. The modified SD algorithm is shown in Fig. 1. In initialization scheme a lot of (~200) randomly generated parameter sets within the given bounds are evaluated, and the initial temperature is calculated from the standard deviation of the objective function. The parameter is then obtained between the minimum and maximum bounds, and the volume of the parameter bounds becomes shrunk in proportion as the temperature is lowered. Although the initial values of the parameters are not required, the minimum and maximum values for the parameter bounds are needed to generate the random parameters. These bounds also have the effect on the speed of convergence. The final solution is sometimes not guaranteed to be better than the intermidiate ones. As the SD process progresses, the best parameter set in a series of the randomly perturbed ones is stored and later recovered in updating temperature if a better solution does not appear. The equilibrium condition and the stopping criterion follow the previous work [9]. The adopted equilibrium condition improves the convergence speed by cutting down the Markov chain-length at high temperatures. Stopping criterion includes both user definable RMS (Root Mean Square) error and maximum error.

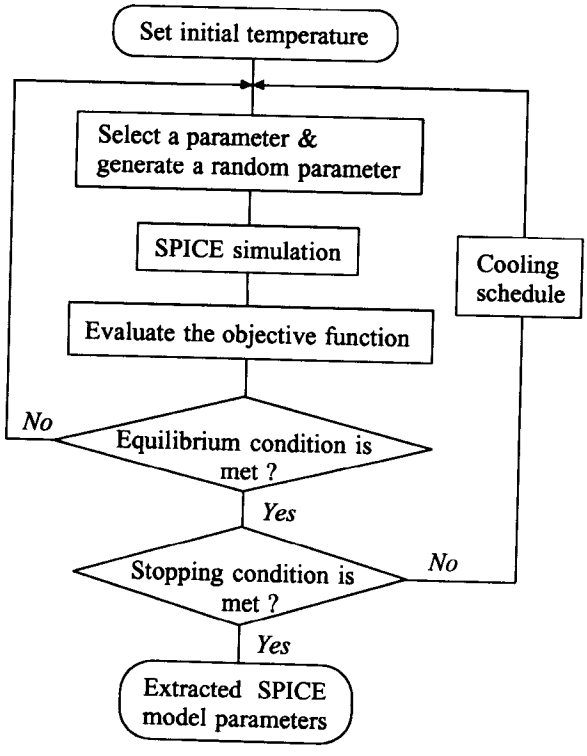

Fig. 1. The modified simulated diffusion algorithm

III. CASPER CONFIGURATION

The modified simulated diffusion algorithm has been implemented into a program called CASPER, which is operated in UNIX environment and has the X-window/Motif graphic routines to show data. In Fig. 2 CASPER configuration is shown. It includes the device drivers to control the following measurement equipments: a dc semiconductor parametric analyzer, a network analyzer, an LCR meter, a switch matrix, a thermochuck system, and an auto prober. Also it has capability of managing data files. It is written in C programming language and can easily be ported to any platform.

The commercially available parameter extraction tools provide their own SPICE models. Consequently their results are often a little different from those of HSPICE or PSPICE widely used. Furthermore there is a need to respond to the updated models. Taking these facts into consideration, CASPER is externally interfaced to HSPICE with IPC (Inter-Process Communication), in which a pipe is constructed for data reading and writing. CASPER has the flexibility to handle all the models in HSPICE and is able to incorporate an updated model by just defining a model file that has the parameter names and their bounds.

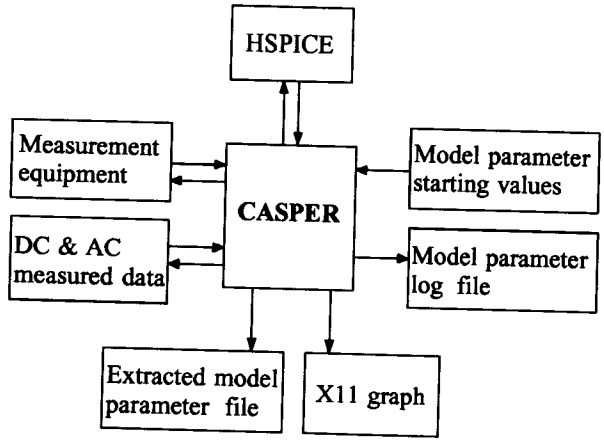

Fig. 2. CASPER Configuration

IV. APPLICATION TO BIPOLAR MODEL PARAMETER EXTRACTION

The CASPER program has been applied to the extraction of bipolar SPICE model parameters. For a benchmarking of the tool, the extended Gummel-Poon model (HSPICE Level 2) accounting for quasi-saturation effects described by Kull *et al* is chosen. Their model, although it is not widely used, is also known to be able to account for the substrate currents of the bipolar transistor in saturation as well as quasi-aturation regions, which enables the accurate prediction of the overall

circuit performance. Actually it is difficult to obtain a good fitting to all the measured data by using the conventional L-M method since there is no exact ways to find good initial values of the model parameters. HSPICE provides an additional model parameter, NKF, which acts as an exponent of base charge (Q_B) and allows us to adjust the slope of the log (β_F) curve. For NKF=0.5 the standard SPICE bipolar model is obtained. Typically NKF lies in the range of 0.5~0.9.

DC data contains Gummel (Ic, Ib & Is vs. Vbe) and output (Ic & Is vs. Vce) characteristics at Vs= -5.0V. Junction capacitances (Cje, Cjc & Cjs) were obtained from C-V measurements. Magnitude and phase data of all four s-parameters were collected by de-embedding the parasitics of RF probe pads and interconnections (probe-pattern) from the measured data of network analyzer HP8510B. The temperature of the device was maintained at 25 ℃ (298.15K) during measurements, which is a nominal temperature in HSPICE. It is known that the temperature has a significant effect on bipolar parameter extraction. In this experiment we nearly obtained an ideal value of NF, which is close to one.

For DC data a noise cancelling technique based on a fast fourier transform (FFT) was used to get a stable fitting in a low current range (<10nA) by filtering noisy (high frequency) data. Noisy data affects the base current model parameter in a low current region , ISE and NE. From the comparison of the measured data with/without noise cancellation in Fig. 3, it is obvious that our method is quite effective in cancelling noisy data and then guarantees the stable fitting to the measured data.

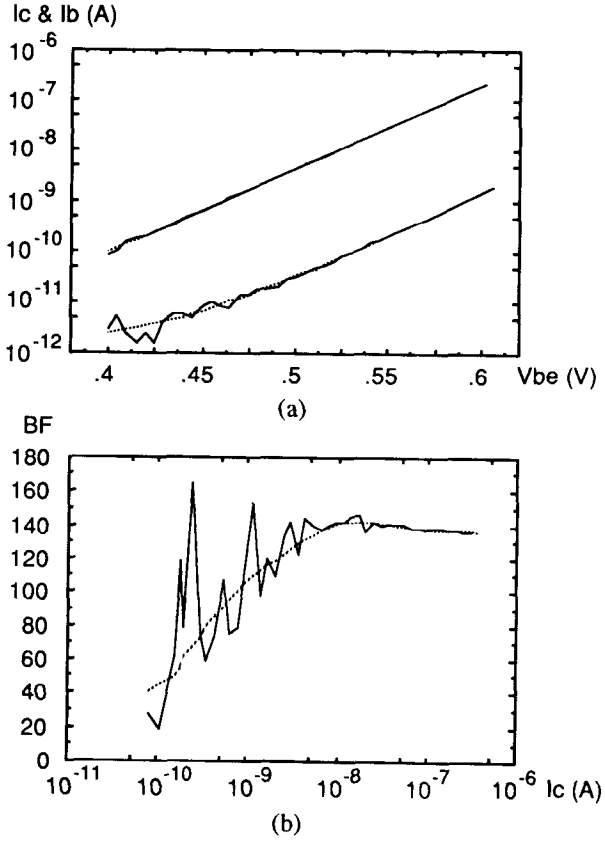

Fig. 3. Noise cancelling in the low current region of forward Gummel by using a fast fourier transform algorithm. Note the measured (solid line) and noise cancelled data (dotted line).

In the parameter extraction procedure using the L-M method good initial values are essential. In the modified SD program, on the other hand, initial values are not necessary. The maximum and the minimum values for the model parameters are only needed to improve the convergence speed. It is easy to define those boundary values because they are almost known.

Bipolar DC characteristics are described by 18 parameters : IS, ISE, NE, BF, BR, VAF, VAR, IKF, IKR, NKF, RB, IRB, RBM, RE, RC, VO, BRS, GAMMA, and NEPI. The quasi-saturation model parameters are VO, BRS, GAMMA, NEPI, and RC for DC and QCO for AC. AC model parameters consist of QCO, CJE, CJC, CJS, XCJC, TF, ITF, VTF, XTF, and PTF.

At first, we seperated DC and AC parameter extraction process. All DC characteristics were used for DC model parameter extraction. The emitter resistance was determined from open-collector method [1] for simplicity. For AC parameter extraction the magnitude and phase of all four s-parameter data were used in the objective function. We used the L-M method to extract the model parameters for junction capacitances (CJ, VJ, MJ), which are quite important in AC modeling and described as simple analytical equations, because it is simpler and faster in this case. Among the model parameters for junction capacitances CJE, CJC, and CJS were involved in AC parameter extraction. Their physical meaning was kept by varying the junction capacitance values at zero bias within 10% of the values obtained from C-V measurements. Finally the global optimization was perfo-rmed for both DC and AC measurement data. We focused on the model parameters related to the base resistance (RB, IRB, RBM), since it has the great effect on both DC and AC characteristics. As the stopping criterion we added the follo-wings: The RMS errors are below 5% for DC and 15% for AC respectively, and the maximum errors are below 15% for DC and 30% for AC. AC and DC model parameters are accomodated during the global optimization in which the DC and AC measured data are simultaneously used in the objective function.

V. Extraction of Bipolar Model Parameters

A. Experimental results for a 40V bipolar NPN transistor

This bipolar technology is used for analog applications requiring 40V power supply. Fig. 4 shows (a) forward Gummel (Ic, Ib & Is vs. Vbe at Vbc=0V), (b) beta, (c) output characteristics (Ic vs. Vce at Vbe=0.775, 0.798, 0.813, 0.825 V), and (d) the substrate current in output characteristics (at the same bias of (c)) of a NPN transistor featuring the emitter size of 10 um x 10 um. The transistor certainly revealed the quasi-saturation effects in forward Gummel and output characteristics due to low doping level of the collector. In the modeling of the substrate current it is not easy to obtain a good fitting even in Gummel plot with the L-M method. On the other hand, our SD shows a good fitting of the substrate current in both Gummel and output characteristics. In Fig. 4 the excellent agreement between the measured and simulated data is observed over full DC regions. The complete fit

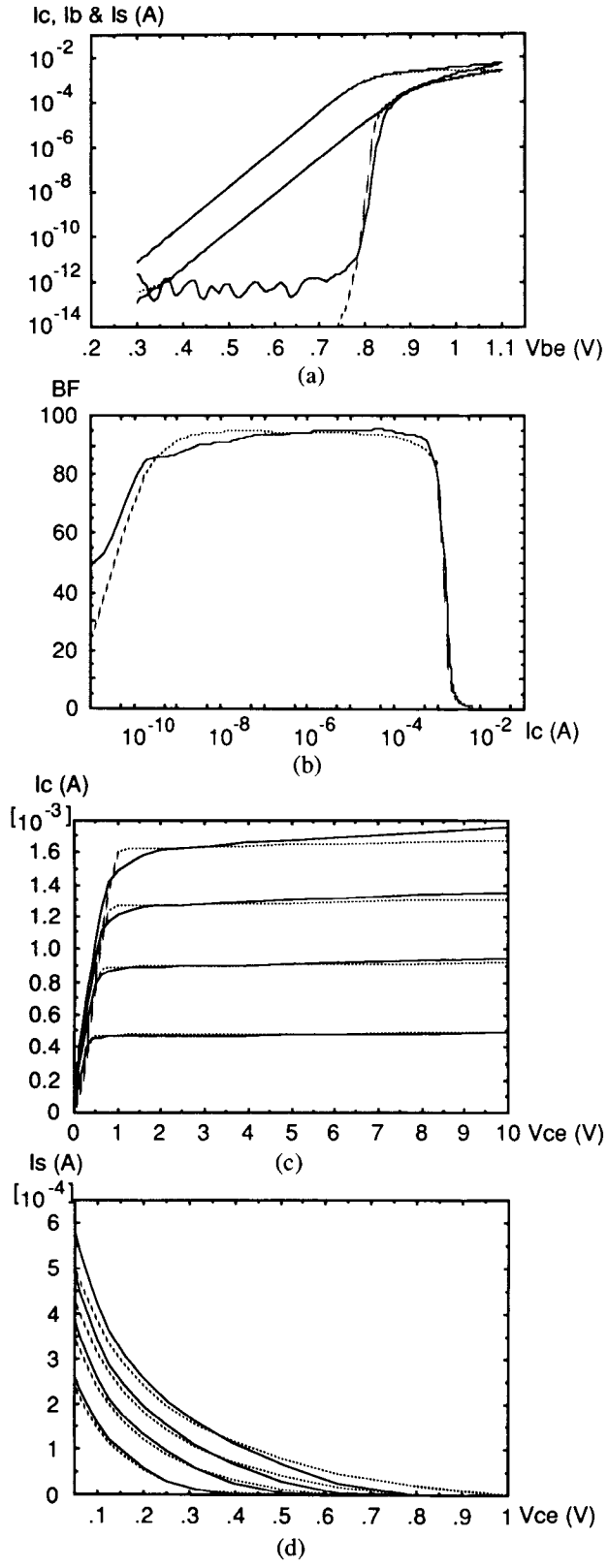

Fig. 4. Note the measured (solid line) and simulated (dotted line) data of (a) forward Gummel, (b) forward current gain, (c) output characteristics, (d) substrate current (Is vs. Vce) for a 40V bipolar NPN transistor. The RMS and maximum errors are below 5% and 15% respectively.

Table 1. List of the extracted parameters in a 40V and a 2um bipolar technology using the modified SD program

Parameter	40V bipolar NPN Tr.	2um bipolar NPN Tr.
IS	5.66e-17	1.91e-17
ISE	2.59e-17	7.87e-13
NE	2.55e+1	1.53e+1
BF	97.2	175.4
BR	3.65	0.97
VAF	229.4	58.1
VAR	20.5	2.69
IKF	1.59e-2	1.35e-2
NKF	0.8	0.716
RB	1.48e+3	2.6e3
RBM	21.9	34.55
IRB	1.75e-5	2.07e-5
RE	5.4	12.45
RC	3.94e+2	64.01
VO	5.81	4.52
BRS	2.05e+1	3.81
GAMMA	5.36e-14	8.22e-12
NEPI	1.037	1.036
QCO	–	1.686e-9
CJE	–	4.40e-14
CJC	–	4.42e-14
CJS	–	1.60e-13
XCJC	–	9.198e-2
TF	–	2.475e-11
ITF	–	1.35e-2
VTF	–	1.058
XTF	–	9.629
PTF	–	10.0

requires about 3 hours for DC of CPU time on HP730 computer. The iteration numbers are 6350. Extracted model parameters are listed in Table. 1.

B. Experimental results for a 2 um polysilicon emitter bipolar technology

The minimum size NPN transistor for a 2 um polysilicon emitter bipolar technology, dedicated to analog and digital applications requiring a 5V power supply, has been considered. The cutoff frequency of this device is 6 GHz (Vce =3V), and the emitter size is 2 um x 6 um.

In Fig. 5 all DC characteristics including forward Gummel (at Vbc=0), beta, output characteristics (at Ib=4, 8, 12, 16uA), and the substrate current in output characteristics show the good correspondence between the measured and simulated data. In Is vs. Vce the substrate current reveals a little discrepancy because Kull's model cannot account for the non-ohmic quasi-saturation effects associated with the current-induced space-charge-region in the epitaxial collector. In Fig. 5 the good agreement between the measured and simulated data is observed for the magnitude and phase of s12 and s21 among four s-parameter sets (at Vbe=0.75, 0.8, 0.85, 0.9, 0.95 and Vce=3). In Fig. 7 is shown the magnitude of h21 and the cutoff frequency calculated from the magnitude and phase of four s-parameter data. The complete fit requires typically 3.5 and 2 hours of CPU time on HP730 computer for DC and AC cases respectively. The iteration numbers are 7030 for DC and 3250 for AC. Extracted model parameters are listed in Table. 1.

VI. Conclusions

The global optimization algorithm based on the simulated diffusion has been presented for the first time and applied to the parameter extraction of bipolar transistors. The utility of our parameter extraction tool was demonstrated by an excellent agreement between the measured and simulated data of nominal biploar junction transistors. We also would like to emphasize that the physical meaning of each model parameters has not been lost because of the physical nature of our algorithm. This means that the modified SD program is fairly effective to find the global minimum and can be successfully applied to any other devices.

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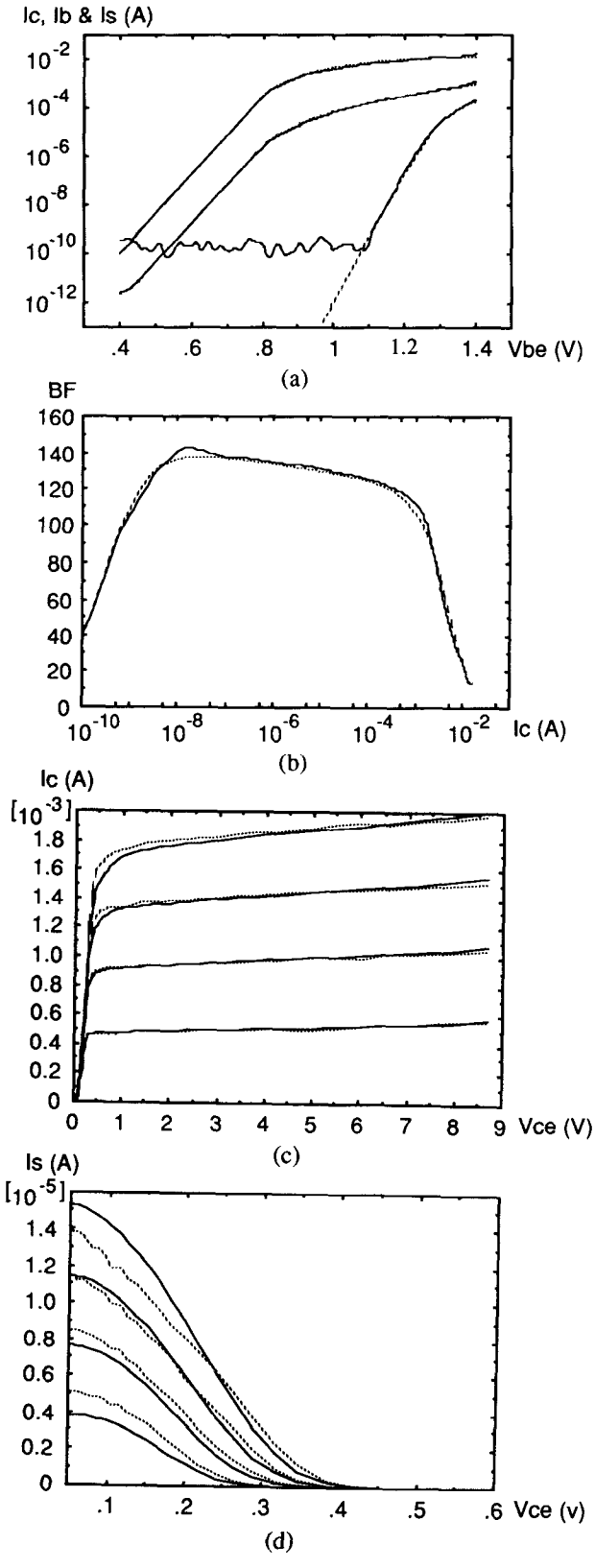

Fig. 5. Note the measured (solid line) and simulated (dotted line) data of (a) forward Gummel, (b) forward current gain, (c) output characteristics, (d) substrate current (Is vs. Vce) for a 2um bipolar NPN transistor. The RMS and maximum errors are below 5% and 15% respectively.

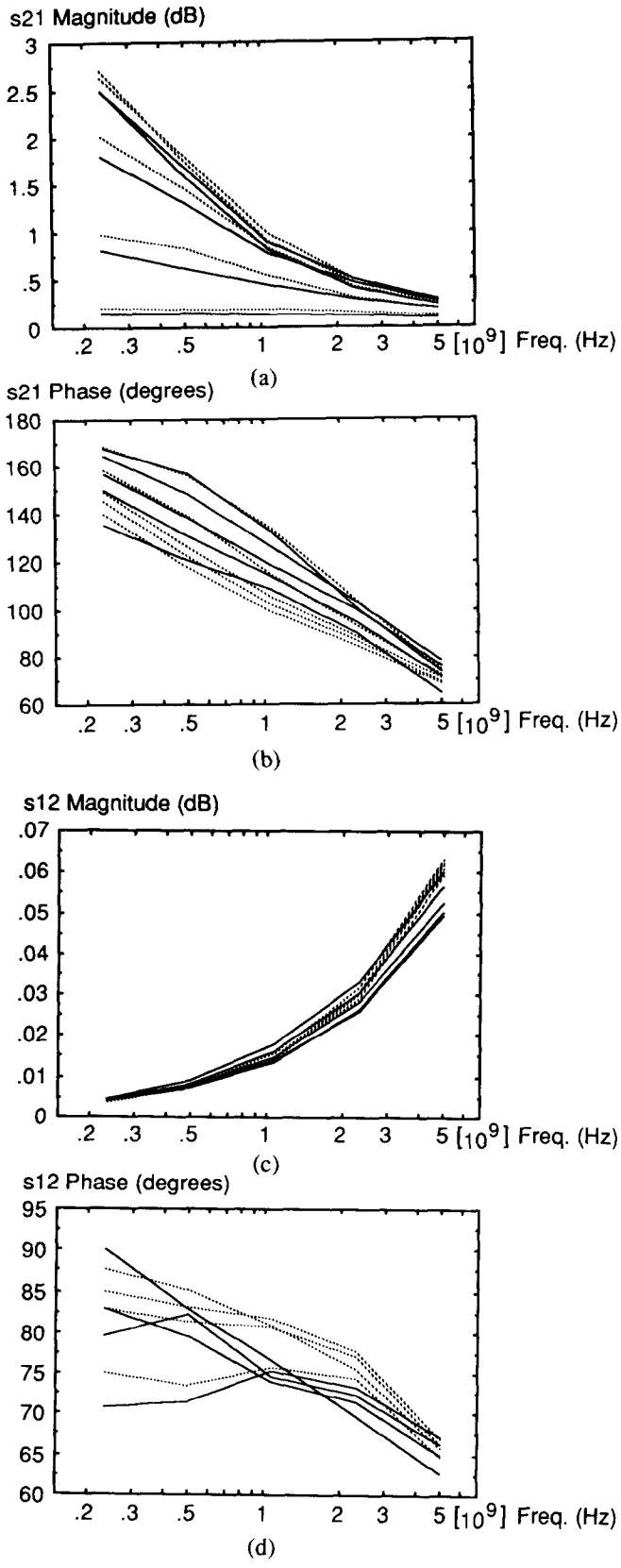

Fig. 6. Note the measured (solid line) and simulated (dotted line) data of (a) s21 magnitude, (b) s21 phase, (c) s12 magnitude, (d) s12 phase for a 2um bipolar NPN transistor. The RMS and maximum errors are below 10% and 30% respectively.

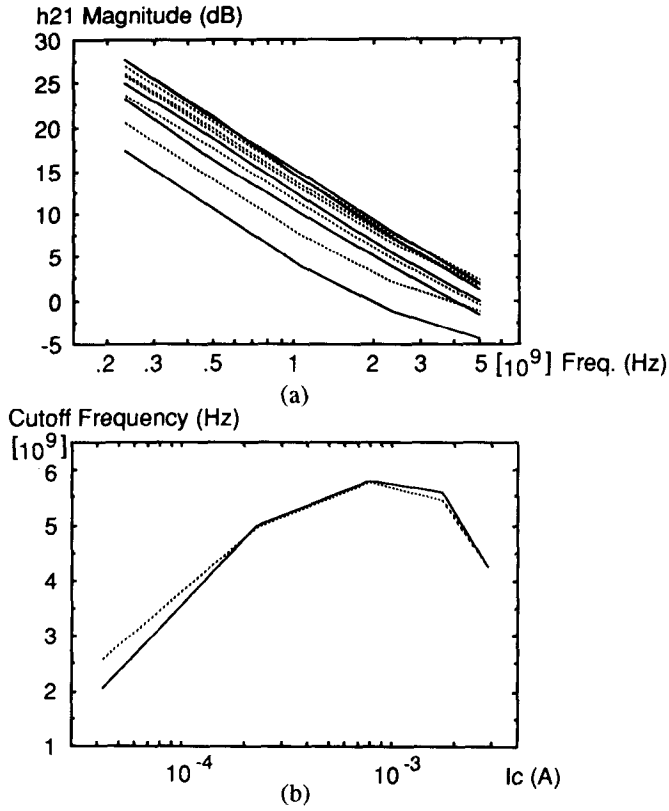

Fig. 7. Note the measured (solid line) and simulated (dotted line) data of (a) h21 magnitude, (b) cutoff frequency for a 2um bipolar NPN transistor.

Fast and Accurate On-Wafer Extraction of Parasitic Resistances in GaAs MESFET's

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Abstract — A new and accurate method for extracting parasitic resistance values of GaAs MESFET's is presented. The technique makes use of only three simple DC measurements. Simulation and measurement results show that this new extraction method is very accurate compared to other currently used methods [1-6]. As the same test device can be used for full characterisation of the MESFET's, this method does not require additional test structures. Using our extraction method, excellent agreement between simulated and measured S-parameters for a small-signal equivalent circuit MESFET model was found, so it is very appropriate for device and circuit modelling purposes. The presented extraction method is implemented in HP-ICCAP, a software tool for parameter extraction. In addition, all the measurements are controlled by this software, so a high level of automation is obtained.

INTRODUCTION

Fast and accurate parameter extraction for modelling high frequency MESFET devices is needed to design, develop and produce high yield, low cost microwave circuits. It should be stressed that device characterization, parameter extraction and device modelling are three very closely related processes [7]. In order to make accurate circuit simulations, it is therefore not only important tot use accurate device models, but it is as equally important to perform accurate device measurements and to use accurate extraction routines to obtain the necessary model parameters. One has to be aware that the accuracy of a parameter extraction routine is dependent on the characterization method and the device model being used. The extraction routine that we present in this paper must be considered in this context.

We present an extraction method to retrieve accurate parasitic resistance values for the non-linear Statz MESFET model [8] based on a DC characterization of the device. The method is also valid for other MESFET models that have the same topology as the Statz MESFET model. Several methods for extracting these parasitic resistance values have already been published [1-6]. They make use of DC or S-parameter measurements, out of which three relations are obtained between the three unknown parasitic resistances. There is however a discrepancy between the different methods [1-6], because none of them gives the same result, although these resistances must be represented by only one value in the model. The method we present here solves this problem.

Extracting the parasitic resistances separately, before the other model parameters are extracted, is an important step in the parameter extraction strategy for the Statz MESFET model, because it reduces the number of element values which require a final optimization. This enhances the speed and accuracy of the extraction process. The parasitic resistance values can also be used for deembedding of the device under test, in order to obtain the intrinsic terminal voltages of the MESFET, which simplifies the extraction of the intrinsic MESFET model parameters. It is obvious that an error on the resistances will lead to a substantial error on those intrinsic model parameters.

THEORY

Figure 1 shows the non-linear Statz MESFET model that is available in most commercial circuit simulators. The model has three dominant non-linearities: the transconductance I_{ds}, the gate-source capacitance C_{gs}, and the gate-drain capacitance C_{gd}, which are expressed in terms of the intrinsic gate to source and drain to source voltage. If we are able to determine the parasitic resistances and inductances of this model independently, we can derive the intrinsic voltages from the measured external voltages and currents, and this would simplify the extraction of the other 10 intrinsic model parameters.

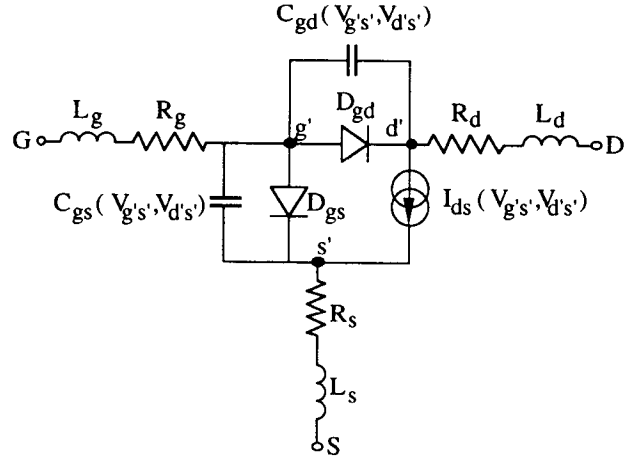

Figure 1: The non-linear Statz MESFET model

Figure 2 depicts the equivalent DC circuit model of a MESFET as it is derived from the model in figure 1. The model includes the parasitic resistances of the gate, the source and the drain, two diodes representing the gate-channel

Schottky junction, and the channel resistance. Since the model does not include a transconductance, it only applies to cold-FET (V_{ds} = 0V) operation. The two diodes are assumed to be identical, and are modelled by the well-known Shockley equation:

$$I = I_{sat}.[\exp(\frac{V}{n.V_t})-1] \quad (1)$$

The reverse saturation current I_{sat} and the ideality factor n can be accurately determined from a forward diode measurement [1]. V_t is the thermal voltage kT/q which is 26mV at room temperature.

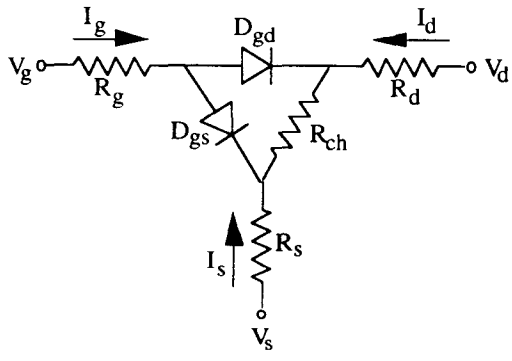

Figure 2: DC equivalent circuit model for a GaAs MESFET

Figure 3 shows the first measurement set-up, where a current I_g is forced through the gate while the intrinsic drain to source voltage is forced to zero by a second current source of $I_g/2$ at the drain. This means that, following the model of figure 2, no current flows through the channel resistance, so

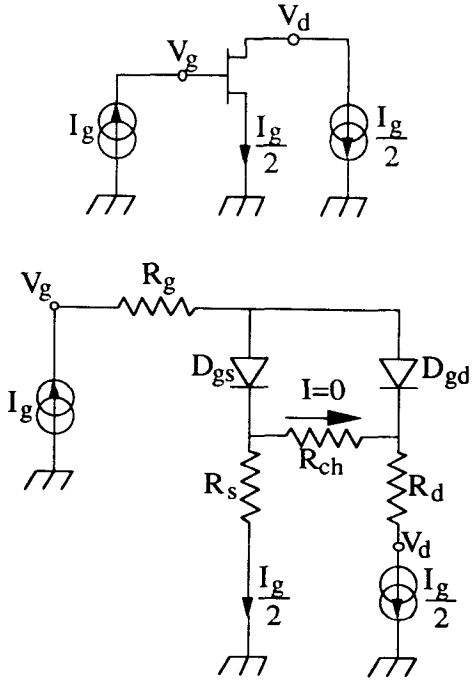

Figure 3: First DC measurement set-up

R_{ch} does not have to be determined, nor does it have to be neglected. The voltage at the drain is proportional to the difference between the source and drain resistance.

From the voltages measured at the drain and the gate, and from eq. (1) and Kirchoff's voltage law, the following relations are obtained:

$$R_d + \frac{2V_d}{I_g} = R_s \quad (2)$$

and

$$R_g + \frac{R_s}{2} = \frac{V_g - n.V_t.\ln(1+\frac{I_g}{2I_{sat}})}{I_g} \quad (3)$$

In the low current region of this measurement, where the voltage drop across the parasitic resistances can be neglected, we can extract the diode ideality factor n, and the reverse saturation current I_{sat}.

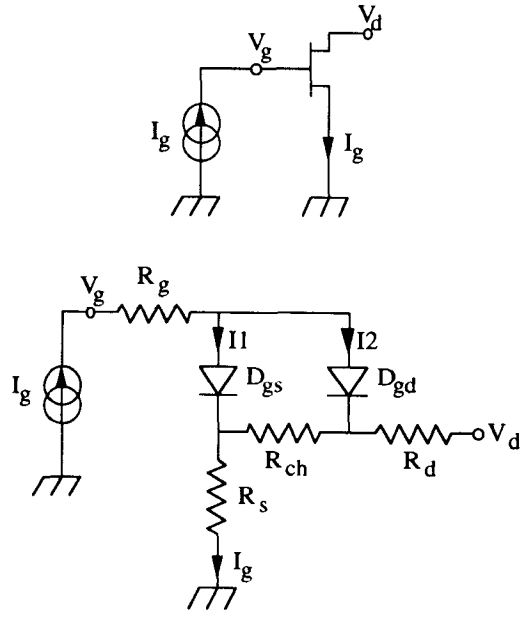

Figure 4: Second DC measurement set-up

Figure 4 shows a second measurement set-up, where again a current I_g is forced through the gate with the drain left open and the source connected to ground, so $I_s = -I_g$. Again, the voltages at the drain and the gate are measured. The currents through the two Schottky diodes are given by:

$$I_1 = I_{sat}.\left\{\exp\left[\frac{V_g-(R_s+R_g).I_g}{n.V_t}\right]-1\right\} \quad (4)$$

and