VLSI

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INTERNATIONAL SYMPOSIUM ON VLSI TECHNOLOGY, SYSTEMS, AND APPLICATIONS

PROCEEDINGS OF TECHNICAL PAPERS

IEEE Catalog Number: 01TH8517

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FOREWORD

The objective of the International Symposium on VLSI Technology, Systems, and Applications is to bring together scientists and engineers actively engaged in research and development on VLSI technology, systems, and applications from all over the world to discuss current progress in this field with the subject experts from Taiwan's local industry. The Organizing Committee for the 2001 VLSI-TSA has decided to shift the conference from the traditional June time frame to April, the beautiful spring season in Taiwan. We have also moved the conference location from Taipei to Hsinchu, the center of advanced integrated circuit design & manufacturing in Taiwan.

There are three keynote speeches delivered by the leading thinkers from the US, Europe, and Japan to position the theme of the 2001 VLSI-TSA on Systems and Complexities. The scaling of silicon technology provides the possibility of creating complete systems on one integrated-circuit chip. In "Systems on a Chip from a System's Perspective", Gene Frantz (Senior Fellow, Texas Instruments, USA) discusses the why, when and who of SOC to dramatically improve system level performance, cost and power. In "Future is in Wireless", Heikki Huomo (Vice President, Research and Technology Access, Nokia, Finland) details how wireless terminal manufacturers address the various design challenges in RF and baseband to ensure fast product creation with rapidly increasing system complexity in the Third Generation mobile communications systems for wireless Internet. Toyoki Takemoto (Executive Vice President, STARC, Japan) describes including the promotion of industrial/academic joint projects and pre-competitive R&D activities on circuits and systems in "Joint Activity for Semiconductor R&D and role of Semiconductor Technology Academic Research Center (STARC)".

Invited papers are the backbone of VLSI-TSA to set the stage for technical interactions. We are very fortunate to have the following six invited presentations in the technology area to discuss advanced technology trends and their optimization for various applications: Ghavam Shahidi (IBM) on "SOI Technology for GHz Era", Bunji Mizuno (Matsushita) on "Ultra Shallow Junction Doping Technology for Sub-100nm CMOS", Kinam Kim (Samsung) on "1T-1C FeRAM Technology", David Bishop (Lucent) on "Silicon Micromachines for Lightwave Networks: Can Little Machines Make It Big?", Joachim N. Burghartz (Delft University of Technology) on "Tailoring Logic CMOS for RF Applications", and M. Houssa et al. (Katholeike Universiteit Leuven and IMEC) on "Electrical and Physical Characterization of High-k Delectric Layers".

On the Circuits and Applications side, we have eight strong invited talks on advanced issued ranging from systems design to CAD methodology: Bob Brodersen (University of California, Berkeley) on "The Case against Software for System-on-a-Chip Design of Wireless Systems", Joseph Williams (Agere) on "Architectures for Network Processing", Kamran Azadet et al. (Agere) on "DSP Implementation Issues in 1000BASE-T Gigabit Ethernet", Josef Fenk (Infineon) on "Highly Integrated RF-IC's for GSM, DECT, and UMTS Systems - Status Review and Development Trends", Albert Theuwissen (Philips) on "CCD or CMOS Image Sensors for Consumer Digital Still Photography?", Paul Stravers et al. (Philips) on "Homogeneous Multiprocessing and the Future of Silicon Design Paradigms", Osamu Takahashi (IBM) on "High-Speed, Power-Conscious Circuit Design Techniques for High-Performance Computing", and Ward Vercuysse (Sun) on "CAD Infrastructure for High Performance Design".

The main contents of VLSI-TSA are the contributed papers. This year, the conference has attracted about 120 excellent submissions from all over the world, representing original works on the latest advances in the area of VLSI technology, circuits and applications. The Technical Program Committee has selected 66 papers for presentation with 33 in the Technology area and the same amount in the Circuits and Applications domain.

We like to thank the keynote, invited and contributed authors for their original and hard work. Appreciations are also extended to all the Technical Program Committee members for their efforts in reviewing and selecting the papers. We like to express special thanks to the Subcommittee Chairs for their great assistance with putting together an excellent technical program. Finally, we are most appreciative of the dedication and tireless efforts by Ms. Annie Lee in arranging all of details of this Technical Digest as well as the whole of 2001 VLSI-TSA.

Technical Program Committee Chair

Ran Yan
Bell Laboratories, Lucent Technologies

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System On A Chip: A System Perspective

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Texas Instruments Inc.
Houston, TX 77251

INTRODUCTION

Technology advances are providing us with an overwhelming capability to create new products that will impact the way we work, live, learn and play. Integrated circuits are getting smaller and at the same time are faster, lower cost and lower power dissipation. We are, at the same time, integrating more on to a single device. The ability to put a complete system on one device is now a practical option.

But, with the ability to create a complete "System On a Chip" (SOC) there comes the responsibility to do it wisely. The remainder of this paper will take a system's perspective of SOC. First, a quick look back at several examples of SOC. Then a discussion of why and how one should use SOC technology. Finally, a discussion on whom should design SOC.

EXAMPLES OF SOC

Over the last couple of decades, I have been part of many product developments that took advantage of the SOC concepts, as best that they could, at that time. The examples that I will use are the Calculator, modem and cellular phone.

Calculators

My first introduction to the concept of SOC was through my first job in TI's Calculator Division. The goal was, with out doubt, to do a single chip calculator: The whole system on a chip. Obviously, we made it. The calculator became four components: Keyboard, Display, Substrate and an Integrated Circuit.

This is a good point in the discussion to begin a working definition of SOC. The reason? It is obvious that we did not put the whole calculator on a single chip. We did not integrate the keyboard and display on the chip with the rest of the electronics. So, SOC, does not mean the whole system on a chip, but only a part of it. I guess this should be obvious.

Modems

The evolution of the modem is an example where SOC can be taken too far. The programmable Digital Signal Processor (DSP) was introduced to the modem industry at about the time of the 2400 bit per second modem, the V.22bis modem. From that point on, modems used DSPs and the data rates began to rapidly grow from 2400 to 9600, to 19.2K, 28.8K, 33.6K to 56K. Each new modem standard was effectively a new software program on a DSP platform. This isn't totally correct as new DSP platforms with higher performance also had to be created.

Each time a new standard was introduced to the market, it sold for about $200.00. As it became popular, its price was $150.00. At its peak of popularity, its price reduced to about $100.00. Then, finally, one manufacturer would declare victory with a SOC offering at $69.95. But, by then, the new standard had been introduced at $200.00.

This cycle occurred time after time. The manufacturers who made money were those who entered early. Those who entered late with a SOC solution didn't.

Cellular Phones

The latest example of SOC is the Cellular Phone. The demand for Cellular Phones is overwhelming. The number of units shipped is in the hundreds of millions per year. Such a run rate is certain proof for the need of a SOC solution; and, it has. The design has been reduced to a small number of devices. But it is still not a complete System on a Chip. Figure 1 is a picture of one of the chips in a Cellular Phone. It is the Digital Base band chip. It has on it a microprocessor, DSP, ASIC, Memory and some analog.

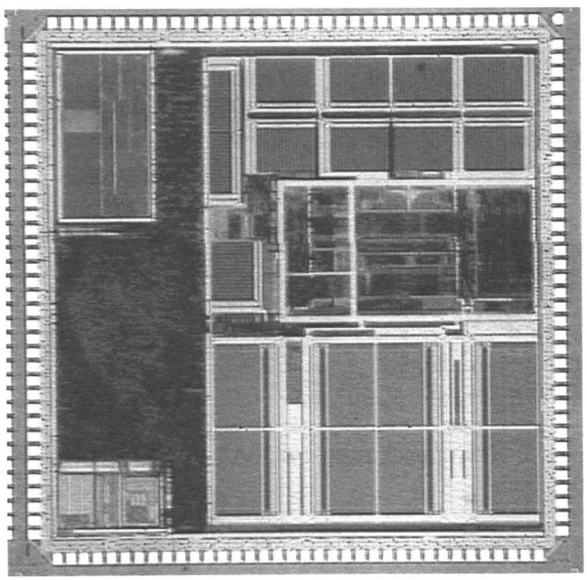

Figure 1. The Digital Base band device which is used in many Digital Cellular phone systems. It includes a microprocessor, DSP, ASIC, Memory and some analog .

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So, we might say that an additional aspect of SOC is that it does not require that the whole system be integrated be integrated on one device.

Now that we have looked at a few examples of SOC, I would like to look at why we should use SOC technology.

WHY USE SOC

There are many reasons for using SOC concepts. They include:

Increased system performance

Reduced system power dissipation

Reduced system cost

Smaller system size

System considerations

Seems like the right thing to do

I would like to look at each of these reasons, one at a time. First, I'll look at increased system performance.

Increased System Performance

System performance has had a long history of doubling every eighteen months. A colleague and I put together a chart about 10 years ago showing how the performance of Digital Signal Processors had progressed. We included a prediction based on the trend that we had seen. It looked a bit like Table 1.

	Typical 1982 DSP	Typical 1992 DSP	Typical 2002 DSP
Die size	50 mm	50 mm	50 mm
Technology	3μ	0.8μ	0.18μ
MIPS	5	40	2000
MHz	20	80	500
RAM	144W	1KW	16KW
ROM	1.5KW	4KW	64KW
Price	$150.00	$15.00	$1.50
Power/MIPS	250 mW	12.5 mW	0.1 mW
Transistors	50K	500K	5M
Wafer size	3"	6"	12"

Table 1. DSP trends from 1982 to 1992 with a projection to 2002.

This table was updated recently to not only correct our poor prediction of 2002, but to extend the prediction to 2010. Table 2 shows this update.

The interesting point to be made in this new prediction is that the DSP in 2010 will have a performance of fifty thousand MIPS with a die size of only 5 square millimeters. Assuming that we will easily be able to manufacture devices of 100 to 150 square millimeters, we will be able to put 20 to 30 of these DSPs on one device. This means that we will have devices with one trillion to 3 trillion instructions per second available.

	1980	1990	2000	2010
Die size (mm)	50	50	50	5
Tech (uM)	3	0.8	0.1	0.02
MIPS	5	40	5,000	50K
MHz	20	80	1,000	10K
RAM (bytes)	256	2K	32K	1M
Price	$150.00	$15.00	$5.00	$0.15
Pwr (mW/MIPS)	250	12.5	0.1	0.001
Transistors	50K	500K	5M	50M
Wafer size	3"	6"	12"	12"

Table 2. Updated performance trends of DSP devices.

Reduce System Power

As I will discuss later in the section on system considerations, power dissipation is becoming, if not already, a significant part of performance. Several years ago I plotted the power dissipation of DSPs to see what the trend would tell us about the past and future of DSP devices. The results of that study showed that the trend for power dissipation seemed to follow similar behavior to Moore's Law. What I found was the power dissipation, per MIPS, was reduced to half every eighteen months. I named this "Gene's Law" (see Figure 2).

At this rate of decrease, the power dissipation of DSPs will be in the order of 1 micro-watt per MIPS by the year 2010. This will change the way we look at products.

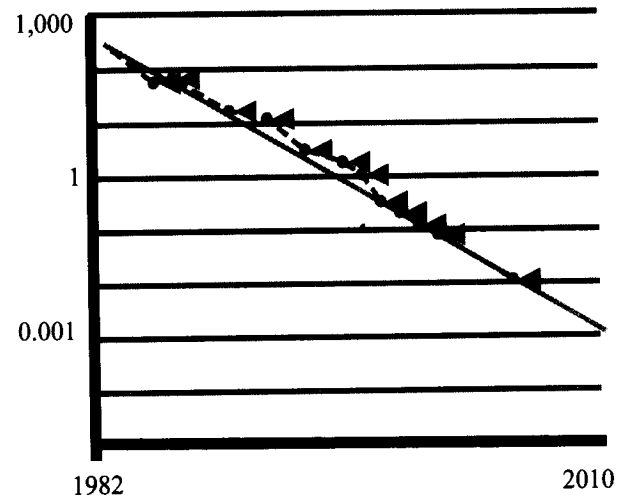

Figure 2. "Gene's Law". Power dissipation of DSP devices since 1982, in mW/MIPS. The trend line shows the power dissipation to decrease to one half power every eighteen months.

Smaller system size

At the same time performance is increasing and power dissipation is decreasing; the size of integrated circuits are also decreasing. At the same time, more is being put on the devices. The implication is that the size of products is also decreasing. But, before we get carried away with the idea of a cellular phone in the ear, or a video phone on our watch, we need to consider the size constraints at the system level.

In spite of our efforts in integrated circuit technology, hand held will remain the same size, the pocket will stay the same size, and even the desk top will maintain the same size constraints. So, the major impact on the size of the end product will not be the integrated circuits, but will be the human factors.

System considerations

Performance, power and size will not be the significant issues in creating new, innovative products that will impact society over the next decade. I believe that the major issues will be system level considerations. These issues can be summarized by three concepts:

The Three Vectors of Value

The Value of Time

The Value of Complexity

The big win of System On a Chip is the impact that it has had on three different vectors of value. These vectors are shown in Figure 3. They are Performance, Cost and Power. Each time we advance the state of the art of integrated circuit technology three things happen: 1) the performance of the device increases, 2) the power dissipation is reduced and 3) the cost of the device is reduced. Actually a fourth impact happens - ore can be integrated onto the same device. But, for the moment, I will focus on the first three.

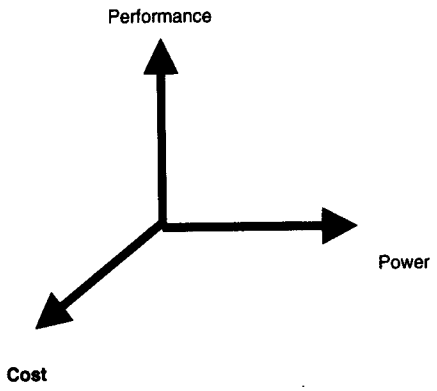

Figure 3. The three vectors of value in an integrated circuit.

Even though all three vectors are affected by advances in integrated circuit technology, at any one technology node, the three must be further optimized. It is easy to drive performance, but at the sacrifice of power and cost. In the same way it is easy to drive power, but at the sacrifice of performance and cost. And it is the same for cost.

Each of the three vectors find new business opportunities. For example, personal and portable products emphasize the power vector. Central office and base station equipment emphasizes the performance vector. Finally, consumer products emphasize the cost vector. At this point, you are probably thinking that, in each of the above examples, the other two vectors are also required to the product needs. But, what generally happens. is one of the vectors is primary and the other two only need to be good enough.

The value of time is beginning to be the ultimate consideration in a new product. Figure 4 attempts to put this into perspective.

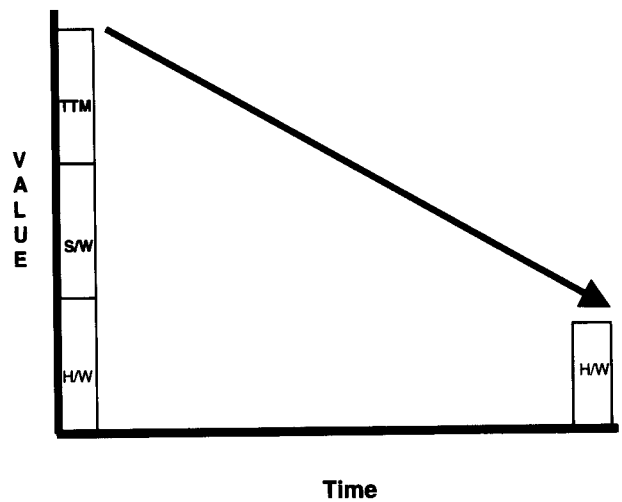

Figure 4. The value of time. The value of a product decreases over time in addition to.

When a new product is introduced, there are three different components of its value. The first is the Hardware (H/W). The second is its software (S/W) or programmability. And, finally is its Time-To-Market (TTM). Of the three components, the most valuable is the Time-To-Market.

The first company to market with a new product:
- -Is forgiven of all mistakes, bugs, etc.
- -Makes a profit
- -Obtains immediate feedback to improve the next product

The Second to market:
- -Must have it right
- -Will only break even

The third to market:
- -Looses money

The final concept is the value of complexity. Typically, as a product becomes more complex, it gains in value. In technology, though, this is not always true. Figure 5 shows the relationship between complexity and value as it seems to occur in technology.

Initially, value and complexity have a strong correlation. As the complexity is increased, the value of a product is increased; but, this only occurs to a point. After this point, the value is actually reduced with added complexity. At first, this seems counterintuitive. So, an example is appropriate. I will take two points on the curve. The first is at the point of minimal complexity and minimum value. This point could be for the simple transistor. The transistor is a very simple item of technology and its value reflects its simplicity. Basically, transistors are "free". If I go to the other end of the complexity curve in Figure 4, I could put in the voice band modem. The modem (V.90 and below) has an interesting history. Although it is very complex in concept and design, it is represented to the market as a complete solution. Because it is a complete solution, it is once again a simple product with little value. Although this was great for consumers, it was very difficult for manufacturers to make money.

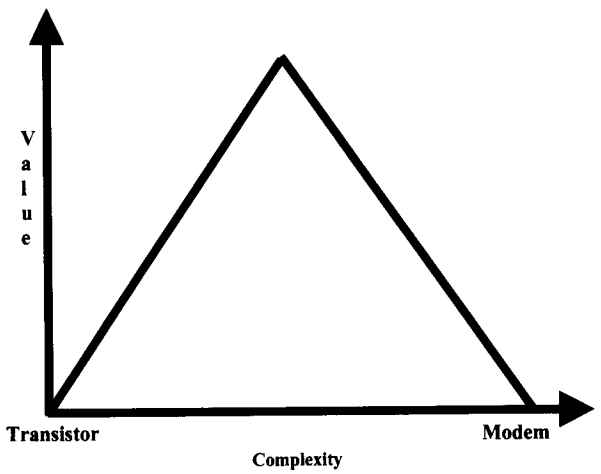

Figure 5. Value versus Complexity. To a point, value grows with complexity. But, at some point, the value decreases with added complexity.

Seems like the right thing to do

Now that I have looked at the system considerations of SOC, let me turn to the last reason for putting systems on a chip. That reason being that "it seems like the right thing to do". Unfortunately, this appears to be the justification of many design teams for putting complete systems on one device.

Rather than use this as the reason for doing SOC, it is better to look at the performance, power and cost needs of the final product. Better success can be assured by carefully considering the system constraints, such as time to market, the value of complexity, and then consider the trade off between performance, power and cost.

HOW SHOULD WE DO IT

Now that I have looked at why and when should we use SOC, I would like to turn my focus to how should we use the concepts to best take advantage of the technology. SOC can be created with several different architectural concepts:

- Custom logic
- ASIC
- Microprocessor/MicroComputer
- Combination

Rather than spend time on each of the architectural concepts, I would like to jump immediately to the last concept of a combination of concepts. I will refer to Figure 6 in the following discussion.

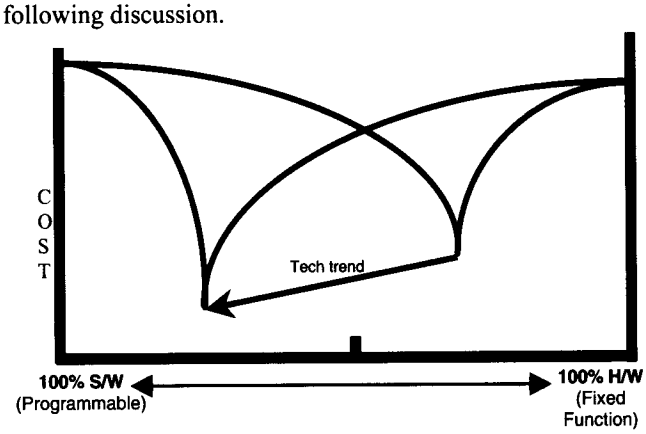

Figure 6. A Eutectic diagram shows the cost function of a task as it is related to a combination of software and hardware.

As shown in Figure 6, a particular task, or function, can be accomplished in either software on a processor or purely in hardware. The diagram, known as an Eutectic diagram, shows that either done in software or hardware, will have a particular cost.

Let me take a moment to talk about the concept of "cost". In the case of SOC, cost can be in the form of development cost, manufacturing cost, power dissipation, size, and/or, time-to-market. And, it might also be a combination. With that said, let me continue on with the discussion.

There are three important concepts that should be taken from the Eutectic diagram. The first is that the lowest cost will always be a combination of software and hardware. The second is that as technology advances, the cost will be reduced. Finally, the solution will move more toward software.

I have begun to refer more to the concept Programmable and Fixed Function rather than Software and Hardware. I believe that this better describes the two concepts as we move into the next era of integrated circuit technology.

WHO SHOULD DO IT

This is really an interesting question. As integrated circuit technology has advanced, we have moved from transistor to Small Scale Integration (SSI), to Medium Scale Integration (MSI), to Large Scale Integration (LSI), to Very Large Scale Integration (VLSI), and finally to System On a Chip (SOC). Another way of looking at it is to think about the division of labor.

During the early stages of the integrated circuit era (consisting of the last 30 to 40 years), a skilled set of designers created components using integrated circuit technology and another skilled set of designers created systems out of components. These were two distinctly different skill sets.

We are now at a juncture where complete systems are integrated on to one integrated circuit. So, then, the question. Will integrated circuit designers become system designers? Or, will system designers become integrated circuit designers? These questions are in the process of being answered. I won't attempt to give a definitive answer, but will predict that the system designer will be the winner.

CONCLUSION

The purpose of this paper was to give a systems perspective to System On a Chip. With the advances of integrated circuit technology, SOC will become our future. It is in our best interest to take full advantage of the technology to create new products that will impact our society.

The most exciting part of this is that the greatest inventions are yet to be made.

As DSP Business Development Manager, Gene Frantz is presently responsible for creating new businesses within TI utilizing digital signal processing technology. In recognition of his leadership role in establishing TI as the world's leading DSP solutions provider, Frantz was elected to TI Senior Fellow in 1997, a privilege enjoyed by less than 0.1 percent of TI's technical personnel.

Frantz joined TI's consumer products division in 1974. While in that division, he took a leadership role in the development of TI's educational products: he was the program manager for the Speak & Spell™ learning aid, and led the development team for all of the early speech products for TI. In 1984, he transferred to Semiconductor Group's DSP Department to become the applications manager. Since this position, he has been recognized as a leader in DSP technology both within TI and throughout the industry.

Frantz received his BSEE from the University of Central Florida in 1971, his MSEE from Southern Methodist University in 1977, and his MBA from Texas Tech University in 1982.

Frantz is a senior member of the Institution of Electric and Electronics Engineers. He holds 29 patents in the area of memories, speech, consumer products and DSP. He has written more than 30 papers and articles and continually makes presentations at universities and conferences worldwide. Frantz is also among DSP experts widely quoted in the media, due to his tremendous knowledge and visionary view of DSP.

Future is in Wireless

Heikki Huomo

Nokia Mobile Phones Ltd,. Finland

PAPER NOT AVAILABLE

Joint Activity for Semiconductor R&D and Role of Semiconductor Technology Academic Research Center (STARC)

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Since its establishment in 1994 SIRIJ (Semiconductor Industry Research Institute Japan) has been working on the promotion of semiconductor R&D in Japan by 10 Japanese semiconductor companies. Major achievements were made in the year of 1995 and 1996 with the establishment of the Semiconductor Technology Academic Research Center (STARC) and Semiconductor Leading Edge Technologies (Selete) which are the first joint companies by the industry in Japan. In the same year the Japanese government founded a research consortium for advanced electronics named Association of Super-advanced Electronics Technologies (ASET). Selete, known as the counterpart of SEMATECH in the U.S., was established by 10 Japanese companies and its major activity was the evaluation of equipment and materials used for next generation 300mm wafers. In 1997 Samsung agreed to join Selete as a non-shareholder member. In 2000, research activities at Selete focused on the "300mm program," an evaluation program for semiconductor manufacturing equipment and materials for 300mm wafers; advanced lithography technology, encompassing VUV laser lithography, related advanced mask technology and EPL; Technology Computer Aided Design (TCAD); and PerFluoro Compound (PFC) emission reduction technology.

ASET is also changing. In 1998 EUV Lithography project started and in 1999 so called Electronic System Integration Technology project which seeks the possibility of new packaging technology, PFC substitution process technology and F2 laser lithography technology started.

STARC was established in December 1995 to grapple with the issues facing the semiconductor industry. Its original goal was to seek out effective new technologies through cooperation between industry and academia, thus achieving breakthroughs in semiconductor technology. STARC is currently involved in joint research with universities focusing on 36 separate themes; several of the research themes taken on shortly after the Center's establishment have already progressed to the practical application stage.

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Purpose of STARC
1) Semiconductor technology research commissioning and joint research
2) Disclosure of the research results
3) Planning, implementation and consulting
4) Study on technology, R&D of IC
5) Joint development on Design Technologies

STARC supports academic research
1) In the field of Si LSI
2) Valuable and transferable to the industry within 10 years
3) 3 to 5 years project
4) Funding : 15 - 20 M yen / year for PG
5 - 10 M yen / year for PJ

STARC provides industry needs and information through Visiting Researcher from member companies

Basic ideas for the invited research projects
1) New technology that can become an industrial standard in the future
2) Pre-competitive technology with potential for transfer into the industry
3) R & D activities that nurture next-generation researchers

Area of Research Recruitment
A : System Research Field
A1) Leading-edge System LSI Architecture
A2) Leading-edge LSI Circuit Technology
A3) Leading-edge Design Technology
B : Process and Device Research Field
B1) Leading-edge Material Technology
B2) Advanced Process Technology
B3) Leading-edge Device Technology
http://www.starc.or.jp/roadmap99/

Recently, we began activities in a new field of operations targeting an increase in the efficiency of new system LSI development. The progress in semiconductor technologies has facilitated the shift from semiconductor as a parts of systems to the production of SoC- "System on a Chip"- in which an entire system can be implemented on a single chip. On the other hand, manufacturers are facing new issues in that circuit designs incorporating tens millions of transistors must be completed in a short period of time. It will be difficult to overcome this issue using extensions of existing design technologies. STARC is thus promoting technological developments aimed at the resolution of this problem through a new approach, namely, the introduction of automation in the high-level design stages of system development, and reuse of design assets. STARC develops strategic IP design technologies, including technologies for reducing power consumption. STARC is also training of LSI design engineers in companies, and providing educational support for semiconductor research at universities.

Finally, I believe that face-to-face collaboration between persons with different career and culture is the most important for the industry because it is the best way to increase the probability of technical breakthrough.