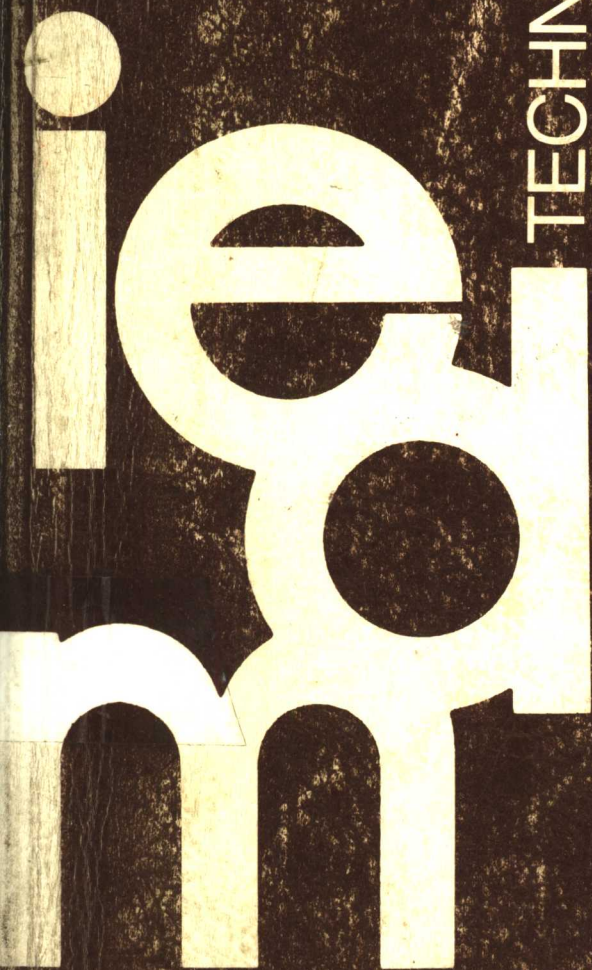


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WELCOME FROM THE GENERAL CHAIR

On behalf of the 1997 IEDM Committee, I would like to welcome you to the 1997 International Electron Devices Meeting in Washington, DC. The 1997 IEDM continues a long tradition as the premier forum for the presentation of the latest research and development in the area of electron devices and their applications. The strong international nature of our industry is evident with invited speakers and contributed papers from major semiconductor centers from around the world.

Two short courses are scheduled for Sunday. These are designed for broad appeal to the IEDM participants including those unfamiliar with the topics. The courses are entitled "Giga-Scale CMOS Technology" and "Trends in RF Devices for Wireless Applications". These courses have been organized and will be presented by active researchers who are experts in these fields.

The plenary talks on Monday will feature presentations on chipcards; on the impact of multimedia on semiconductor technology; and on the limits of optical lithography. Speakers from North America, Europe and Asia will be features.

The IEDM Luncheon speaker this year will be Jim Early. Jim has had a long and distinguished career, first at Bell Labs and then at Fairchild. Dr. Early's talk is entitled "... out to Murray Hill to play!—An Early History of Transistors". I believe that this will be both informative and entertaining. I recommend that you not miss it.

On Tuesday night, panel sessions are planned on two important and potentially controversial topics: "Manufacturing in the Next Millennium: The Emerging Role of Foundries in Silicon Technologies" and "Lithography for 100 nm Device Fabrication".

This year we are continuing two new features to improve accessibility to the information in the IEDM abstracts. We have included 50 word abstracts on the IEDM home page which are available now (please visit our site at <http://www.ieee.org/conference/iedm>). We are also providing the digest in a CD-ROM version that will be distributed along with the technical digest.

On behalf of the IEEE Electron Devices Society, which sponsors the IEDM, Pierre Woerlee, Technical Program Chair and Gary Bronner, Technical Program Vice Chair, I wish to express my sincere appreciation and congratulations to the members of the IEDM committee for the outstanding job they have done in planning and organizing the 1997 meeting. The authors are to be commended for their efforts in preparing and presenting the high-quality papers that form the foundation of the IEDM

It is with great pleasure that I extend a warm welcome to them and to all the attendees of the 1997 IEEE International Electron Devices Meeting.



Ken Galloway
General Chair



Pierre Woerlee
Technical Program Chair



Gary Bronner
Technical Program
Vice Chair



001634

AWARD PRESENTATIONS

PLENARY SESSION

Monday, December 8

1996 Roger A. Haken Best Student Paper Award:

To: Jan De Blauwe, IMEC, Leuven, Belgium

For the paper entitled: "A New Quantitative Model to Predict SILC-Related Disturb Characteristics in Flash-E² PROM Devices"

Paul Rappaport Award

To: Chris Diorio, Paul Hasler, Bradley Minch and Carver Mead, TRW, Inc., Georgia Institute of Technology, Cornell University and Cal Tech.

For the paper entitled: "A Single-Transistor Silicon Synapse"

EDS Distinguished Service Award

To: George Smith

Bell Labs (retired), Barnegat, NJ

"To recognize and honor outstanding service to the Electron Devices Society"

J. J. EBERS Award

To: Marvin White

Lehigh University, Bethlehem, PA

"For outstanding technical contributions to electron devices"

IEDM LUNCHEON

Tuesday, December 9

1997 IEEE Clelio Brunetti Award

To: Dieter Kern (M'IEEE), Eberhard-Karls-Universitat Tübingen, Tübingen, Germany and George Sai-Halasz (F'IEEE), IBM/TJ Watson Research Center, Yorktown Heights, NY and Matthew Wordeman (SM'IEEE), IBM Microelectronics, Hopewell Junction, NY

"For the development of sub-0.1 micron MOSFET devices and circuits"

1997 IEEE Jack A. Morton Award

To: Chenming Hu (F'IEEE), University of California, Berkeley, CA

"For outstanding contributions to the physics and modeling of MOS device reliability"

IEEE Undergraduate Teaching Award

To: Chand Viswanathan (LF'IEEE), University of California, Los Angeles, CA

"For inspirational undergraduate teaching and curriculum development in solid-state electronics"

LUNCHEON PRESENTATION

"... out to Murray Hill to play!, An Early History of Transistors" a presentation by James M. Early

CONFERENCE HIGHLIGHTS

<u>Date</u>	<u>Time</u>	<u>Place</u>	<u>Event</u>
12/7	9:00 a.m. - 5:30 p.m.	International Ballroom Center & East	Short Courses
12/8	9:00 a.m. - 12:00 p.m.	International Ballroom Center	Plenary Session
12/8	6:00 p.m. - 7:30 p.m.	International Ballroom Center	Reception
12/9	9:00 a.m. - 12:00 p.m.	Monroe Room	Emerging Technologies Session
12/9	12:20 p.m. - 2:00 p.m.	International Ballroom West	Luncheon
12/9	8:00 p.m. - 10:00 p.m.	International Ballroom Center & East	Panel Sessions

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1997 IEDM Conference and Program Committee

Seated from left to right: Judy Hoyt, Short Course Vice Chair; Lalita Manchanda, Short Course Chair; Gary Bronner, Technical Program Vice Chair; Ken Galloway, General Chair; Pierre Woerlee, Technical Program Chair; Ilesanmi Adesida, Emerging Technologies Chair; Sophie Verdonckt Vandebroek, Publicity Vice Chair; First row standing from left to right: Joel Hartmann, European Arrangements Co-Chair; Taylor Efland, Subcommittee Chair, Solid State Devices; Seiichiro Kawamura, Subcommittee Chair, Device Interconnect Technology; Pallab Bhattacharya, Subcommittee Chair, Quantum Electronics and Compound Semiconductors; Savvas Chamberlain, Subcommittee Chair, Detectors, Sensors and Displays; Guido Groeseneken, Publicity Vice Chair; Werner Weber, European Arrangements Co-Chair; Mark Law, Publicity Chair; Dick Klaassen, Subcommittee Chair, Modeling and Simulation; Shih-Wei Sun, Asian Arrangements Co-Chair; Jack Sun, Subcommittee Chair, CMOS Devices and Reliability; Morgan Thoma, Subcommittee Chair, Integrated Circuits; Second row standing from left to right: Phyllis Mahoney, Conference Manager; Melissa Widerkehr, Conference Manager; Shuji Ikeda, Asian Arrangements Co-Chair

SUBCOMMITTEE ON CMOS DEVICES AND RELIABILITY

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TABLE OF CONTENTS

PLENARY SESSION

Monday, December 8, 9:00 a.m.
International Ballroom Center

- 1.1 **Multimedia: Future and Impact for Semiconductor Technology**, H. Sasaki, NEC Corporation, Tokyo, Japan 3
- 1.2 **Pushing the Limits of Lithography for IC Production**, T. Brunner, IBM, Hopewell Junction, NY 9
- 1.3 **The Significance of Innovation in the Semiconductor Industry for Performance in Chip Card Applications**, U. Hamann, Siemens, Munich Germany 15

Session 2: Integrated Circuits—Advanced and Embedded DRAM Technology 23

Monday, December 8, 1:00 p.m.
International Ballroom Center

Co-Chairs: Tze-Chiang Chen, IBM Corp.
Won-Seong Lee, Samsung Electronics Co.

- 1:05 p.m.
- 2.1 **Two-Dimensional Borderless Contact Pad Technology for a 0.135 μ m² 4-Gigabit DRAM Cell**, H. Koga, T. Matsuki, N. Kasai, T. Tatsumi, Y. Hayashi, Y. Saito, K. Nakajima, K. Tokunaga, Y. Yamada, N. Onoda, K. Tokashiki, A. Nishizawa, H. Kawamoto and K. Koyama, NEC Corp., Kanagawa, Japan 25
- 1:30 p.m.
- 2.2 **A Simple 4 G-bit DRAM Technology Utilizing High-Aspect-Ratio Pillars for Cell-Capacitors and Peripheral-Vias Simultaneously Fabricated**, S. Nakamura, M. Kosugi, A. Sato, A. Hatada, H. Minakata, M. Kobayashi, T. Kurahashi, R. Suzuki and N. Sasaki, Fujitsu Laboratories, Ltd., Atsugi, Japan 29
- 1:55 p.m.
- 2.3 **Embedded DRAM Technologies**, H. Ishiuchi, T. Yoshida, H. Takato, K. Tomioka, K. Matsuo, H. Momose, S. Sawada, K. Yamazaki and K. Maeguchi, Toshiba Corp., Yokohama, Japan 33
- 2:20 p.m.
- 2.4 **A Salicide-Bridged Trench Capacitor with a Double-Sacrificial-Si₃N₄-Side-wall(DSS) for High Performance Logic-Embedded DRAMs**, M. Togo, S. Iwao, H. Nobusawa, M. Hamada, K. Yoshida, N. Yasuzato and T. Tanigawa, NEC Corp., Kanagawa, Japan 37
- 2:45 p.m.
- 2.5 **Low Temperature Metal-Based Cell Integration Technology for Gigabit and Embedded DRAMs**, M. Yoshida, T. Kumauchi, K. Kawakita, N. Ohashi, H. Enomoto, T. Umezawa, N. Yamamoto, I. Asano, and Y. Tadaki, Hitachi, Ltd., Tokyo, Japan 41
- 3:10 p.m.
- 2.6 **Trade-Offs in the Integration of High Performance Devices with Trench Capacitor DRAM**, S. Crowder, S. Stiffler, P. Parries, G. Bronner, L. Nesbit, W. Wille, M. Powell, A. Ray, B. Chen, and B. Davari, IBM, Hopewell Junction, NY 45

Session 3: Solid State Devices—RF Technology 49

Monday, December 8, 1:00 p.m.
International Ballroom West

Co-Chairs: Jenny Ford, Motorola
Steve Kosiers, VTC

- 1:05 p.m.
- 3.1 **2-GHz Si Power MOSFET Technology**, I. Yoshida, Hitachi, Ltd., Tokyo, Japan 51

- 1:30 p.m.
- 3.2 **Novel Substrate Contact Structure for High-Q Silicon-Integrated Spiral Inductors**, J.N. Burghartz, A.E. Ruehli, K.A. Jenkins, M. Soyuer and D. Nguyen-Ngoc, IBM T.J. Watson Research Center, Yorktown Heights, NY 55

- 1:55 p.m.
- 3.3 **High Q Microwave Inductors in CMOS Double-Metal Technology and Its Substrate Bias Effects for 2 GHz RF ICs Application**, M. Park, C.S. Kim, J.M. Park, H.K. Yu and K.S. Nam, Electronics and Telecommunications Research Institute, Taejeon, Korea 59

- 2:20 p.m.
- 3.4 **Extremely High-Q Tunable Inductor for Si-Based RF Integrated Circuit Applications**, D. Pehlke, A. Burstein and M.F. Chang, Rockwell Science Center, Thousand Oaks, CA 63

- 2:45 p.m.
- 3.5 **Monolithic High-Performance Three-Dimensional Coil Inductors for Wireless Communication Applications**, D.J. Young, J.J. Ou, B.E. Boser, V. Malba* and A.F. Bernhardt*, University of California, Berkeley, CA and *Lawrence Livermore National Laboratory, CA 67

Session 4: CMOS Devices and Reliability—Thin Oxide Reliability and Characterization 71

Monday, December 8, 1:00 p.m.
International Ballroom East

Co-Chairs: John Suehle, NIST
Roland Thewes, Siemens

- 1:05 p.m.
- 4.1 **Ultra-Thin Gate Dielectrics: They Break Down, but do they Fail?**, B.E. Weir, P.J. Silverman, D. Monroe, K.S. Krisch, M. Alam, G.B. Alers, T.W. Sorsch, G.L. Timp, F. Baumann, C.T. Liu, Y. Ma* and D. Hwang*, Bell Laboratories, Lucent Technologies, Murray Hill, NJ and *Bell Laboratories, Lucent Technologies, Orlando, FL 73

- 1:30 p.m.
- 4.2 **Thickness and Polarity Dependence of Intrinsic Breakdown of Ultra-Thin Reoxidized-Nitride for DRAM Technology Applications**, E. Wu, C. Hwang*, R. Vollersten**, H. Shen*, R. Kleinhenz*, C. Radens* and A. Strong, IBM Microelectronics, Essex Junction, VT and *IBM, Hopewell Junction, NY and **Siemens Comp., Essex Junction, VT 77

- 1:55 p.m.
- 4.3 **Investigations of Hot-Carrier-Induced Breakdown of Thin Oxides**, Y. Kamakura, H. Utsunomiya, T. Tomita, K. Umeda and K. Taniguchi, Osaka University, Osaka, Japan 81

- 2:20 p.m.
- 4.4 **Intrinsic and Stress-Induced Traps in the Direct Tunneling Current of 2.3–3.8 nm Oxides and Unified Characterization Methodologies for Sub-30 nm Oxides**, C.T. Liu, A. Ghetti, Y. Ma*, G. Alers, C.P. Chang, K.P. Cheung, J.I. Colonell, W.Y.C. Lai, C.S. Pai, R. Liu, H. Vaidya, and J.T. Clemens, Bell Laboratories, Lucent Technologies, Murray Hill, NJ and *Bell Laboratories, Lucent Technologies, Orlando, FL 85

- 2:45 p.m.
- 4.5 **Characterization of Various Stress-Induced Oxide Traps in MOSFETs by Using a Novel Transient Current Technique**, T. Wang, L. Chiang, N. Zous, T. Chang and C. Huang*, National Chiao-Tung University, Taiwan, Rep. of China and *Macronix Co., Taiwan, Rep. of China 89

- 3:10 p.m.
4.6 High-Temperature Reliability Behavior of SSI-Flash E²PROM Devices, J. DeBlauwe, D. Wellekens, G. Groeseneken, L. Haspeslagh, J. Van Houdt, L. Deferm and H. Maes, IMEC, Leuven, Belgium 93

Session 5: Device Interconnect Technology— Low Resistance Silicide Integration 97

Monday, December 8, 1:00 p.m.
Jefferson Room

Co-Chairs: M. Motoyoshi, Sony Corp.
 Kelly Baker, Motorola, Inc.

- 1:05 p.m.
5.1 A High-Performance 0.1 μ m CMOS with Elevated Salicide Using Novel Si-SEG Process, H. Wakabayashi, T. Yamamoto, T. Tatsumi, K. Tokunaga, T. Tamura, T. Mogami and T. Kunio, NEC Corp., Kanagawa, Japan 99

- 1:30 p.m.
5.2 Low Resistance Ti or Co Salicided Raised Source/Drain Transistors for Sub-0.13 μ m CMOS Technologies, C. Chao, K. Violette, S. Unnikrishnan, M. Nandakumar, R. Wise, J. Kittl, Q.Z. Hong and I.C. Chen, Texas Instruments, Dallas, TX 103

- 1:55 p.m.
5.3 CoSi₂ with Low Diode Leakage and Low Sheet Resistance of 0.065 μ m Gate Length, Q.Z. Hong, W.T. Shiau, H. Yang, J. Kittl, C. Chao, H. Tsai, S. Krishnan, I. Chen and R. Havemann, Texas Instruments, Inc., Dallas, TX 107

- 2:20 p.m.
5.4 Novel One-Step RTP Ti SALICIDE Process with Low Sheet Resistance 0.06 μ m Gates and High Drive Current, J. Kittl, Q.Z. Hong, M. Rodder and T. Breedijk, Texas Instruments, Dallas, TX 111

- 2:45 p.m.
5.5 Temperature and Current Effects on Small-Geometry-Contact Resistance, K. Banerjee, A. Amerasekera*, G. Dixit* and C. Hu, University of California, Berkeley, CA and *Texas Instruments, Dallas, TX 115

- 3:10 p.m.
5.6 Low-Resistivity Noble Integrated Clustered Electrode (NICE) WSix Polycide and its Application to a Deep Sub-Quarter Micron CMOS, J.S. Byun, J.S. Park, B.H. Lee, D.K. Sohn, J.W. Park, J.J. Kim and J.M. Hwang, LG Semicon Co. Ltd., Cheongju-si, Korea 119

Session 6: Modeling and Simulation— Interconnect Modeling and Manufacturability 123

Monday, December 8, 1:00 p.m.
Georgetown Room

Co-Chairs: Duane Boning, Massachusetts Institute of Technology
 Kristin DeMeyer, IMEC

- 1:05 p.m.
6.1 Hierarchical Interconnect Modeling, E. Chiprout, IBM Austin Research Lab, Austin, TX 125

- 1:30 p.m.
6.2 Automated Extraction of Capacitances and Electrostatic Forces in MEMS and ULSI Interconnects from the Mask Layout, M. Bächtold, S. Taschini, J.G. Korvink* and H. Baltes, Swiss Federal Institute of Technology, Zurich, Switzerland and *Albert Ludwig University, Freiburg, Germany 129

- 1:55 p.m.
6.3 A Simulation Methodology for Assessing the Impact of Spatial/Pattern Dependent Interconnect Parameter Variation on Circuit Performance, B. Stine, V. Mehrotra, D. Boning, J. Chung and D. Ciplickas*, Massachusetts Institute of Technology, Cambridge, MA and *PDF Solutions, San Jose, CA 133

- 2:20 p.m.
6.4 Modeling of Pattern-dependent On-chip Interconnect Geometry Variation for Deep-Submicron Process and Design Technology, O.S. Nakagawa, S.-Y. Oh and G. Ray, Hewlett Packard Laboratory, Palo Alto, CA 137

- 2:45 p.m.
6.5 Spice Simulation of 0.18 μ m CMOS Ringoscillators Using Physical Models for Capacitance and Series Resistance, S. Biesemans, S. Kubicek and K. De Meyer, IMEC, Leuven, Belgium 141

- 3:10 p.m.
6.6 New Method for Verification of Analytical Device Models Using Transistor Parameter Fluctuations, C. Kühn, S. Marksteiner*, T. Kopley* and W. Weber*, Universität der Bundeswehr, Neubiberg, Germany and *Siemens AG, Munich, Germany 145

- 3:35 p.m.
6.7 An Application of Process Synthesis Methodology for First-Pass Fabrication Success of High-Performance Deep-Submicron CMOS, S. Saxena, R. Burch, K. Vasanth, S. Rao, C. Fernando, J. Davis and P. Mozumder, Texas Instruments, Dallas, TX 149

Session 7: Quantum Electronics and Compound Semiconductors—Single Electron Devices 153

Monday, December 8, 1:00 p.m.
Monroe Room

Co-Chairs: Leda Lunardi, AT&T Laboratories
 C.P. Lee, National Chiao Tung University

- 1:05 p.m.
7.1 Fabrication of Single Electron Memory on Atomically Flat α -Al₂O₃ Substrate made by ATM Nano-Oxidation Process, K. Matsumoto, Y. Gotoh, J. Shirakashi, T. Maeda and J.S. Harris*, Electrotechnical Laboratory, Tsukuba, Japan and *Stanford University, Stanford, CA 155

- 1:30 p.m.
7.2 Single Electron Charging of Sn Nanocrystals in Thin SiO₂ Film Formed by Low Energy Ion Implantation, A. Nakajima, T. Futatsugi, N. Horiguchi, H. Nakao and N. Yokoyama, Fujitsu Laboratories, Ltd., Atsugi, Japan 159

- 1:55 p.m.
7.3 Silicon Double-Island Single-Electron Device, A. Fujiwara, Y. Takahashi, K. Yamazaki, H. Namatsu, M. Nagase, K. Kurihara and K. Murase, NTT Basic Research Laboratories, Kanagawa, Japan 163

- 2:20 p.m.
7.4 Room Temperature Silicon Single-Electron Quantum-Dot Transistor Switch, L. Zhuang, L. Guo and S.Y. Chou, University of Minnesota, Minneapolis, MN 167

- 2:45 p.m.
7.5 Verify: Key to the Stable Single-Electron-Memory Operation, T. Ishii, K. Yano, T. Sano, T. Mine, F. Murai and K. Seki, Hitachi, Tokyo, Japan 171

- 3:10 p.m.
7.6 Room Temperature Nb/Nb Oxide-Based Single-Electron Transistors, J.I. Shirakashi, K. Matsumoto, N. Miura* and M. Konagai*, Electrotechnical Laboratory, Ibaraki, Japan and *Tokyo Institute of Technology, Tokyo, Japan 175

- 3:35 p.m.
7.7 PLED—Planar Localised Electron Devices, K. Nakazato, P. Piotrowicz*, D. Hasko*, H. Ahmed* and K. Itoh**, Hitachi Europe Ltd., Cambridge, UK and *Cavendish Laboratory, Cambridge, UK and **Hitachi Ltd., Tokyo, Japan 179

Session 8: Detectors, Sensors and Displays—Image Sensors 183

Monday, December 8, 1:00 p.m.
Thoroughbred Room

Co-Chairs: Richard Bredthauer, Lockheed Martin Fairchild Systems
Jerry Hynecek, Texas Instruments, Inc.

1:05 p.m.

- 8.1 A 1/3" Progressive Scan 1280(H) X 960(V) FT-CCD for Digital Still Camera Applications,** J. Bosiers, Y. Boersma, A. Kleimann, D. Verbugt, H. Peek and A. van der Sijde, Philips Imaging Technology, Eindhoven, The Netherlands 185

1:30 p.m.

- 8.2 Frame Transfer Area Array Sensor with Vertical Antiblooming and Novel Readout for Enhanced Performance,** M. Kiik, C. Flood, G. Weale and S.G. Ingram, Dalsa, Inc., Waterloo, Canada 189

1:55 p.m.

- 8.3 Characterization of Surface- and Buried-Channel Detection Transistors for CCD On-Chip Amplifiers,** P. Centen and E. Roks, Philips Imaging Technology, Eindhoven, The Netherlands 193

2:20 p.m.

- 8.4 a-Si:H Schottky Diode Direct Detection Pixel for Large Area X-Ray Imaging,** K. Aflatoni, A. Nathan, R. Hornsey, I. Cunningham* and S.G. Chamberlain**, University of Waterloo, Waterloo, Canada, *University Hospital, London, Canada and **Dalsa Inc., Ontario, Canada 197

2:45 p.m.

- 8.5 CMOS Image Sensors—Recent Advances and Device Scaling Considerations,** H.S.P. Wong, IBM TJ Watson Research Center, Yorktown Heights, NY 201

3:10 p.m.

- 8.6 Noise Performance of a Color CMOS Photogate Image Sensor,** A. Blanksby, M. Loinaz*, D. Inglis* and B. Ackland*, University of Adelaide, South Australia and *Bell Laboratories, Holmdel, NJ 205

3:35 p.m.

- 8.7 TFA Image Sensors: From the One Transistor Cell to a Locally Adaptive High Dynamic Range Sensor,** B. Schneider, H. Fischer, S. Benthien, H. Keller, T. Lule, P. Rieve, J. Schulte, M. Sommer and M. Bohm, Universitat-GH Siegen, Siegen, Germany 209

Session 9: CMOS Devices and Reliability—Advanced CMOS Devices 213

Tuesday, December 9, 9:00 a.m.
International Ballroom Center

Co-Chairs: Suresh Venkatesan, Motorola
Thomas Skotnicki, France-Telecom CNET

9:05 a.m.

- 9.1 CMOS Devices Below 0.1 μ m: How High Will Performance Go?** Y. Taur and E. Nowak*, IBM Research, Yorktown Heights, NY and *IBM Microelectronics Division, Essex Junction, VT 215

9:30 a.m.

- 9.2 Subband Structure Engineering for Performance Enhancement of Si MOSFETs,** S.I. Takagi, J. Koga, and A. Toriumi, Toshiba Corporation, Yokohama, Japan 219

9:55 a.m.

- 9.3 A 0.10 μ m Gate Length CMOS Technology with 30A Gate Dielectric for 1.0V–1.5V Applications,** M. Rodder, M. Hanratty, D. Rogers, T. Laaksonen, J. Hu, S. Murtaza, C.P. Chao, S. Hattangady, S. Aur, A. Amerasekera and I.C. Chen, Texas Instruments, Dallas, TX 223

10:20 a.m.

- 9.4 TED Control Technology for Suppression of Reverse Narrow Channel Effect in 0.1 μ m MOS Devices,** A. Ono, R. Ueno and I. Sakai, NEC Corporation, Kanagawa, Japan 227

10:45 a.m.

- 9.5 Anomalous Short Channel Effects in Indium Implanted nMOSFETs,** P. Bouillon, R. Gwozdecki and T. Skotnicki, France-Telecom, Meylan, France 231

11:10 a.m.

- 9.6 Increase of Parasitic Resistance of p MOSFETs Due to Nitrogen Atoms Incorporation into Silicon Substrate by N₂O-Oxynitride Gate Dielectrics Process,** M. Takayanagi-Takagi, H. Yoshimura and Y. Toyoshima, Toshiba Corporation, Yokohama, Japan 235

11:35 a.m.

- 9.7 Sub-10-ps Gate Delay by Reducing the Current Crowding Effect at an Extension,** D. Hisamoto, K. Umeda, K. Ohnishi, J. Yugami, M. Ushiyama and T. Shiba, Hitachi, Ltd., Tokyo, Japan 239

Session 10: Device Interconnect Technology—DRAM 243

Tuesday, December 9, 9:00 a.m.
International Ballroom East

Co-Chairs: Jeff Gambino, IBM
Akihiko Ishitani, ASET

9:05 a.m.

- 10.1 A Novel BST Storage Capacitor Node Technology Using Platinum Electrodes for Gbit DRAMs,** R.B. Khamankar, M.A. Kressley, M.R. Visokay, T. Moise, G. Xing, S. Nemoto, Y. Okuno, S.J. Fang, A.M. Wilson, J.F. Gaynor, T.Q. Hurd, P.L. Crenshaw, S. Summerfelt and L. Colombo, Texas Instruments Incorporated, Dallas, TX 245

9:30 a.m.

- 10.2 Integration of (Ba,Sr)TiO₃ Capacitor with Platinum Electrodes Having SiO₂ Spacer,** B.T. Lee, K.H. Lee, C.S. Hwang, W.D. Kim, H. Horii, H.W. Kim, H.J. Cho, C.S. Kang, J.H. Chung, S.I. Lee and M.Y. Lee, Samsung Electronics Co., Kyungki-do, Korea 249

9:55 a.m.

- 10.3 Effect of Bottom Electrode Materials on the Electrical and Reliability Characteristics of (Ba,Sr)TiO₃ Capacitors,** S.C. Sun and M.S. Tsai*, Taiwan Semiconductor Manufacturing Company, Taiwan, ROC and *National Chiao-Tung University, Taiwan, ROC 253

10:20 a.m.

- 10.4 Epitaxial (Ba,Sr)TiO₃ Capacitors with Extremely High Dielectric Constant for DRAM Applications,** N. Fukushima, K. Abe, M. Izuha, T. Schimizu and T. Kawakubo, Toshiba Corporation, Kawasaki, Japan 257

10:45 a.m.

- 10.5 Impact of Time Dependent Dielectric Breakdown and Stress Induced Leakage Current on the Reliability of (Ba,Sr)TiO₃ Thin Film Capacitors for Gbit-Scale DRAMs,** S. Yamamichi, A. Yamamichi, D. Park and C. Hu, University of California, Berkeley, CA 261

11:10 a.m.

- 10.6 Single Layer Nitride Capacitor Dielectric Film and High Concentration Doping Technology for 1Gb/4Gb Trench-Type DRAMs,** S. Saida, T. Sato, I. Mizushima, Y. Ozawa and Y. Tsunashima, Toshiba Corporation, Kanagawa, Japan 265

Session 11: Integrated Circuits—Flash Memory Technology 269

Tuesday, December 9, 9:00 a.m.
Jefferson Room

Co-Chairs: Kuo-Tung Chang, Motorola, Inc.
Seiichi Aritome, Toshiba Corp.

9:05 a.m.

- 11.1 A Novel High-Density 5F² NAND STI Cell Technology Suitable for 256Mbit and 1Gbit Flash Memories,** K. Shimizu, K. Narita, H. Watanabe, E. Kamiya, Y. Takeuchi, T. Yaegashi, S. Aritome and T. Watanabe, Toshiba Corp., Yokohama, Japan 271

9:30 a.m.

- 11.2 A 0.24 μ m² Cell Process with 0.18 μ m Width Isolation and 3-D Interpoly Dielectric Films for 1-Gb Flash Memories**, T. Kobayashi, N. Matsuzaki, A. Sato, A. Katayama, H. Kurata, A. Miura, T. Mine, Y. Goto, T. Morimoto*, H. Kume, T. Kure and K. Kimura, Hitachi, Ltd., Tokyo, Japan and *Hitachi ULSI Eng. Corp., Tokyo, Japan **275**

9:55 a.m.

- 11.3 Secondary Electron Flash—A High Performance, Low Power Flash Technology for 0.35 μ m and Below**, J. Bude, M. Mastrapasqua, M. Pinto, R. Gregor*, P. Kelley*, R. Kohler**, C. Leung*, Y. Ma*, R. McPartland**, P. Roy* and R. Singh*, Bell Laboratories, Lucent Technologies, Murray Hill, NJ and *Orlando, FL and **Allentown, PA **279**

10:20 a.m.

- 11.4 A Triple Polysilicon Stacked Flash Memory Cell with Wordline Self-Boosting Programming**, J.D. Choi, D.G. Lee, D.J. Kim, S.S. Cho, H.S. Kim, C.H. Shin and S.T. Ahn, Samsung Electronics Co. Ltd., Kyungki-do, Korea **283**

10:45 a.m.

- 11.5 Novel-Self-Convergent Programming Scheme for Multi-Level P-Channel Flash Memory**, S.J. Shen, C.S. Yang, Y.S. Wang, C.C.H. Hsu, S.D.T. Chang*, N. Rodjy* and A.C. Wang*, National Tsing-Hua University, Taiwan, Rep. of China, Programmable Microelectronics Corp.* **287**

11:10 a.m.

- 11.6 A Novel Isolation-Scaling Technology for NAND EEPROMs with the Minimized Program Disturbance**, S. Satoh, H. Hagiwara, T. Tanzawa, K. Takeuchi and R. Shiota, Toshiba Corp., Yokohama, Japan **291**

11:35 a.m.

- 11.7 Performance and Reliability Evaluations of P-Channel Flash Memories with Different Programming Schemes**, S.S. Chung, S.N. Kuo, C.M. Yih and T.S. Chao*, National Chiao Tung University, Taiwan, ROC and *National Nano Device Lab, Taiwan, ROC **295**

Session 12: Modeling and Simulation—RF Modeling **299**

Tuesday, December 9, 9:00 a.m.

Georgetown Room

Co-Chairs: Chandra Mouli, Micron Technology, Inc.
Mi-Chang Chang, Texas Instruments, Inc.

9:05 a.m.

- 12.1 Device Simulation for RF Application**, R. Dutton, B. Troyanovsky¹, Z. Yu, T. Arnborg², F. Rotella, G. Ma³ and J. Sato-Iwanaga⁴, Stanford University, Stanford, CA and ¹HP/EESof and ²Ericsson ComponentsAB, ³Motorola, Tempe, AZ and ⁴Matsushita Electronics Corp. **301**

9:30 a.m.

- 12.2 Low Noise FET Design for Wireless Communications**, L.M. Franca-Neto, E. Mao and J.S. Harris Jr., Stanford University, Stanford, CA **305**

9:55 a.m.

- 12.3 R.F. MOSFET Modeling Accounting for Distributed Substrate and Channel Resistances with Emphasis on the BSIM3v3 SPICE Model**, W. Liu, R. Gharpurey, M.C. Chang, U. Erdogan, R. Aggarwal and J. Mattia, Texas Instruments, Dallas, TX **309**

10:20 a.m.

- 12.4 Accurate Drain Conductance Modeling for Distortion Analysis in MOSFETs**, R. van Langevelde and F. Klaassen, Eindhoven University of Technology, Eindhoven, The Netherlands **313**

10:45 a.m.

- 12.5 RF Noise Modelling of 0.25 μ m CMOS and Low Power LNAs**, R. Vanoppen, L. deMaaijer, D. Klaasen and L. Tiemeijer, Philips Research Labs, Eindhoven, The Netherlands **317**

11:10 a.m.

- 12.6 A New Approach to the Physics-Based Noise Analysis of Semiconductor Devices Operating in Large Signal, (quasi) Periodic Regime**, F. Bonani, S. Donati Guerrieri, G. Ghione and M. Pirola, Politecnico di Torino, Torino, Italy **321**

11:35 a.m.

- 12.7 Experimental Results and Simulation of Substrate Noise Coupling via Planar Spiral Inductor in RF ICs**, A. Pun, T. Yeung, J. Lau, F.J.R. Clement*, D. Su**, The Hong Kong University of Science and Technology, Hong Kong, P.R. of China and *Swiss Federal Institute of Technology, Zurich, Switzerland and **Hewlett Packard Laboratory, Palo Alto, CA **325**

Session 13: Emerging Technologies **329**

Tuesday, December 9, 9:00 a.m.

Monroe Room

Co-Chairs: Ilesanmi Adesida, University of Illinois

9:05 a.m.

- 13.1 Organic Polymer Devices and Displays**, D.M. de Leeuw, P.W.M. Blom, C.M. Hart, C.M.J. Mutsaers, C.J. Drury, M. Matters and H. Termeer, Philips Research Labs, Eindhoven, The Netherlands **331**

9:55 a.m.

- 13.2 Neural Microelectronics**, T. Shibata and T. Ohmi, University of Tokyo, Tokyo, Japan **337**

10:45 a.m.

- 13.3 Optical Interconnect Technologies for Si ULSI**, D.A.B. Miller, Stanford University, Stanford, CA **343**

Session 14: Solid State Devices—Power Devices **349**

Tuesday, December 9, 9:00 a.m.

Thoroughbred Room

Co-Chairs: Richard K. Williams, Siliconix-Temic
Ingham A. Mack, Office of Naval Research

9:05 a.m.

- 14.1 A New Concept for High Voltage MCCT With No J-FET Resistance by Using a Very Thin Wafer**, N. Iwamuro, T. Iwaana, Y. Harada, Y. Onozawa and Y. Seki, Fuji Electric Corporate R&D Ltd., Matsumoto, Japan **351**

9:30 a.m.

- 14.2 Reverse Channel Floating Base Emitter Switched Thyristor (RFB-EST)**, S. Xu, R. Constapel, D. Silber* and J. Sin**, Daimler-Benz AG, Frankfurt, Germany and *University Bremen, Bremen, Germany and **The Hong Kong University of Science and Technology, Hong Kong, P.R. of China **355**

9:55 a.m.

- 14.3 A Trench Lateral Power MOSFET Using Self-Aligned Trench Bottom Contact Holes**, N. Fujishima and C.A.T. Salama University of Toronto, Ontario, Canada **359**

10:20 a.m.

- 14.4 A 1 Million Cell 2.0 m Ω 30-V TrenchFET Utilizing 32 Mcell/in² Density with Distributed Voltage Clamping**, R.K. Williams, W. Grabowski, M. Darwish, M. Chang, H. Yilmaz and K. Owyang, Siliconix-Temic, Santa Clara, CA **363**

10:45 a.m.

- 14.5 16-60V Rated LDMOS Show Advanced Performance in an 0.72 μ m Evolution BiCMOS Power Technology**, C.Y. Tsai, T. Efland, S. Pendharkar, J. Mitros, A. Tessmer, J. Smith, J. Erdeljac and L. Hutter, Texas Instruments, Dallas, TX **365**

11:10 a.m.

- 14.6 Hot-Carrier Reliability in Submicrometer LDMOS Transistors**, R. Versari, A. Pieracci, S. Manzini*, C. Contiero* and B. Ricco, University of Bologna, Bologna, Italy and *SGS-Thomson Microelectronics, Cornaredo Milano, Italy **371**

11:35 a.m.

- 14.7 Lateral DMOS Design for ESD Robustness, C. 375**
Duvvury, F. Carvajal, C. Jones and D. Briggs, Texas Instruments, Dallas, TX

Session 15: Quantum Electronics and Semiconductor Devices—Lasers and LEDs 379

Tuesday, December 9, 9:00 a.m.
Military Room

Co-Chairs: Connie Chang-Hasnain, University of California
John Zavada, Army Research Office

9:05 a.m.

- 15.1 Edge and Surface Emitting Quantum Dot Lasers, D. 381**
Bimberg, N.N. Ledentsov, M. Grundmann, F. Heinrichsdorff, V.M. Ustinov*, P.S. Kop'ev*, Z.I. Alferov* and J.A. Lott**, Technische Universität Berlin, Berlin, Germany, A.F. Ioffe Physical Technical Institute, St. Petersburg, Russia* and Air Force Institute of Technology, Wright-Patterson A.F.B., Ohio**

9:30 a.m.

- 15.2 DC, Modulation and Gain-Switched Characteristics 385**
of Self-Organized $\text{In}_{0.4}\text{Ga}_{0.6}\text{As}/\text{GaAs}$ Quantum Dot Room Temperature Lasers, D. Klotzkin, K. Kamath, R. Jambunathan and P. Bhattacharya, University of Michigan, Ann Arbor, MI

9:55 a.m.

- 15.3 Electron Leakage and the Excess Voltage at p-P 389**
Heterojunctions in $\text{InGaAsP}/\text{InP}$ Lasers, E. Flynn and D. Ackermann*, Lucent Technologies, Breinigsville, PA and *Lucent Technologies, Bell Laboratories, Murray Hill, NJ

10:20 a.m.

- 15.4 Estimation of the Γ -X Crossover Composition in 393**
Disordered $(\text{Al}_x\text{Ga}_{1-x})_{0.5}\text{In}_{0.5}\text{P}$ Using n-i-n Diodes, A. Morrison, J. Lambkin, C. van der Poel* and A. Valster*, University College, Cork, Ireland and *Philips Research Laboratories, Eindhoven, The Netherlands

10:45 a.m.

- 15.5 Short Wavelength Light Emitting Diodes in 397**
 $\text{Al}_{0.4}\text{Ga}_{0.6}\text{P}/\text{GaP}$ Quantum Wells, M. Gerhold, K. Kamath and P. Bhattacharya, University of Michigan, Ann Arbor, MI

11:10 a.m.

- 15.6 220 K Continuous-Wave Operation of AlGaAs/GaAs 401**
Multi-Quantum Well Vertical-Cavity Surface-Emitting Laser on Si Substrate, T. Egawa, N. Nakanishi, T. Jimbo, and M. Umeno, Nagoya Institute of Technology, Nagoya, Japan

11:35 a.m.

- 15.7 WITHDRAWN 405**
Technology, Taejeon, Korea

Session 16: CMOS Devices and Reliability—SOI Devices and Circuits 405

Tuesday, December 9, 2:15 p.m.
International Ballroom Center

Co-Chairs: Kaizad Mistry, Digital Equipment Corp.
Atsushi Hori, Matsushita Electronics Corp.

2:20 p.m.

- 16.1 SOI Floating-Body, Device and Circuit Issues, J. 407**
Gautier, M. Pelella* and J. Fossum**, CEA-LETI, Grenoble, France and *IBM Microelectronics Division, Hopewell Junction, NY and **University of Florida, Gainesville, FL

2:45 p.m.

- 16.2 Design Methodology for Minimizing Hysteretic V_{th} 411**
Variation in Partially-Depleted SOI CMOS, A. Wei and D. Antoniadis, Massachusetts Institute of Technology, Cambridge, MA

3:10 p.m.

- 16.3 A 7.9/5.5 psec Room/Low Temperature SOI CMOS, F. 415**
Assaderaghi, W. Rausch, A. Ajmera, E. Leobandung, D. Schepis, L. Wagner, H.J. Wann, R. Bolam, D. Yee, B. Davari and G.G. Shahidi, IBM Semiconductor Research and Development Center, Hopewell Junction, NY

3:35 p.m.

- 16.4 A Compact Schottky body Contact Technology for 419**
SOI Transistors, J. Sleight and K. Mistry, Digital Equipment Corp., Hudson, MA

4:00 p.m.

- 16.5 Fmax Enhancement of Dynamic Threshold-Voltage 423**
MOSFET (DTMOS) Under Ultra-Low Supply Voltage, T. Tanaka, Y. Momiyama and T. Sugii, Fujitsu Laboratories Ltd., Atsugi, Japan

4:25 p.m.

- 16.6 Self-Aligned (Top and Bottom) Double Gate 427**
MOSFET with a 25 nm Thick Silicon Channel, H.S.P. Wong, K. Chan and Y. Taur, IBM TJ Watson Research Center, Yorktown Heights, NY

Session 17: CMOS Devices and Reliability—Plasma Damage and Hot Carrier Effects 431

Tuesday, December 9, 2:15 p.m.
International Ballroom East

Co-Chairs: Herman Maes, IMEC
K.P. Cheung, Lucent Technologies

2:20 p.m.

- 17.1 Process Charging in ULSI: Mechanisms, Impact and 433**
Solutions, J. McVittie, Stanford University, Stanford, CA

2:45 p.m.

- 17.2 Impact of Plasma-Charging Damage Polarity on 437**
MOSFET Noise, K. Cheung, S. Martin, D. Misra*, K. Steiner**, J. Colonell, C. Chang, W. Lai, C. Liu, R. Liu and C. Pai, Bell Laboratories, Lucent Technologies, Murray Hill, NJ and *Newark, NJ and **Orlando, FL

3:10 p.m.

- 17.3 Reliability of Thin Gate Oxide Under Plasma 441**
Charging Caused by Antenna Topography-Dependent Electron Shading Effect, K. Noguchi, K. Tokashiki, T. Horiuchi and H. Miyamoto, NEC Corp., Kanagawa, Japan

3:35 p.m.

- 17.4 Assessment of Charge-Induced Damage to Ultra- 445**
Thin Gate MOSFETs, S. Krishnan, S. Rangan*, S. Hattangady, G. Xing, K. Brennan, M. Rodder and S. Ashok*, Texas Instruments, Dallas, TX and *Penn State University, University Park, PA

4:00 p.m.

- 17.5 Degradation of Deep Sub-Micron Isolation by 449**
Vacuum Ultraviolet Radiation From Low Temperature Back End Plasma-Assisted Processes, S. Ashburn, S. Krishnan, G. Dixit, M. Rodder, K. Taylor, T. Breedijk, I.C. Chen, M. Goodwin and A. Esquivel, Texas Instruments, Inc., Dallas, TX

4:25 p.m.

- 17.6 A Study of Hot-Carrier Degradation in n- and p- 453**
MOSFETs with Ultra-Thin Gate Oxides in the Direct-Tunneling Regime, H.S. Momose, S. Nakamura, T. Ohguro, T. Yoshitomi, E. Morifuji, T. Morimoto, Y. Katsumata and H. Iwai, Toshiba Corp., Kawasaki, Japan

Session 18: Device Interconnect Technology—Device Technology 457

Tuesday, December 9, 2:15 p.m.
Jefferson Room

Co-Chairs: Dim-Lee Kwong, University of Texas
C.T. Liu, Bell Labs, Lucent Technologies

2:20 p.m.

- 18.1 A Comparison of TiN Processes for CVD W/TiN Gate Electrode on 3 nm Gate Oxide,** H. Yang, G. Brown, J. Hu, J. Lu, S. Hattangady, R. Kraft, A. Rotondaro, I.C. Chen, J. Luttmer, R. Chapman, P. Chen, H. Tsai, B. Amirhekmat and L. Magel, Texas Instruments, Dallas, TX **459**

2:45 p.m.

- 18.2 Ultra Thin (<3 nm) High Quality Nitride/Oxide Stack Gate Dielectrics Fabricated by In-Situ Rapid Thermal Processing,** B.Y. Kim, H.F. Luan and D.L. Kwong, University of Texas, Austin, TX **463**

3:10 p.m.

- 18.3 Boron-Enhanced-Diffusion of Boron: The Limiting Factor for Ultra-Shallow Junctions,** A. Agarwal, D.J. Eaglesham, H.-J. Gossmann, L. Pelaz, S.B. Herner, D.C. Jacobson, T.E. Haynes*, Y. Erokhin** and R. Simonton**, Bell Labs, Lucent Technologies, Murray Hill, NJ and *Oak Ridge National Lab, Oak Ridge, TN and **Eaton Corp, Beverly, MA **467**

3:35 p.m.

- 18.4 A High Performance 50 nm PMOSFET using Decaborane ($B_{10}H_{14}$) Ion Implantation and 2-Step Activation Annealing Process,** K. Goto, J. Matsuo*, Y. Tada, T. Tanaka, Y. Momiyama, T. Sugii and I. Yamada*, Fujitsu Laboratories Ltd., Atsugi, Japan and *Kyoto University, Kyoto, Japan **471**

4:00 p.m.

- 18.5 Shallow Source/Drain Extensions for pMOSFETs with High Activation and Low Process Damage Fabricated by Plasma Doping,** M. Takase, K. Yamashita, A. Hori and B. Mizuno, Matsushita Electric Ind., Co. Ltd., Osaka, Japan **475**

4:25 p.m.

- 18.6 A Raised Source/Drain Technology Using In-situ P-doped SiGe and B-doped Si for 0.1- μ m CMOS ULSIs,** T. Uchino, T. Shiba, K. Ohnishi, A. Miyauchi*, M. Nakata*, Y. Inoue* and T. Suzuki*, Hitachi Ltd., Tokyo, Japan, *Hitachi Ltd., Ibaraki, Japan **479**

4:50 p.m.

- 18.7 Practical Application of 2-D Optical Proximity Corrections for Enhanced Performance of 0.25 μ m Random Logic Devices,** H. Chuang, P. Gilbert, W. Grobmann, M. Kling, K. Lucas, A. Reich, B. Roman, E. Travis, P. Tsui, J. West and T. Vuong, Motorola, Austin, TX **483**

Session 19: Modeling and Simulation—Process Modeling I **487**

Tuesday, December 9, 2:15 p.m.
Georgetown Room

Co-Chairs: Paul Packan, Intel Corp.
James B. Kuo, National Taiwan University

2:20 p.m.

- 19.1 Modeling of Ultra-Low Energy Boron Implantation in Silicon,** G. Hobler, H.H. Vuong, J. Bevk, A. Agarwal, H. Gossmann, D. Jacobson, M. Foad*, A. Murrell* and E. Erokhin**, Lucent Technologies, Bell Labs, Murray Hill, NJ and *Applied Materials, West Sussex, UK and **Eaton Corp., Beverly, MA **489**

2:45 p.m.

- 19.2 A Physics-Based Modeling Approach for the Simulation of Anomalous Boron Diffusion and Clustering Behaviors,** A.D. Lilak, M.E. Law, K.S. Jones, M.D. Giles* and S.K. Earles, University of Florida, Gainesville, FL and *Intel Corporation, Santa Clara, CA **493**

3:10 p.m.

- 19.3 Experiments and Modeling of Boron Segregation in As Implanted Si During Annealing,** R.D. Chang, P. Choi, D. Wristler* and D.L. Kwong, The University of Texas, Austin, TX and Advanced Micro Devices, Austin, TX **497**

3:35 p.m.

- 19.4 Damage Calibration Concept and Novel B Cluster Reaction Model for B Transient Enhanced Diffusion over Thermal Process Range from 600°C (839 h) to 1100°C (5 s) with Various Ion Implantation Doses and Energies,** K. Suzuki, T. Miyashita, Y. Tada*, A. Hoefler, N. Strecker* and W. Fichtner*, Fujitsu Laboratories, Ltd., Atsugi, Japan and *Swiss Federal Institute of Technology, Zurich, Switzerland **501**

4:00 p.m.

- 19.5 A New Clustering Model for Runaway Boron Pile-Up Effect,** M. Orlowski, Motorola, Moscow Research Lab, Moscow, Russia **505**

4:25 p.m.

- 19.6 Simulation of Transient Enhanced Diffusion Using Computationally Efficient Models,** S. Yu, H. Kennel, M. Giles and P. Packan, Intel Corp., Hillsboro, OR **509**

Session 20: Detectors, Sensors and Displays—TFT Technology **513**

Tuesday, December 9, 2:15 p.m.
Monroe Room

Co-Chairs: Yoshiyuki Kaneko, Hitachi, Ltd.
Savvas Chamberlain, DALSA, Inc.

2:20 p.m.

- 20.1 A Simple Polysilicon TFT Technology for Display Systems on Glass,** A. Kumar and J. Sin, Hong Kong University of Science and Technology, Hong Kong, P.R. of China **515**

2:45 p.m.

- 20.2 Suppressed Short-Channel Effects and Improved Stability in Polysilicon Thin Film Transistors with Very Thin ECR N_2O -Plasma Gate Oxide,** J.W. Lee, N.I. Lee, S.H. Hur and C.H. Han, KAIST, Taejeon, Korea **519**

3:10 p.m.

- 20.3 A Novel Self-Aligned Gate-Overlapped LDD Poly-Si TFT with High Reliability and Performance,** M. Hatano, H. Akimoto and T. Sakai, Hitachi, Ltd., Tokyo, Japan **523**

3:35 p.m.

- 20.4 Analysis of Threshold Voltage Shift Caused by Bias Stress in Low Temperature Poly-Si TFTs,** S. Inoue, H. Ohshima and T. Shimoda, Seiko Epson Corporation, Nagano, Japan **527**

4:00 p.m.

- 20.5 Advances in Amorphous Silicon Technology for LCDs,** T. Tsukada, Hitachi, Ltd., Tokyo, Japan **531**

4:25 p.m.

- 20.6 Thin Film Transistors for Foldable Displays,** E. Ma, S. Theiss, M. Lu, C.C. Wu, J. Sturm and S. Wagner, Princeton University, Princeton, NJ **535**

4:50 p.m.

- 20.7 Pentacene Thin Film Transistors and Inverter Circuits,** H. Klauk, Y.Y. Lin, D.J. Gundlach and T.N. Jackson, Pennsylvania State University, University Park, PA **539**

Session 21: Quantum Electronics and Compound Semiconductors—FETs **543**

Tuesday, December 9, 2:15 p.m.
Thoroughbred Room

Co-Chairs: Jon Abrokwhah, Motorola, Inc.
Giovanni Ghione, Politecnico di Torino

2:20 p.m.

- 21.1 Oxide Based Compound Semiconductor Electronics,** U. Mishra, P. Parikh, P. Chavarkar, J. Yen, J. Champlain, B. Thibeault*, H. Reese, S.S. Shi, E. Hu, L. Zhu and J. Speck, University of California, Santa Barbara, CA and *WiTech, Goleta, CA **545**

2:45 p.m.
21.2 Dual Material Gate Field Effect Transistor (DMGFET), W. Long and K.K. Chin, New Jersey Institute of Technology, Newark, NJ **549**

3:10 p.m.
21.3 On-State Breakdown in High-Power HEMTs: Measurements and Modeling, M. Somerville, R. Blanchard, J. del Alamo, G. Duh* and P.C. Chao*, Massachusetts Institute of Technology, Cambridge, MA and *Sanders, Nashua, NH **553**

3:35 p.m.
21.4 A GaAs Power FET with Zero-Temperature-Coefficient, T. Tanaka, H. Furukawa and D. Ueda, Matsushita Electronics Corp., Osaka, Japan **557**

4:00 p.m.
21.5 High-Performance 0.25 μ m Gate-Length Doped-Channel AlGaIn/GaN Heterostructure Field Effect Transistors Grown on p-Type SiC Substrates, A.T. Ping, Q. Chen*, J.W. Yang*, M.A. Khan* and I. Adesida, University of Illinois, Urbana, IL and *APA Optics, Inc., Blaine, MN **561**

4:25 p.m.
21.6 Novel High Power AlGaIn/GaN HFETs on SiC Substrates, R. Gaska, J. Yang, A. Osinsky, M.A. Khan, M.S. Shur*, APA Optics, Blaine, MN and *Rensselaer Polytechnic Institute, Troy, NY **565**

4:50 p.m.
21.7 High Performance and Large Area Flip-Chip Bonded AlGaIn/GaN MODFETs, B. Thibeault, B. Keller, Y. Wu*, P. Fini*, U. Mishra, C. Nguyen**, N. Nguyen** and M. Le**, Widegap Technology, Goleta, CA and *University of California, Santa Barbara, CA and **Hughes Research Labs, Malibu, CA **569**

Session 22: 1997 IEDM Evening Panel Discussion **573**

Tuesday, December 9, 8:00 p.m.
International Ballroom Center

Manufacturing in the next millenium. The Emerging Role of Foundries in Silicon Technology.

Panel Moderator: Paul Fahey, Intel

Session 23: 1997 IEDM Evening Panel Discussion **575**

Tuesday, December 9, 8:00 p.m.
International Ballroom Center

Lithography for 100 nm Device Fabrication

Panel Moderator: Bill Arnold, AMD

Session 24: Integrated Circuits—Large Scale SOI ICs **577**

Wednesday, December 10, 9:00 a.m.
International Ballroom Center

Co-Chairs: Fumio Ootsuka, Hitachi, Ltd.
 Fred Perner, Hewlett-Packard

9:05 a.m.
24.1 1 Giga Bit SOI DRAM with Fully Bulk Compatible Process and Body-Contacted SOI MOSFET Structure, Y.H. Koh, M.R. Oh, J.W. Lee, J.W. Yang, W.C. Lee, C.K. Park, J.B. Park, Y.C. Heo, K.M. Rho, B.C. Lee, M.J. Chung, M. Huh, H.S. Kim, K.S. Choi, W.C. Lee, J.K. Lee, K.H. Ahn, K.W. Park, J.Y. Yang, D.H. Lee, I.S. Hwang and H.K. Kim, Hyundai Electronics Industries, Co., Ltd., Kyungki-do, Korea **579**

9:30 a.m.
24.2 A 2.0V, 0.35 μ m Partially Depleted SOI-CMOS Technology, K. Mistry, G. Grula, J. Sleight, L. Bair, R. Stephany, R. Flatley and P. Skerry, Digital Equipment Corp., Hudson, MA **583**

9:55 a.m.
24.3 A 0.25 μ m CMOS SOI Technology and its Application to 4 Mb SRAM, D. Schepis, F. Assaderaghi, D. Yee, W. Rausch, R. Bolam, A. Ajmera, E. Leobandung, S. Kulkarni, R. Flaker, D. Sadana, H. Hovel, T. Kebede, C. Schiller, S. Wu, L. Wagner, M.J. Saccamango, S. Ratanaphanyarat, J.B. Kuang, M. Hsieh, K. Tallman, R. Martino, D. Fitzpatrick, D. Badami, M. Hakey, S. Chu, B. Davari and G. Shahidi, IBM, Hopewell Junction, NY **587**

10:20 a.m.
24.4 Scalability of Partially Depleted SOI Technology for Sub-0.25 μ m Logic Applications, R. Chau, M. Alavi, R. Arghavani, D. Douglas, J. Greason, R. Green, C. Liang, J. Xu, P. Packan, S. Tyagi and S. Yu, Intel Corporation, Hillsboro, OR **591**

Session 25: Device Interconnect Technology—FeRAM **595**

Wednesday, December 10, 9:00 a.m.
International Ballroom West

Co-Chairs: Sang-In Lee, Samsung Electronics Co.
 Tadashi Nishimura, Mitsubishi Electric Corp.

9:05 a.m.
25.1 Highly-Reliable Ferroelectric Memory Technology with Bismuth-Layer Structured Thin Films (Y-1 Family), E. Fujii, T. Otsuki, Y. Judai*, Y. Shimada, M. Azuma, Y. Uemoto, Y. Nagano, T. Nasu, Y. Izutsu, A. Matsuda, K. Nakao, K. Tanaka, K. Hirano*, T. Ito*, T. Mikawa*, T. Kutsunai*, L. McMillan** and C.A. Paz de Araujo**, Matsushita Electronics Corp., Osaka, Japan and *Matsushita Electronics Corp., Kyoto, Japan and **Symetrix Corp., Colorado Springs, CO **597**

9:30 a.m.
25.2 Preparation of SrBi₂Ta₂O₉ Thin Films with Ultra-High Resistance to Annealing in Hydrogen Atmosphere for Ferroelectric Memories, T. Kanehara, I. Koiwa, Y. Okada, K. Ashikaga, H. Katoh and K. Kaifu, Oki Electric Industry Co. Ltd., Hachioji, Japan **601**

9:55 a.m.
25.3 Crystal-Orientation Controlled PZT FeRAM-Capacitors Using RF Magnetron Sputtering with 12 Φ Single Target, N. Inoue, Y. Maejima and Y. Hayashi, NEC Corp., Kanagawa, Japan **605**

10:20 a.m.
25.4 A High Stability Electrode Technology for Stacked SrBi₂Ta₂O₉ Capacitors Applicable to Advanced Ferroelectric Memory, J. Kudo, Y. Ito, S. Mitarai, N. Ogata, S. Yamazaki, H. Urashima, A. Okutoh, M. Nagata and K. Ishihara, Sharp Corporation, Nara, Japan **609**

10:45 a.m.
25.5 Advanced 0.5 μ m FRAM Device Technology with Fully Compatibility of Half-Micron CMOS Logic Device, T. Yamazaki, K.I. Inoue, H. Miyazawa, M. Nakamura, N. Sashida, R. Satomi, A. Kerry, Y. Katoh, H. Noshiro, K. Takai, R. Shinohara, C. Ohno, T. Nakajima, Y. Furumura and S. Kawamura, Fujitsu Ltd., Kawasaki, Japan **613**

11:10 a.m.
25.6 Ultra-Thin EBL (Encapsulating Barrier Layer) for Ferroelectric Capacitor, I.S. Park, Y.K. Kim, S.M. Lee, J.H. Chung, S.B. Kang, C.S. Park, C.Y. Yoo, S.I. Lee and M.Y. Lee, Samsung Electronics, Co., Kyungki-Do, Korea **617**

11:35 a.m.
25.7 SrBi₂Ta₂O₉ Thin Film Capacitor Model Including Polarization Reversal Response for Nanosecond Range Circuit Simulation of Ferroelectric Nonvolatile Memory, M. Takeo, M. Azuma, H. Hirano, K. Asari, N. Moriwaki, K.I. Tatsuuma and T. Otsuki, Matsushita Electronics Corp., Kyoto, Japan **621**

Session 26: CMOS Devices and Reliability—Gate Electrode and Dielectrics **625**

Wednesday, December 10, 9:00 a.m.
International Ballroom East

Co-Chairs: Jeong-Mo Hwang, LG Semicon Co., Ltd.
Hisayo Momose, Toshiba Corp.

9:05 a.m.

- 26.1 Flat-Band Voltage Shifts in P-MOS Devices Caused by Carrier Activation in P⁺-Polycrystalline Silicon and Boron Penetration**, T. Aoyama, K. Suzuki, H. Tashiro, Y. Tada and H. Arimoto, Fujitsu Labs, Ltd., Atsugi, Japan 627

9:30 a.m.

- 26.2 Effects of Gate Depletion and Boron Penetration on Matching of Deep Submicron CMOS Transistors**, H. Tuinhout, A. Montree, J. Schmitz and P. Stolk, Philips Research Labs, Eindhoven, The Netherlands 631

9:55 a.m.

- 26.3 Gate Electrode Microstructure Having Stacked Large-Grain Poly-Si with Ultra-Thin SiO_x Interlayer for Reliability in Sub-Micrometer CMOS**, H. Ito, M. Sasaki, N. Kimizuka, K. Uwasawa, N. Nakamura, T. Ito, Y. Goto, A. Tsuboi, S. Watanuki, T. Ueda and T. Horiuchi, NEC Corporation, Kanagawa, Japan 635

10:20 a.m.

- 26.4 Performance and Reliability Assessment of Dual-Gate CMOS Devices with Gate Oxide Grown on Nitrogen Implanted Si Substrates**, Y. Chen, I.M. Liu, M. Gardner*, J. Fulford* and D.L. Kwong, University of Texas, Austin, TX and *Advanced Micro Devices, Austin, TX 639

10:45 a.m.

- 26.5 Electrical Characteristics and Reliability of Sub 3 nm Gate Oxides Grown on Nitrogen Implanted Silicon Substrates**, L.K. Han, S. Crowder, M. Hargrove, E. Wu, S.H. Lo, F. Guarin, E. Crabbé and L. Su, IBM SRDC, Hopewell Junction, NY 643

11:10 a.m.

- 26.6 Application of JVD Nitride Gate Dielectric to A 0.35 Micron CMOS Process for Reduction of Gate Leakage Current and Boron Penetration**, H.-H. Tseng, P. Tsui, P.J. Tobin, J. Mogab, M. Khare*, X.W. Wang*, T.P. Ma*, R. Hegde, C. Hobbs, J. Veteran, M. Hartig, G. Kenig, V. Wang, R. Blumenthal, R. Cotton, V. Kaushik, T. Tamagawa**, B.L. Halpern**, G.J. Cui** and J.J. Schmitt**, Motorola, Austin, TX and *Yale University, New Haven, CT and **Jet Process Corporation 647

11:35 a.m.

- 26.7 High Performance 20Å NO Oxynitride for Gate Dielectric in Deep Sub-Quarter Micron CMOS Technology**, B. Maiti, P. Tobin, V. Misra, R. Hegde, K. Reid and C. Gelatos, Motorola, Austin, TX 651

Session 27: Device Interconnect Technology—Device Isolation Technology 655

Wednesday, December 10, 9:00 a.m.
Jefferson Room

Co-Chairs: Erwin Hammerl, Siemens
Dale Hetherington, Sandia

9:05 a.m.

- 27.1 A Shallow Trench Isolation for Sub-0.13µm CMOS Technologies**, N. Nandakumar, S. Sridhar, S. Nag, P. Mei, D. Rogers, M. Hanratty, A. Amerasekera and I.C. Chen, Texas Instruments, Dallas, TX 657

9:30 a.m.

- 27.2 A Highly Manufacturable Corner Rounding Solution for 0.18µm Shallow Trench Isolation**, C.P. Chang, C.S. Pai, F.H. Baumann, C.T. Liu, C.S. Rafferty, M.R. Pinto, E.J. Lloyd, M. Bude, F.P. Klemens, J.F. Miner, K.P. Cheung, J.I. Colonell, W.Y.C. Lai, H. Vaidya, S.J. Hillenius, R.C. Liu and J.T. Clemens, Bell Labs, Lucent Technology, Murray Hill, NJ 661

9:55 a.m.

- 27.3 Corner Field Effect of the CMP Oxide Recess in Shallow Trench Isolation Technology for High Density Flash Memories**, D. Shum, J. Higman, M. Khazhinsky, K. Wu, S. Kao, J. Burnett and C. Swift, Motorola, Austin, TX 665

10:20 a.m.

- 27.4 Stress Minimization in Deep Sub-Micron Full CMOS Devices by Using an Optimized Combination of the Trench Filling CVD Oxides**, M.H. Park, S.H. Hong, S.J. Hong, T. Park, S. Song, J.H. Park, H.S. Kim, Y.G. Shin, H.K. Kang and M.Y. Lee, Samsung Electronics Co. Ltd., Kyungki-Do, Korea 669

10:45 a.m.

- 27.5 Highly Reliable Double Well in Thin-p⁺ on p⁺ Epitaxial Wafer for Logic Embedded DRAM**, T. Yamashita, S. Komori, K. Horita, Y. Kawasaki, Y. Inoue and T. Nishimura, Mitsubishi Electric Corporation, Hyogo, Japan 673

Session 28: Modeling and Simulation—Process Modeling II 677

Wednesday, December 10, 9:00 a.m.
Georgetown Room

Co-Chairs: Shukla Kapur, IBM
Peter Griffin, Stanford University

9:05 a.m.

- 28.1 Suppression of Reverse and Short Channel Effect by High Energy Implantation**, S. Chaudhry, C. Rafferty*, W. Nagy, Y. Chyan, M. Carroll, A. Chen and K. Lee, Bell Laboratories, Lucent Technologies, Orlando, FL and *Bell Laboratories, Lucent Technologies, Murray Hill, NJ 679

9:30 a.m.

- 28.2 Inverse Modeling of MOSFETs Using I-V Characteristics in the Subthreshold Region**, Z.K. Lee, M.B. McIlrath and D. Antoniadis, Massachusetts Institute of Technology, Cambridge, MA 683

9:55 a.m.

- 28.3 An Advanced MOSFET Design Approach and a Calibration Methodology Using Inverse Modeling that Accurately Predicts Device Characteristics**, A. Das, D. Newmark, I. Clejan, M. Foisy, M. Sharma, S. Venkatesan, S. Veeraraghavan, V. Misra, B. Gadepally and L. Parillo, Motorola, Austin, TX 687

10:20 a.m.

- 28.4 Junction Delineation of 0.15µm MOS Devices Using Scanning Capacitance Microscopy**, R.N. Kleiman, M.L. O'Malley, F.H. Baumann, J.P. Garbo and G.L. Timp, Bell Laboratories, Lucent Technologies, Murray Hill, NJ 691

10:45 a.m.

- 28.5 Impact of Nitrogen Implant Prior to the Gate Oxide Growth on Transient Enhanced Diffusion**, A. Kamgar, H.H. Vuong, C.T. Liu, C.S. Rafferty and J.T. Clemens, Bell Laboratories, Lucent Technologies, Murray Hill, NJ 695

11:10 a.m.

- 28.6 Diffusion Mechanism Study of Arsenic in SiO₂, Using Oxygen Isotope ¹⁸O as a Component Element of Matrix SiO₂**, Y. Tsunashima and N. Aoki, Toshiba Corporation, Yokohama, Japan 699

11:35 a.m.

- 28.7 Oxygen Vacancy with Large Lattice Distortion as Origin of Leakage Currents in SiO₂**, A. Yokozawa, A. Oshiyama*, Y. Miyamoto** and S. Kumashiro, NEC Corp., Kanagawa, Japan and *University of Tsukuba, Ibaraki, Japan and **NEC, Ibaraki, Japan 703

Session 29: Detectors, Sensors and Displays—Field Emitter Arrays and Advanced Electron Sources 707

Wednesday, December 10, 9:00 a.m.
Monroe Room

Co-Chairs: Kevin Jensen, Naval Research Laboratory
Kozo Orihara, NEC Corporation