

international
**ELECTRON
DEVICES**
meeting

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DECEMBER 8-11, 1996

TECHNICAL DIGEST

iee

1996 International Electron Devices Meeting

TECHNICAL DIGEST

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WELCOME FROM THE GENERAL CHAIR

001564

The Conference Committee and I welcome you to the 1996 IEEE International Electron Devices Meeting. This year the conference returns to San Francisco and continues a 42 year tradition as the premier forum for the presentation of the latest research and development in the area of electron devices and their applications. The conference reflects the strong international nature of our industry with invited speakers and contributed papers from major semiconductor centers from around the world.

This year we are introducing two new features to the IEDM to improve the accessibility of the information in the abstracts. We have included 50 word abstracts on the IEDM home page which are available now (please visit our site at <http://www.ieee.org/conference/iedm>). We are also introducing the digest in a CD ROM version that will be distributed along with the technical digest.

Two short courses are scheduled for Sunday. These are designed for broad appeal to the IEDM participants including those unfamiliar with the topics. The courses cover the topics of DRAM technology trends and the issues of the back end modules. Both of these courses are organized and lectured by active researchers and represent the world experts in these fields.

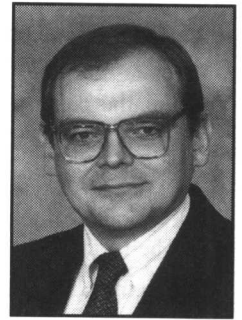
The plenary talks on Monday feature the topics of micro-mechanical systems, silicon on insulator technology and the silicon foundry business featuring speakers from North America, Europe, and Asia.

This years Luncheon speaker will be Dr. Gordon Moore, co-founder and Chairman of the Board of Intel, speaking on "Silicon Device Fabrication Technology Revisited". Dr. Moore's talk will address the complex technology trends.

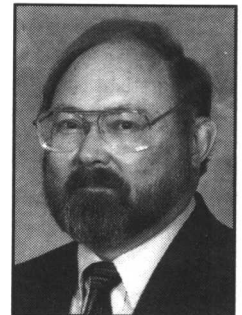
On Tuesday night, two panel sessions are planned on the diverse topics of system on a chip applications and the people issues of semiconductor development.

On behalf of the IEEE Electron Devices Society, which sponsors the IEDM, Ken Galloway, Technical Program Chairman and Pierre Woerlee, Technical Program Vice Chairman, I wish to express my sincere appreciation and congratulations to the members of the conference committee for the outstanding job they have done in planning and organizing the 1996 meeting. The authors are to be commended for their efforts in preparing and presenting the high-quality papers that form the foundation of this conference.

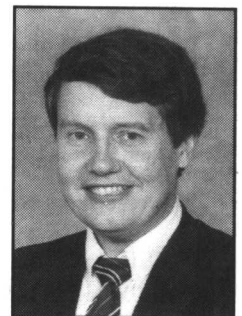
It is with great pleasure that I extend a warm welcome to them and to all of the attendees of the 1996 IEEE International Electron Devices Meeting.



Steve Hillenius
General Chair



Ken Galloway
Technical Program
Chair



Pierre Woerlee
Technical Program
Vice Chair



SBO 8302

AWARD PRESENTATIONS

PLENARY SESSION Monday, December 9

1995 Roger A. Haken Best Student Paper Award:

To: Scott Crowder, Stanford University, Stanford, CA

For the paper entitled: "The Effect of Source/Drain Processing on the Reverse Short Channel Effect of Deep Sub-Micron Bulk and SOI NMOSFETs".

Paul Rappaport Award

To: Reinout Woltjer, Ger Paulzen, Henk Pomp, Herbert Lifka and Pierre Woerlee, Philips Research Laboratory, Eindhoven, The Netherlands

For the paper entitled: "Three Hot-Carrier Degradation Mechanisms in Deep Submicron PMOSFETs"

EDS Distinguished Service Award

To: Alfred U. MacRae,
Berkley Heights, NJ

"To recognize and honor outstanding service to the Electron Devices Society"

J.J. Ebers Award

To: Tetsushi Sakai
NTT Electronics Technology Corporation, Kanagawa, Japan

"For outstanding technical contributions to electron devices"

IEDM LUNCHEON Tuesday, December 10

1996 IEEE Clelio Brunetti Award

To: Mitsumasa Koyanagi (SM'IEEE), Tohoku University, Sendai, Japan

"For pioneering research and development of the three dimensional stacked capacitor DRAM cell."

1996 IEEE Morris N. Liebmman Memorial Award

To: Seiki R. Ogura (F'IEEE), IBM Corporation, Hopewell Junction, NY

"For contributions to and leadership in the development of the lightly doped drain silicon field effect transistor (LDDFET)."

1996 IEEE Jack A. Morton Award

To: Robert W. Dutton (F'IEEE), Stanford University, Stanford, CA

"For seminal contributions to semiconductor process and device modeling."

1996 IEEE David Sarnoff Award

To: Hiroyuki Sakaki (SM'IEEE), University of Tokyo, Tokyo, Japan

"For pioneering studies of quantum effects in semiconductor microstructures."

LUNCHEON PRESENTATION

"Silicon Device Fabrication Technology Revisited" a presentation by Gordon E. Moore, Chairman of the Board, Intel.

CONFERENCE HIGHLIGHTS

Date	Time	Place	Event
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12/9	9:00 a.m. - 12:00 p.m.	Continental Ballrooms 1-9	Plenary Session
12/9	6:00 p.m. - 7:00 p.m.	Continental Ballrooms 1-9	Reception
12/10	9:00 a.m. - 11:35 a.m.	Continental Ballroom 4	Emerging Technologies Session
12/10	12:20 p.m. - 2:00 p.m.	Grand Ballroom B	Luncheon
12/10	8:00 p.m. - 10:00 p.m.	Continental Ballrooms 1-4 & 6-9	Panel Sessions

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Technical Program Chair: Ken Galloway

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- 1.2 **Microelectromechanical Systems: Interfacing Electronics to a Non-Electronic World**, K. Wise, University of Michigan, Ann Arbor, MI
- 1.3 **Foundry Technologies**, F. Tseng, Vanguard International Semiconductor Corp., Taiwan, Rep. of China

Session 2: Quantum Electronics and Compound Semiconductor Devices—HEMTs

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Co-Chairs: Takatomo Enoki, NTT System Electronics Lab
Julia Brown, Hughes Research Labs

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Session 7: Integrated Circuits—Non-Volatile Memory Technology

Monday, December 9, 1:30 p.m.
Imperial Room

Co-Chairs: Paolo Cappelletti, SGS-Thomson
Seichi Mori, Toshiba Corporation

1:30 p.m.

Introduction

1:35 p.m.

- 7.1 **Multilevel FLASH Cells and Their Trade-Offs**, (Invited Paper) B. Eitan, R. Kazerounian, A. Roy, G. Crisenza*, P. Cappelletti* and A. Modelli*, WSI, Inc., Fremont, CA and *SGS-Thomson, Agrate, Italy

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2:00 p.m.

- 7.2 **A New Shared Bit Line NAND Cell Technology for the 256 Mb Flash Memory with 12V Programming**, W.C. Shin, J.D. Choi, D.J. Kim, J. Kim, H.S. Kim, K.M. Mang, C.H. Chung, S.T. Ahn, O.H. Kwon, Samsung Electronics Co., Ltd., Kyungki-Do, Korea

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2:25 p.m.

- 7.3 **A Shallow-Trench Isolation Flash Memory Technology with a Source-Bias Programming Method**, M. Kato, T. Adachi and T. Tanaka, Hitachi, Ltd., Tokyo, Japan

177

2:50 p.m.

- 7.4 **Novel Self-Limiting Program Scheme Utilizing N-channel Select Transistors in P-channel DINOR Flash Memory**, T. Ohnakado, H. Takada, K. Hayashi, K. Sugahara, S. Satoh and H. Abe, Mitsubishi Electric Corp., Hyogo, Japan

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3:15 p.m.

- 7.5 **New Interconnect Plasma Induced Damage Analyzed by Flash Memory Cell Array**, M. Takebuchi, K. Yamada, T. Nishimura, K. Isobe, T. Uemura, T. Fujimoto, M. Arakawa, S. Mori, A. Kimitsuka and Y. Yoshikawa, Toshiba Corporation, Kawasaki, Japan

185

3:40 p.m.

- 7.6 **A Novel High-Density Low-Cost Diode Programmable Read Only Memory**, C. DeGraaf, P. Woerlee, C. Hart, H. Lifka, P. de Vreede, P. Janssen, F. Sluijs and B. Paulzen, Philips Research Labs, Eindhoven, The Netherlands

189

4:05 p.m.

- 7.7 **High Density Nonvolatile Magnetorestrictive RAM**, S. Tehrani, E. Chen, M. Durlam, T. Zhu and H. Goronkin, Motorola, Inc., Tempe, AZ

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Session 8: Quantum Electronics and Compound Semiconductor Devices—III-V HBTs and MESFETs

Tuesday, December 10, 9:00 a.m.
Continental Ballrooms 1-3

Co-Chairs: Darrell Hill, Texas Instruments
Lovell Carnnitz, Hewlett-Packard

9:00 a.m.

Introduction

9:05 a.m.

- 8.1 **InP-Based HBT Technology for Millimeter-Wave MMIC VCOs**, J. Cowles, L. Tran, H. Wang, E. Lin, T. Block, D. Streit and A. Oki, TRW Space & Electronics Group, Redondo Beach, CA

199

9:30 a.m.

- 8.2 **Hydrogen-Related Burn-in in GaAs/AlGaAs HBTs and Implications for Reliability**, T. Henderson, V. Ley, T. Kim, T. Moise and D. Hill, Texas Instruments Corporate R&D, Dallas, TX

203

9:55 a.m.

- 8.3 **InGaP/GaAs HBT with Novel Layer Structure for Emitter Ledge Fabrication**, M. Fresina, Q. Hartmann, S. Thomas, D. Ahmari, D. Caruth, M. Feng and G. Stillman, University of Illinois, Urbana, IL

207

10:20 a.m.

- 8.4 **A 0.1 μ m Self-Aligned-Gate GaAs MESFET with Multilayer Interconnection Structure for Ultra-High-Speed ICs**, M. Tokumitsu, M. Hirano, T. Otsuji, S. Yamaguchi and K. Yamasaki, NTT LSI Lab, Kanagawa, Japan

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10:45 a.m.

- 8.5 **A Novel Fabrication Technology for Integrating FETs and High-Performance Diodes, and Its Application to MMIC VCO**, J.-W. June, Y.-S. Kwon, KAIST, Taejeon, Korea

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11:10 a.m.

- High Temperature MESFET Based Integrated Circuits Operating up to 300°C**, J. Würfl, B. Janke, E. Nebauer, S. Thierbach and P. Wolter, Ferdinand-Braun-Institut, Berlin, Germany

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Session 9: Emerging Technologies

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Tuesday, December 10, 9:00 a.m.
Continental Ballroom 4

Co-Chair: Judy Hoyt, Stanford University

9:00 a.m.

Introduction

9:05 a.m.

- 9.1 **SIC Electronics (Invited Paper)**, A. Agarwal, G. Augustine, V. Balakrishna, C.D. Brandt, A.A. Burk,* L.-S. Chen*, R.C. Clarke, P.M. Esker*, A.M. Hobgood, R.H. Hopkins, A.W. Morse*, L.B. Rowland, S. Seshadri, R.R. Siegiej, T.N. Smith Jr. and S. Sriram, Northrop Grumman Science & Technology Center, Pittsburgh, PA, *Northrop Grumman Corp., Baltimore, MD

225

9:55 a.m.

- 9.2 **Recent Progress in Crystal Growth, Conductivity Control and Light Emitters of Group III Nitride Semiconductors (Invited Paper)**, I. Akasaki and H. Amano, Meijo University, Nagoya, Japan

231

10:45 a.m.

- 9.3 **Biomedical Applications of MEMs (Invited Paper)**, K. Peterson, Cepheid

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Session 10: Solid State Devices—Silicon Heterostructures and Novel Devices

243

Tuesday, December 10, 9:00 a.m.
Continental Ballroom 5

Co-Chairs: John Cressler, Auburn University
Khalid Ismail, Cairo University

9:00 a.m.

Introduction

9:05 a.m.

- 10.1 Sub-10-fJ ECL/68 μ A 4.7-GHz Divider Ultra-Low-Power SiGe Base Bipolar Transistors with a Wedge-Shaped CVD-SiO₂ Isolation Structure and a BPSG-Refilled Trench**, M. Kondo, K. Oda, E. Ohue, H. Shimamoto*, M. Tanabe*, T. Onai and K. Washio, Hitachi, Ltd., Tokyo, Japan and *Hitachi Device Engineering, Co. Ltd., Tokyo, Japan

245

9:30 a.m.

- 10.2 Suppression of Boron Outdiffusion in SiGe HBTs by Carbon Incorporation**, L. Lanzerotti, J. Sturm, E. Stach*, R. Hull*, T. Buyuklimanli** and C. Magee**, Princeton University, Princeton, NJ, *University of Virginia, Charlottesville, VA and **Evans East, Plainsboro, NJ

249

9:55 a.m.

- 10.3 Impact of Profile Scaling on High-Injection Barrier Effects in Advanced UHV/CVD SiGe HBTs**, A. Joseph, J. Cressler, D. Richey and D. Harame*, Auburn University, Auburn, AL and *IBM Microelectronics Division, Hopewell Junction, NY

253

10:20 a.m.

- 10.4 Effect of Carbon on the Valence Band Offset of Si_{1-x-y}Ge_xC_y/Si Heterojunctions**, C. Chang, A. St. Armour and J. Sturm, Princeton University, Princeton, NJ

257

10:45 a.m.

- 10.5 Novel SiGeC Channel Heterojunction PMOSFET**, S. Ray, S. John, S. Oswal and S. Banerjee, University of Texas, Austin, TX

261

11:10 a.m.

- 10.6 Room Temperature Negative Differential Conductance in Three-Terminal Silicon Surface Tunneling Device**, J. Koga and A. Toriumi, Toshiba Corp., Kawasaki, Japan

265

Session 11: Integrated Circuits—Advanced SRAM Technology

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Tuesday, December 10, 9:00 a.m.
Continental Ballroom 6

Co-Chairs: Morgan Thoma, Lucent Technologies
Nobuo Tamba, Hitachi, Ltd.

9:00 a.m.

Introduction

9:05 a.m.

- 11.1 Advanced SRAM Technology—The Race Between 4T and 6T Cells** (Invited Paper), C. Lage, J. Hayden and C. Subramanian, Motorola, Inc., Austin, TX

271

9:30 a.m.

- 11.2 A High-Density 6.9 sq. μ m Embedded SRAM Cell in a High-Performance 0.25 μ m-Generation CMOS Logic Technology**, S. Subbanna, P. Agnello, E. Crabbe, R. Schulz, S. Wu, K. Tallman, M. Saccamango, S. Greco, V. McGahay, A. Allen, B. Chen, T. Cotler, E. Eld, J. Lasky*, H. Ng, A. Ray, H. Snare, L. Su, D. Sunderland, J. Sun and B. Davari, IBM Microelectronics, Hopewell Junction, NY, *IBM Microelectronics, Burlington, NJ

275

9:55 a.m.

- 11.3 A C-Switch Cell for Low-Voltage Operation and High-Density SRAMS**, H. Kuriyama, Y. Ishigaki, Y. Fujii, S. Maegawa, S. Maeda, S. Miyamoto, K. Tsutsumi and H. Miyoshi, Mitsubishi Electric Corp., Hyogo, Japan

279

10:20 a.m.

- 11.4 A Highly Stable SRAM Memory Cell with Top-Gated P-N Drain Poly-Si TFTs for 1.5V Operation**, F. Hayashi, H. Ohkubo, T. Takahashi, S. Horiba, K. Noda, T. Uchida, T. Shimizu, N. Sugawara* and S. Kumashiro, NEC Corporation, Kanagawa, Japan and *NEC Infomatec Systems, Kawasaki, Japan

283

Session 12: Detectors, Sensors and Displays—Vacuum Microelectronics

287

Tuesday, December 10, 9:00 a.m.
Continental Ballrooms 7–9

Co-Chairs: Kevin Jensen, NRL
Rade Popovic, EPFL

9:00 a.m.

Introduction

9:05 a.m.

- 12.1 Molybdenum Field-Emitter Arrays**, C. Spindt and I. Brodie, SRI International, Menlo Park, CA

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9:30 a.m.

- 12.2 Enhancement of Electron Emission Efficiency and Stability of Molybdenum Field Emitter Array by Diamond-Like Carbon Coating**, J.H. Jung, B.K. Ju, Y.H. Lee, J. Jang* and M.H. Oh, Korea Institute of Science and Technology, Seoul, Korea and *Kyung-Hee University, Seoul, Korea

293

9:55 a.m.

- 12.3 Low Operation Voltage Field Emitter Arrays Using Low Work Function Materials Fabricated by Transfer Mold Technique**, M. Nakamoto, T. Hasegawa, T. Ono, T. Sakai and N. Sakuma, Toshiba Corporation, Kawasaki, Japan

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10:20 a.m.

- 12.4 A Novel Structure of Silicon Field Emission Cathode with Sputtered TiW for Gate Electrode and TEOS Oxide for Gate Dielectric**, S.W. Kang, J.H. Lee, Y.H. Song, B.G. Yu, K.I. Cho and H.J. Yoo, ETRI, Taejeon, Korea

301

10:45 a.m.

- 12.5 A Novel Lateral Field Emitter Triode with Insitu Vacuum Encapsulation**, C.M. Park, M.S. Lim, B-H. Min, M.K. Han and Y.I. Choi*, Seoul National University, Seoul, Korea and *Ajou University, Kyungki-do, Korea

305

11:10 a.m.

- 12.6 A MOSFET-Structured Si Tip for Stable Emission Current**, T. Hirano, S. Kanemaru and J. Itoh, Electrotechnical Laboratory, Ibaraki, Japan

309

11:35 a.m.

- Novel Single- and Double-Gate Race-Track-Shaped Field Emitter Structures**, B. Wang, J. Sin, J. Cai, M.C. Poon, Y. Tang*, C. Wang* and L. Tong*, Hong Kong University of Science and Technology, Kowloon, Hong Kong and *Southeast University, Peoples Rep. of China

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Session 13: CMOS Devices and Reliability—Thin Dielectrics

317

Tuesday, December 10, 9:00 a.m.
Imperial Room

Co-Chairs: John Chen, TSMC
Cary Yang, Santa Clara University

- 9:00 a.m.
Introduction
- 9:05 a.m.
13.1 Gate Oxide Scaling Limits and Projection (Invited Paper), C. Hu, University of California, Berkeley, CA, **319**
- 9:30 a.m.
13.2 Experimental Evidence of Inelastic Tunneling and New I-V Model for Stress-Induced Leakage Current, S. Takagi, N. Yasuda and A. Toriumi, Toshiba Corporation, Kawasaki, Japan **323**
- 9:55 a.m.
13.3 A New Polarity Dependence of the Reduced Trap Generation during High-Field Degradation of Nitrided Oxides, R. Degraeve, J. De Blauwe, J. Ogier, P. Roussel, G. Groeseneken and H. Maes, IMEC, Leuven Belgium **327**
- 10:20 a.m.
13.4 Leakage Current, Reliability Characteristics and Boron Penetration of Ultra-Thin (32–36Å) O₂-Oxide and N₂O/NO Oxynitrides, C. Lin, A. Chou, K. Kumar, P. Chowdhury and J. Lee, The University of Texas, Austin, TX **331**
- 10:45 a.m.
13.5 High Reliability of Nanometer-Range N₂O-Nitrided Oxides Due to Suppressing Hole Injection, K. Kobayashi, A. Teramoto, T. Nakamura*, H. Watanabe, H. Kurokawa**, Y. Matsui and M. Hirayama, Mitsubishi Electric Corp., Itami, Japan and *Ryoden Semiconductor System Eng. Corp., Itami, Japan and **Mitsubishi Electric Corp., Amagasaki, Japan **335**
- 11:10 a.m.
13.6 Improved Performance and Reliability of Split Gate Source-side Injected Flash Memory Cells, S. Bhattacharya, K. Lai, K. Fox, E. Worley, P. Chan, G. Li*, L. Hwang* and U. Sharma, Rockwell Semiconductor Systems, Newport Beach, CA and *University of California, Irvine, CA **339**
- 11:35 a.m.
13.7 A New Quantitative Model to Predict SILC-Related Disturb characteristics in Flash E²PROM Devices, J. DeBlauwe, J. Van Houdt, D. Wellekens, R. Degraeve, P. Roussel, L. Haspeslagh, L. Deferm, G. Groeseneken, H. Maes, IMEC, Leuven, Belgium **343**

Session 14: Device Interconnect Technology—Interconnects

Tuesday, December 10, 9:00 a.m.
Grand Ballroom A

Co-Chairs: Takamoro Kikkawa, NEC Corporation
Michel Lerme, CEA LETI CENG

- 9:00 a.m.
Introduction
- 9:05 a.m.
14.1 Slurry Engineering for Self-Stopping, Dishing Free SiO₂-CMP, H. Nojo, M. Kodera and R. Nakata, Toshiba corporation, Kawasaki, Japan **349**
- 9:30 a.m.
14.2 A Novel Low Temperature PVD Planarized Al-Cu Process for High Aspect Ratio Sub-Half Micron Interconnect, B. Zhao, M. Biberger*, V. Hoffman*, S.-Q. Wang, P. Vasudev and T. Seidel, SEMATECH, Austin, TX and *Varian Associates, Palo Alto, CA **353**

- 9:55 a.m.
14.3 Ion Metal Plasma (IMP) Deposited Titanium Liners for 0.25/0.18µm Multilevel Interconnections, G. Dixit, W. Hsu, A. Konecni, S. Krishnan, J. Luttmner, J. Forster*, G. Yao*, M. Narasimhan*, Z. Xu*, S. Ramaswami*, F. Chen* and J. Nulman*, Texas Instruments, Dallas, TX and *Applied Materials, Santa Clara, CA **357**
- 10:20 a.m.
14.4 A Novel TiN/Ti Contact Plug Technology for Gigabit Scale DRAM Using Ti-PECVD and TiN-LPCVD, K. Ohto, K. Urabe, T. Taguwa, S. Chikaki and T. Kikkawa, NEC Corp. Kanagawa, Japan **361**
- 10:45 a.m.
14.5 Barrier Metal Free Copper Damascene Interconnection Technology Using Atmospheric Copper Reflow and Nitrogen Doping in SiOF Film, K. Mikagi, H. Ishikawa, T. Usami, M. Suzuki, K. Inoue, N. Oda, S. Chikaki, I. Sakai and t. Kikkawa, NEC Corp., Kanagawa, Japan **365**
- 11:10 a.m.
14.6 Low-k Fluorinated Amorphous Carbon Interlayer Technology for Quarter Micron Devices, Y. Matsubara, K. Endo, T. Tatsumi, H. Ueno, K. Sugai, T. Horiuchi, NEC Corporation, Kanagawa, Japan **369**

Session 15: Modeling and Simulation—Device Modeling

Tuesday, December 10, 9:00 a.m.
Plaza Room

Co-Chairs: Franco Venturi, University of Parma
Hiroshi Iwai, Toshiba Corporation

- 9:00 a.m.
Introduction
- 9:05 a.m.
15.1 Hot-Carriers at Low Voltages: New Experimental Evidences and Open Issues (Invited Paper), L. Selmi, B. Fischer*, A. Ghetti and R. Bez**, University of Bologna, Bologna, Italy and *University of Hannover, Hannover, Germany and **SGS-Thomson Microelectronics, Agrate Brianza, Italy **375**
- 9:30 a.m.
15.2 Monte Carlo Simulation of Low Voltage Hot Carrier Effects in Non Volatile Memory Cells, A. Ghetti, L. Selmi, R. Bexz* and E. Sangiorgi**, University of Bologna, Bologna, Italy and *SGS-Thomson Microelectronics, Agrate Brianza, Italy and **University of Udine, Udine, Italy **379**
- 9:55 a.m.
15.3 Is There Experimental Evidence for a Difference Between Surface and Bulk Impact Ionization in Silicon?, C. Jungemann, S. Yamaguchi and H. Goto, Fujitsu, Ltd., Kawasaki, Japan **383**
- 10:20 a.m.
15.4 Scattering Theory of the Short Channel MOSFET, M. Lundstrom, Purdue University, West Lafayette, IN **387**
- 10:45 a.m.
15.5 Understanding the Differences in the Effective-Field Dependence of Electron and Hole Inversion Layer Mobilities, S. Jallepalli, W.-K. Shih, J. Bude*, M. Pinto*, C. Maziar and A. Tasch, University of Texas, Austin, TX and *Bell Labs, Lucent Technologies, Murray Hill, NJ **391**

11:10 a.m.

- 15.6 Effective Mobility in Heavily Doped n-MOSFETs: Measurements and Models**, S. Villa, A. Lacaita, L. Perron and R. Bez*, Politecnico di Milano, Milan, Italy and *SGS-Thomson Microelectronics, Agrate Brianza, Italy

395

11:35 a.m.

- 15.7 Investigation of Quantum Effects in Highly-Doped MOSFETs by Means of a Self-Consistent 2D Model**, A. Spinelli, A. Benvenuti* and A. Pacelli, Politecnico di Milano, Milan, Italy and *SGS-Thomson Microelectronics, Agrate Brianza, Italy

399

Session 16: Quantum Electronics and Compound Semiconductors—Lasers and Quantum Devices

403

Tuesday, December 10, 2:15 p.m.
Continental Ballrooms 1-3

Co-Chairs: Ming Wu, University of California
Mike Strosio, Army Research Office

2:15 p.m.

Introduction

2:20 p.m.

- 16.1 Micromachined Tunable Vertical Cavity Surface-Emitting Lasers**, M. Larson, F. Sugihwo, A. Massengale and J. Harris, Jr., Stanford University, Stanford, CA

405

2:45 p.m.

- 16.2 Extremely High-Power Operation of 650nm-Band AlGaInP Visible Lasers with Low Optical Absorption Mirrors**, T. Fukuhisa, I. Kidoguchi, H. Adachi, K. Tanaka, M. Mannoh and A. Takamori, Matsushita Electric Industrial Co., Ltd., Osaka, Japan

409

3:10 p.m.

- 16.3 First Fabrication of AlGaAs/GaAs Laser Diodes with GaAs Islands Active Regions on Si Grown by Droplet Epitaxy**, T. Egawa, A. Ogawa, T. Jimbo and M. Umeno, Nagoya Institute of Technology, Nagoya, Japan

413

3:35 p.m.

- 16.4 A Novel Electroluminescent Diode with Nanocrystalline Silicon Quantum Dots**, T. Yoshida, Y. Yamada and T. Orii*, Matsushita Research Institute Tokyo, Inc., Kawasaki, Japan and *University of Tsukuba, Ibaraki, Japan

417

4:00 p.m.

- 16.5 Dynamic Properties of InAs Self-Assembled Quantum Dots for Spectral Hole Burning Memory Application**, N. Horiguchi, T. Futatsugi, Y. Nakata and N. Yokoyama, Fujitsu Laboratories, Ltd., Atsugi, Japan

421

4:25 p.m.

- 16.6 RTD/HFET Low Standby Power SRAM Gain Cell**, J. van der Wagt, A. Seabaugh, E. Beam, Texas Instruments Inc., Dallas, TX

425

4:50 p.m.

- 16.7 Experimental Observation of Coulomb Staircase in an Asymmetric Tunnel Barrier System**, Y. Matsumoto, T. Hanajiri, T. Toyabe and T. Sugano*, Toyo University, Saitama, Japan and *The Institute of Physical and Chemical Research, Saitama, Japan

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Session 17: Device Interconnect Technology—Shallow Junction and Salicide Technologies

433

Tuesday, December 10, 2:15 p.m.
Continental Ballroom 4

Co-Chairs: Dale Hetherington, Sandia National Labs
David Thomas, IBM

2:15 p.m.

Introduction

2:20 p.m.

- 17.1 Novel Shallow Junction Technology Using Decaborane ($B_{10}H_{14}$)**, K. Goto, J. Matsuo*, T. Sugii, H. Minakata, I. Yamada* and T. Hisatsugu, Fujitsu Laboratories, Ltd., Atsugi, Japan and *Kyoto University, Kyoto, Japan

435

2:45 p.m.

- 17.2 δ -Doped Source/Drain 0.1 μ m n-MOSFETs with Extremely Shallow Junctions**, E. Murakami, K. Harada, D. Hisamoto and S.I. Kimura, Hitachi, Ltd., Tokyo, Japan

439

3:10 p.m.

- 17.3 A 0.18 μ m Ti-Salicided p-MOSFET with Shallow Junctions Fabricated by Rapid Thermal Processing in an NH₃ Ambient**, M. Segawa, T. Yabu, M. Arai, M. Moriwaki, H. Umimoto, M. Sekiguchi and A. Kanda, Matsushita Electric Industrial Co., Ltd., Osaka, Japan

443

3:35 p.m.

- 17.4 Highly Reliable W/TiN/pn-poly-Si Gate CMOS Technology with Simultaneous Gate and Source/Drain Doping Process**, H. Wakabayashi, T. Andoh, K. Sato, K. Yoshida, H. Miyamoto, T. Mogami and T. Kunio, NEC Corp., Kanagawa, Japan

447

4:00 p.m.

- 17.5 A Thermally Stable Ti-W Salicide for Deep-Submicron Logic with Embedded DRAM**, K. Fujii, K. Kikuta, K. Inoue, K. Mikagi,

451

4:25 p.m.

- 17.6 A Novel 0.15 μ m CMOS Technology Using W/WNx/Polysilicon Gate Electrode and Ti Silicided Source/Drain Diffusions**, M. Takagi, K. Miyashita, H. Koyama, K. Nakajima, K. Miyano, Y. Akasaka, Y. Hiura, S. Inaba, A. Azuma, H. Koike, H. Yoshimura, K. Suguro and H. Ishiuchi, Toshiba Corp., Kawasaki, Japan

455

4:50 p.m.

- 17.7 Novel Bulk Dynamic Threshold Voltage MOSFET (BDTMO) with Advanced Isolation (SITOS) and Gate to Shallow-Well Contact (SSS-C) Processes for Ultra Low Power Dual Gate CMOS**, H. Kotaki, S. Kakimoto, M. Nakano, T. Matsuoka, K. Adachi, K. Sugimoto, T. Fukushima and Y. Sato, Sharp corporation, Nara, Japan

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Session 18: Solid State Devices—Smartpower Devices and Technologies

463

Tuesday, December 10, 2:15 p.m.
Continental Ballroom 5

Co-Chairs: C. Andre Salama, University of Toronto
Hak-Yam Tsoi, Motorola

2:15 p.m.

Introduction

- 2:20 p.m.
18.1 Characteristics and Applications of 0.6 μ m Bipolar-CMOS-DMOS Technology Combining VLSI Non-Volatile Memories (Invited Paper), C. Contiero, P. Galbiati, M. Palmieri and L. Vecchi, SGS-Thomson Microelectronics, Milano, Italy **465**
- 2:45 p.m.
18.2 Optimized 25V, 0.34m Ω cm² Very-Thin-RESURF (VTR), Drain Extended IGFETs in a Compressed BiCMOS Process, C.Y. Tsai, J. Arch, T. Efland, J. Erdeljac, L. Hutter, J. Mitros, J.Y. Yang and H.T. Yuan, Texas Instruments, Dallas, TX **469**
- 3:10 p.m.
18.3 Fabrication of a 300V, High Current (300mA/Output) Smart-Power IC Using Gate-Controlled SCRs on Bonded SOI (BSOI) Technology, F. Gonzalez, V. Shekhar, C.K. Chan, B. Choy, and N. Chen, Supertex Inc., Sunnyvale, CA **473**
- 3:35 p.m.
18.4 New High voltage SOI Device Structure Eliminating Substrate Bias Effects, A. Nakagawa, Y. Yamaguchi, N. Yasuhara, K. Hirayama and H. Funaki, Toshiba Materials and Devices Lab., Kawasaki, Japan **477**
- 4:00 p.m.
18.5 Simulations and Measurements of Cross-Talk Phenomena in BiCMOS Technology for Hard Disk Drives, G. de Cremoux, E. Dubois, S. Bardy* and J. Lebailly*, IEMN/ISEN, Villeneuve d'Ascq, France and *Philips Semiconductors, Caen, France **481**
- 4:25 p.m.
18.6 Extraction of Channel Doping Profile in DMOS Transistors, A. Pieracci, M. Lanzoni, P. Galbiati*, S. Manzini*, C. Contiero* and B. Ricco, University of Bologna, Bologna, Italy and *SGS-Thomson Microelectronics, Milano, Italy **485**
- 4:50 p.m.
18.7 Physically Based Description of Quasi-Saturation Region of Vertical DMOS Power Transistors, C. Kreuzer, N. Krsichke* and P. Nance*, Universitat der Bundeswehr Munich, Munich, Germany and *Siemens AG **489**

Session 19: Device Interconnect Technology—Advanced Dielectric Technology

Tuesday, December 10, 2:15 p.m.
Continental Ballroom 6

Co-Chairs: Mark Bohr, Intel
 Dim-Lee Kwong, University of Texas

2:15 p.m. Introduction

- 2:20 p.m.
19.1 Ultrathin Nitrogen-profile Engineered Gate Dielectric Films, S. Hattangady, R. Kraft, D. Grider, G. Brown, M.A. Douglas, P. Tiner, J. Kuehne, P. Nicollan and M. Pas, Texas Instruments, Inc., Dallas, TX **495**
- 2:45 p.m.
19.2 High Performance 0.2 μ m CMOS with 2.5 nm Gate Oxide Grown on Nitrogen Implanted Si Substrates, C. Liu, E. Lloyd, Y. Ma, M. Du, R. Opila and S. Hillenius, Bell Laboratories, Lucent Technologies, Murray Hill, NJ **499**

- 3:10 p.m.
19.3 Metal-Ferroelectric-Semiconductor Field-Effect Transistor (MFSFET) for Single Transistor Memory Using Poly-Si source/Drain and BaMgF₂ Dielectric, J.S. Lyu, K.H. Kim*, J.Y. Cha*, B.W. Kim* and H.J. Yoo, Electronics and Telecommunications Research Institute, Taejeon, Korea and *Cheong-Ju University, Cheong-Ju, Korea **503**
- 3:35 p.m.
19.4 Trench Storage Node Technology for Gigabit DRAM Generations, K. Muller, B. Fluetner*, C. Hwang, R. Kleinhenz, T. Nakao**, R. Ranade*, Y. Tsunashima** and T. Mii, IBM, *Siemens and **Toshiba at IBM Advanced Semiconductor Technology Center, Hopewell Junction, NY **507**
- 4:00 p.m.
19.5 Impact of an In-Situ Nitrogen and Phosphorus Co-Doped Amorphous Silicon as the Scalable and Reliable Floating Gate of Flash Memory, T. Kaneoka, M. Anma, H. Itoh and M. Hirayama, Mitsubishi Electric, Hyogo, Japan **511**
- 4:25 p.m.
19.6 Ultra Fast Write Speed, Long Refresh Time, Low Power F-N Operated Volatile Memory Cell with Stacked Nanocrystalline Si Film, S.J. Shen, C.J. Lin, C.C.H. Hsu, National Tsing-Hua University, Taiwan, Rep. of China **515**

Session 20: Detectors, Sensors and Displays—MEMS I

Tuesday, December 10, 2:15 p.m.
Continental Ballrooms 7-9

Co-Chairs: Carlos Mastrangelo, University of Michigan
 Kozo Orihara, NEC Corporation

2:15 p.m. Introduction

- 2:20 p.m.
20.1 IC MEMS Microtransducers (Invited Paper), H. Baltes, O. Paul, J. Korvink, M. Schneider, J. Bühler, N. Schneeberger, D. Jaeggi, P. Malcovati, M. Homung, A. Häberli, M. von Arx, F. Mayer and J. Funk, ETH Zurich, Zurich, Switzerland **521**
- 2:45 p.m.
20.2 α (6H)-Si Pressure Sensors at 350 °C, R. Okojie, A. Ned, A. Kurtz and W.N. Carr*, Kulite Semiconductor Products, Leonia, NJ and *New Jersey Institute of Technology, Newark, NJ **525**
- 3:10 p.m.
20.3 A Low-Voltage Force-Balanced Barometric Pressure Sensor, B. Gogoi and C. Mastrangelo, University of Michigan, Ann Arbor, MI **529**
- 3:35 p.m.
20.4 Temperature Calibration of CMOS Magnetic Vector Probe for Contactless Angle Measurement system, M. Schneider, A. Häberli, M. Metz, P. Malcovati* and H. Baltes, ETH Zurich, Zurich, Switzerland and *University of Pavia, Pavia, Italy **533**
- 4:00 p.m.
20.5 Offset Reduction in Multicollector Magnetotransistors, M. Metz, M. Schneider, A. Häberli and H. Baltes, ETH Zurich, Zurich, Switzerland **537**

- 4:25 p.m.
20.6 Cylindrical Hall Device, H. Blanchard, L. Chiesi, R. Popovic and *R. Racz*, Swiss Federal Institute of Technology, Lausanne, Switzerland and *Sentron AG, Zug, Switzerland 541
- 4:50 p.m.
20.7 Smart Force Sensors for Scanning Force Microscope Using the Micromachined Piezoelectric PZT Cantilevers, C. Lee, T. Itoh, R. Maeda and T. Suga, AIST, MITI, Ibaraki, Japan 545
- 5:15 p.m.
An Ultrasensitive Uncooled Heat-Balancing Infrared Detector, C.C. Liu and C.H. Mastrangelo, University of Michigan, Ann Arbor 549

Session 21: CMOS Devices and Reliability—Advanced CMOS Transistor Architectures 553

Tuesday, December 10, 2:15 p.m.
Imperial Room

Co-Chairs: Jim Hayden, Motorola
 Mark Gardner, AMD

- 2:15 p.m.
Introduction
- 2:20 p.m.
CMOS Technology Scaling, 0.1 μ m and Beyond (Invited Paper), B. Davari, IBM Semiconductor Research & Development Center, Hopewell Junction, NY 555
- 2:45 p.m.
21.2 Search for the Optimal Channel Architecture for 0.18/0.12 μ m Bulk CMOS-Experimental Study, P. Bouillon, T. Skotnicki, C. Kelaidis, R. Gwoziecki, J.-L. Regolini, I. Sagnes, S. Bodnar, P. Dollfus*, CNET, Grenoble, France, *University d'Orsay, Paris, France 559
- 3:10 p.m.
21.3 A Sub-0.18 μ m Gate Length CMOS Technology for High Performance (1.5V) and Low Power (1.0V), M. Rodder, Q.Z. Hong, M. Nandakumar, S. Aur, J.C. Hu and I.C. Chen, Texas Instruments, Dallas, TX 563
- 3:35 p.m.
21.4 Degradation of MOSFETs Drive Current Due to Halo Ion Implantation, H. Hwang, D.-H. Lee, J. Hwang, LG Semicon Co., Ltd., Cheongju, Korea 567
- 4:00 p.m.
21.5 Anomalous Short-Channel Effects in 0.1 μ m MOSFETs, E. Crabbe, R. Logan, J. Snare, P. Agnello and J. Sun, IBM Semiconductor R&D Center, Hopewell Junction, NY 571
- 4:25 p.m.
21.6 High Speed 0.1 μ m Dual Gate CMOS with Low Energy Phosphorus/Boron Implantation and Cobalt Salicide, A. Hori, H. Umimoto, H. Nakaoka, M. Sekiguchi, M. Segawa, M. Arai, M. Takase and A. Kanda, Matsushita Electric Industrial Co., Osaka, Japan 575
- 4:50 p.m.
21.7 Low Resistive Ultra Shallow Junction for Sub 0.1 μ m MOSFETs formed by Sb Implantation, K. Shibahara, M. Mifuji, T. Kugimiya*, H. Furumoto, M. Tsuno, S. Yokoyama, M. Nagata, S. Miyazaki and M. Hirose, Hiroshima University, Higashi-Hiroshima, Japan and *Kobe Steel Corporation, Japan 579

- 5:15 p.m.
21.8 Low Voltage Operation of Sub-Quarter Micron W-Polycide Dual Gate CMOS with Non-Uniformly Doped Channel, H. Sayama, T. Kuroi, S. Shimizu, M. Shirahata, Y. Okumura, M. Inuishi and H. Miyoshi, Mitsubishi Electric Corporation, Hyogo, Japan 583

Session 22: Integrated Circuits—DRAM Technology 587

Tuesday, December 10, 2:15 p.m.
Grand Ballroom A

Co-Chairs: Tze-Chiang Chen, IBM
 Tohru Mogami, NEC

- 2:15 p.m.
Introduction
- 2:20 p.m.
A 0.23 μ m² Double Self-Aligned Contact Cell for Gigabit DRAMs with a Ge-Added Vertical Epitaxial Si Pad, H. Koga, N. Kasai, H. Hada, T. Tatsumi, H. Mori, S. Iwao, K. Saino, H. Yamaguchi, K. Nakajima, Y. Yamada, K. Tokunaga, S. Hirasawa, K. Yoshida, A. Nishizawa, T. Hashimoto, K. Ando, Y. Kato*, K. Takemura* and K. Koyama, NEC, Kanagawa, Japan and *Ibaraki, Japan 589
- 2:45 p.m.
22.2 Simultaneously Formed Storage Node Contact and Metal Contact Cell (SSMC) for 1Gb DRAM and Beyond, J.Y. Lee, K.N. Kim, Y.C. Shin, K.H. Lee, J.S. Kim, D.H. Kim, J.W. Park and J.G. Lee, Samsung Electronics Co., Kyungki-do, Korea 593
- 3:10 p.m.
22.3 A New Planar Stacked Technology (PST) for Scaled and Embedded DRAMs, S.P. Sim, W.S. Lee, Y.S. Ohu, H.C. Choe, J.H. Kim, H.D. Ban, I.C. Kim, Y.H. Chang, Y.J. Lee, H.K. Kang, U.I. Chung, C.S. Choi and C.G. Hwang, Samsung Electronics Co., Ltd., Suwon, Korea 597
- 3:35 p.m.
22.4 240nm Pitch 4GDRAM Array MOSFET Technologies with X-ray Lithography, K. Sunouchi, H. Kawaguchiya, S. Matsuda, H. Nomura, T. Shino, K. Murooka, S. Sugihara, S. Mitsui, K. Kondo, Y. Kikuchi, K. Deguchi*, M. Fukuda*, M. Oda*, S. Uchiyama*, M. Suzuki*, T. Watanabe* and K. Yamada*, Toshiba Corp, Kawasaki, Japan and *NTT LSI Labs, Atsugi-shi, Japan 601
- 4:00 p.m.
22.5 Advanced Integration Technology for a Highly Scalable SOI DRAM with SOC (Silicon-On-Capacitors), I.K. Kim, W.T. Kang, J.H. Lee, S.I. Yu, S.C. Lee, K. Yeom, Y.G. Kim, D.H. Lee, G. Cha, B.H. Lee, S.-I. Lee, K.C. Park, T.E. Shim, C.G. Hwang, Samsung Electronics Co. Ltd., Kyungki-Do, Korea 605
- 4:25 p.m.
22.6 16Mb DRAM/SOI Technologies for Sub-1V Operation, T. Oashi, T. Eimori, F. Morishita, T. Iwamatsu, Y. Yamaguchi, F. Okuda*, K. Shimomura, H. Shimano, N. Sakashita, K. Arimoto, Y. Inoue, S. Komori, M. Inuishi, T. Nishimura and H. Miyoshi, Mitsubishi Elec Corp., Hyogo, Japan and *LTEC Corp. 609
- 4:50 p.m.
22.7 Discussion Session