Electron-Beam, X-Ray, and Ion-Beam Techniques for Submicrometer Lithographies IV

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Electron-Beam, X-Ray, and Ion-Beam Techniques for Submicrometer Lithographies IV

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ELECTRON-BEAM, X-RAY, AND ION-BEAM TECHNIQUES FOR SUBMICROMETER LITHOGRAPHIES IV

Volume 537

INTRODUCTION

Optical lithography has enjoyed a preeminent position in the semiconductor industry because of its outstanding technical merit and cost advantages. Both of these factors are being strained, however, as linewidth approaches 0.7 μm—the first with linewidth control due to depth of field, and the second with higher capital cost and the need to use multilayer resists. Meanwhile, E-beam, x-ray, and ion-beam lithographies have sharpened their tools to improve throughput and reduce capital cost. No competent lithographer expects these technologies to appreciably displace optical lithography in the forseeable future, but most believe that a trend toward increased usage is in progress. It is reasonable to expect that the trend will continue until we find it natural to install these technologies in new, probably hybrid, production lines.

Predicting when optical lithography will run out of steam has become a favorite avocation of many workers in advanced lithography. Most scenarios begin with a plot of linewidth versus year of implementation. These plots, first used by Gordon Moore, use the functional relationship that $LW = A(Yr^{-m})$. Remarkably, these simple curves have passed the test of time for over 10 years and we have no reason to believe they will suddenly fail. Generally, these plots indicate that advanced chips with 1.0 μm linewidths will be in volume production by about 1990, and that linewidths of 0.5 μm are now in advanced pilot lines (VHSIC) and will be in production by 1995. The second step in predicting the course of lithography begins by selecting an area where optical lithography is technically vulnerable, and then determining at what linewidth the deficiency becomes paralyzing. Linewidth control appears to be the area of most vulnerability. It is then a simple matter to determine when this will occur by referring to the curve of linewidth versus time.

Three papers were presented during this conference which project the critical linewidth when E-beam, x-ray, or ion-beam lithographies may begin to replace optical lithography in production. There seems to be a consensus that x-ray lithography is the candidate most likely to inherit the throne presently held by optical lithography. The first paper, by R. Ruddell (537-25), presents a case for a crossover at 1.25 μm based on a depth of focus limitation as numerical aperture is increased. A. Wilson (537-11) projects a crossover at 0.5 μm after lenses with a numerical aperture of 0.4 at 250 nm have run their course. The third paper, by M. Nakase (537-20), concludes that optical lithography has superior image contrast to E-beam lithography at 0.5 μm when using a numerical aperture of 0.6 and a wavelength of 193 nm. Obviously, a consensus is not available at this time, and we must be content with an estimate that optical lithography will run out of steam between 1.25 and 0.5 μm. The period of implementing x-ray lithography into production therfore lies between 1987 and 1995. It is important to recognize that we are now entering the pilot line era.

E-beam lithography is a relatively mature tool and already dominates the pattern generation, prototype chip fabrication, and custom-connected gate array areas of lithography. Penetration into direct wafer writing in pilot lines is very evident by the many reports regarding the sudden increase in machines sold to GaAs fabrication facilities. S. Kimoto (537-17) described a new low-cost commercially available laboratory-type machine with 0.1 μm direct write capability. Throughput using E-beam lithography is low for economical direct wafer writing on a large scale, but advanced machines were described by Petric (537-04) and Carroll (537-05). These faster machines feature throughputs of between 10 to 30 wafer levels per hour at 0.5 μm when using resists with sensitivities of 3-5 $\mu C/cm^2$. Economic parity with optical lithography has not yet been achieved but the gap is closing! Mask inspection and repair with submicron capability is becoming a new area of application for E-beam and/or ion-beam techniques. Livesay (537-03) announced that Electron Vision plans to commence development of a submicron defect inspection system.

Present x-ray lithography systems using electron impact sources are limited to throughputs of 3 to 10 wafers per hour when resists with good submicron resolution are used. Barring any breakthrough in resist technology, throughput will remain a barrier to production usage until pulsed plasma or synchrotron sources become practical. A. Wilson (537-11) presented data supporting economic feasibility for using a synchrotron. His conclusion is that x-ray lithography is economically viable below 0.5 μm if sufficient capital is available for installation of a synchrotron. The problem of alignment in x-ray lithography was shown to be manageable by Fay (537-08), who used electrical test devices to show that full wafer alignment can be achieved to <0.25 μm (3σ).

Ion-beam lithography is showing early advantages in repairing defects on optical masks. Ward (537-13) showed that both opaque and pinhole defects can be repaired, the latter by ion-milling a crevice that scatters light away from the area below the pinhole. T. Kato et al. (537-29) reported on an experimental FIB system with a beam diameter of only 70 nm. Alignment using multichannelplate detectors was reported to have better S/N ratios than when using scintillators-photomultipliers. The adverse effects of multiple scans over alignment marks was shown and correlated with rounding of the marks by the ion beam.

Optical lithography was also represented in the special session on Submicron Lithography in Japan. The presentations on E-beam, x-ray, and ion-beams have been incorporated in the previous sections for clarity. Yanazawa et al. (537-19) reported adequate resist profiles of 0.6 μm lines using an i-line lens with NA = 0.4. Multilayer resist techniques, however, are seen as becoming necessary in the future to control linewidth. Todokoro et al. (537-22) described improvements to the normal trilevel resist system for optical and E-beam lithography. Planarization of steps was significantly improved by exposing the resist prior to the high-temperature bake, and spin-on indium tin oxide (ITO) films were described to control electron charging.

Evidence that optical, E-beam, x-ray, and ion-beam lithographies are each finding their own areas of advantage is clearly visible, and a synergistic hybrid approach to submicron lithography seems most likely in the future.

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Volume 537

Contents

ELECTRON-BEAM, X-RAY, AND ION-BEAM TECHNIQUES FOR SUBMICROMETER LITHOGRAPHIES IV

Volume 537

Session 1

Electron-Beam Lithography

Chairman
John C. Wiesner
Perkin-Elmer Corporation

E-BEAM TOOL REQUIREMENTS FOR NANOLITHOGRAPHY

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Introduction

Since the beginning of the use of Electron Beam Lithography there has been a continuous pressure for very fine lithography. This was initially developed for high frequency FET's and these applications remain a powerful user of nanolithography. [1] In addition since those early days, there has emerged the requirements for integrated optics. Recently the use of electron beams to write distributed feedback laser systems has provided greater flexibility in the selection of their operating wavelength. [2] The use of electron beams to write fine holographic patterns of arbitrary complexity has been a growing application. What all these devices have in common, is a high range of complexity coupled with very fine demanding lithography. In addition, there is a strong requirement for ultra fine lithography for physics experiments. These include the use of Josephson Junctions and associated systems for flux entrapment and fundamental physics experiments, as well as the ability to use complex arrays of regular patterns for electro magnetic experiments. [3], [4] In this case the requirements are characterised by a need for very simple fine structures, together with coarser connection to the outside world.

System requirements

From this brief overview of the applications it is clear that the capabilities of the ideal system should cover a wide range. In particular at its heart, the system must be capable of producing good quality nanolithography. By this we mean the capability to produce lines in the region of 100 - 20 nm and to produce these lines without any additional edge perturbation caused by such machine defects as magnetic field or power supply instabilities. The system must further be capable of handling intermediate lithography which we define to be in the region of 100 - 500 nm. This region is important both economically for the large complex systems described before, and also to provide the interconnection to the outside world. The equipment must be capable of producing extended structures, that is to say structures which although they contain nanolithography, may extend to several millimetres and on occasion several centimetres. This is particularly true with integrated optic systems and surface acoustic devices as shown in Figure 1. The equipment must be designed for use by people whose main interest is producing the devices, whether to enable some complex communication system or to further a physics experiment. They are not interested in the technology of the equipment itself having sufficient problems to master their own techniques. Therefore, a primary requirement is that such a system shall be useable by people whose main expertise lies other than in the operation of the machine.

Finally, but often a significant problem, the system must be within the financial scope of the institution operating it. This often means not only that the system should represent good value for money, but also that it should be capable of taking on tasks which might otherwise be done elsewhere within the users environment. For example the system may be used as a back-up capability to provide otherwise conventional mask plates.

System implementation

We have already reviewed the application capabilities required of an E-beam tool, we should now briefly investigate how such a tool can be provided to the practitioner. The first thing that clearly emerges is that the system should be based as far as possible upon existing technology. We have seen how the requirements blend into existing integrated circuit fabrication scene and from this to the specific tool. The existing techniques provide finely focused probes, with energies in the range of 1 - 50 kV. These capabilities can be readily made to provide the nanolithography whilst at the same time the precision stage handling and the precision alignment techniques that have been painstakingly developed over the past decade, may also be applied to the nanolithography tool.

Equally important is the control and calibration software. Crucial to the operation of any modern machine, is the software that will control the exposure. This software must be robust and bug free. Despite the advances in software theory, the only practical way of doing this is to ensure that the software has been created in an evolutionary manner. [5]

Closely linked to the software requirements are the requirements that the system should be compatible with existing CAD systems. Although some of the physics experiments may be defined in a few lines of code, most of the more complex structures will require the use of a CAD system to define and to refine them. In summary, the provision of the E-beam nanolithography tool should use where possible existing techniques, for both the design of the tool and the application of the tool provide enough problems in themselves to keep both the supplier and the user busy without the need to introduce any extra problems.

Let us now review how the machine requirements can be met in any design. The primary requirement for the nanolithography tool is to provide a fine beam of electrons. High resolution resists are relatively insensitive and will require dosages of the order of 1 nC/cm for fine line structure. This means that the writing time for even a modest sized device may readily extend into several hours writing. [16] Because of this it is clear that a high brightness source is required. However, the available high brightness sources have several significant drawbacks. In particular the use of field emission which would otherwise be the natural choice, proves to be technically very difficult because the field emission, characterised as it is by the emission from a few atomic sites, is subject to sudden and relatively violent changes in current. It is fairly normal experience that field emission systems may produce changes of current of the order of 5 -10% which will take place over sub-microsecond periods as shown in Figure 2 [7]. When a fine structure is being written such a sudden change in dosage will manifest itself as an unacceptable change in the linewidth. It is thus important that one utilises a bright but stable source. Of the available sources the directly heated LaB6 has shown itself over many years to be a superior technique, and now with the greater availability of single crystal devices, it becomes suitable for the incorporation in a production tool.

A further requirement of the E-beam tool is that it should be capable of handling irregular substrates as well as complete wafers and, as has already been discussed, also be capable of handling mask plates. The reason for the need to handle wafers is clear when large complex devices are considered, but even for physics experiments it is very useful to be able to handle wafers and thus make use of the wide range of process equipment which has been designed for the semiconductor industry. One has only to consider the need to apply uniform coatings of resist to immediately see how much easier it is to handle a 4" uniform wafer than, for example, some fractured sample of a single crystal.

Because the devices that are to be fabricated will often extend over many centimetres, there is a very significant requirement that the equipment be capable of abutting many fields to produce one large uniform feature. These may be required for leadouts but they may be fundamental to the operation of the device itself. It is of great importance that the junction of the fields should provide as smooth as possible a continuation of the pattern. [8] Closely related to this is the requirement to be able to apply one layer of lithography, accurately overlaid on to some feature. One would seek to attain an overlay accuracy of the order of 30 nm or less, and this will clearly require the ability to use the beam to register previously written marks.

It is also a requirement of these systems that fine changes in scale may be executed. In the case of surface acoustic waves and DFB's, it is required to make fine adjustments to the emitted frequencies, or it may be required for scaling and process sensitivity experiments in the case of rather more conventional applications. Therefore the system must provide a very fine control over the basic scaling of the lithography. Figure 3.

Finally, we need to review the choice of excitation voltage. It has readily been shown elsewhere that the use of very low energy electrons can provide low back scattering effects. [9] However, the application of very low voltage electrons is subject to stray field effects, high chromatic spread and a lack of penetration through the resist. For this reason most nanolithography has been conducted at 20kV and greater. One must therefore look to the reasons why one should select to operate at 30, 40 or 50kV. As the excitation energy is increased so the electrons penetrate further into the body of the material and, if it is bulk material, will then scatter back over a greater range. [10] Even when 20kV energy electrons are used the scattering range is considerably in excess of the nanolithography and therefore for these applications the bulk of the so-called proximity effect is inevitably spread over many shapes and it is highly likely that the background dose equalisation technique is a better mechanism for overcoming the inter and intra proximity effects. [11] On the other hand the higher kV provide better uniformity as the beam crosses underlying shapes or changes of material, for this reason one requires the ability to use excitation levels above the normal 20kV. However the use of excitation levels above 50kV will, in most cases, result in significant electron beam damage without a compensating improvement in the nanolithography. For this reason the Cambridge EBMF UHR system (see Figures 4 and 5) has restricted the excitation voltage to 50kV.

Conclusion

We have reviewed the requirements for a nanolithography tool, we have seen how, despite the wide range of requirements they may be integrated into a single system. Indeed we have seen how, for many of the applications an integrated system is essential if the user is not to be burdened with impossible complexities of operation. In order to provide this integrated system, we have seen how most of the capabilities of a conventional lithography equipment are required. In particular the requirements for a laser controlled stage to provide capability for large field operation, and to provide lithography that may extend over several centimetres whilst within the same machine retaining the capability of nanolithography. In the same way the requirements of the system to be able to handle a wide range of excitation voltages has been discussed. At the lower end the low excitation electrons will provide little back scattering, but are vulnerable to the effects of fields generated within the equipment and also suffer from poor penetration of resists whilst at the higher excitation level the superior performance in terms of penetrating the resist must be balanced against the wider range back scattering and the increased incidence of damage to the material. Different experimental requirements are benefited by different excitation voltages and so it is imperative that any system provided as a nonolithography tool must be flexible. These requirements for the nanolithography tool have been discussed in terms of the Cambridge EBMF UHR system, this is part of the continuous evolution of the Cambridge EBMF series and has been tailored to the nanolithography applications. It sacrifices some of the high speed large field intermediate lithography capability and provides instead a system with the latest features for nanolithography, whilst retaining basic facilities for intermediate and coarse lithography.

Acknowledgements

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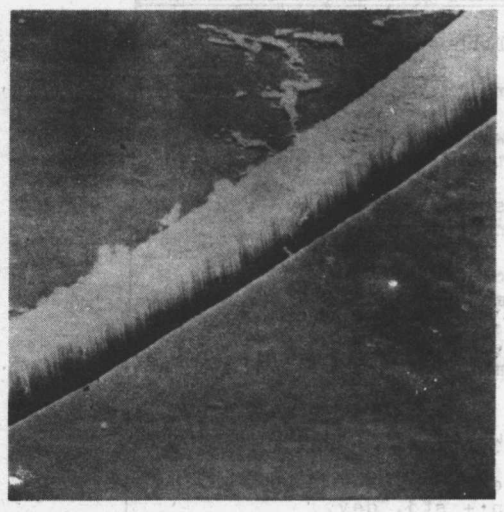

Figure 1 Integrated Optical Waveguide Lithography

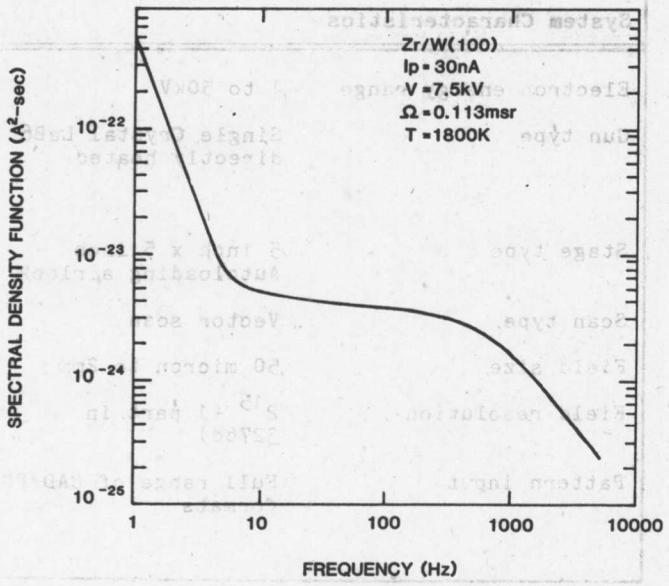

Figure 2 Spectral Density Function for a Zr/W(100) TFE emitter vs frequency

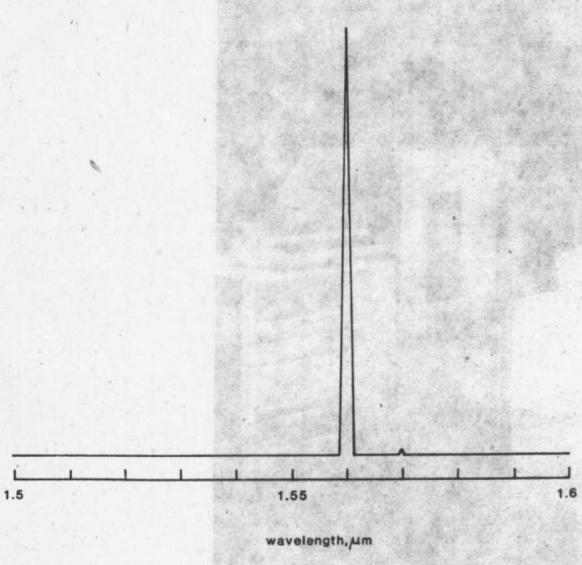

Figure 3 Spectral output characteristic of E-Beam fabricated DFB laser

System Characteristics		Operational Characteristics	
Electron energy range	1 to 50kV	Nanolithography:	
Gun type	Single Crystal LaB6 directly heated	Minimum spot size	8nm
		Linewidth control (50 micron field)	10%
Stage type	5 inch x 5 inch Autoloading airlock	Registration overlay (standard deviation)	0.03um
Scan type	Vector scan	Microlithography: (1.6mm field)	
Field size	50 micron to 2mm		
Field resolution	2^{15} (1 part in 32768)	Minimum linewidth	0.25um
Pattern input	Full range of CAD/PG formats	Linewidth control	<20%
		Stitching error (mean + std. dev.)	<0.3um

Figure 4 Table of main specification details of EBMF 2.5 UHR Nanolithography System

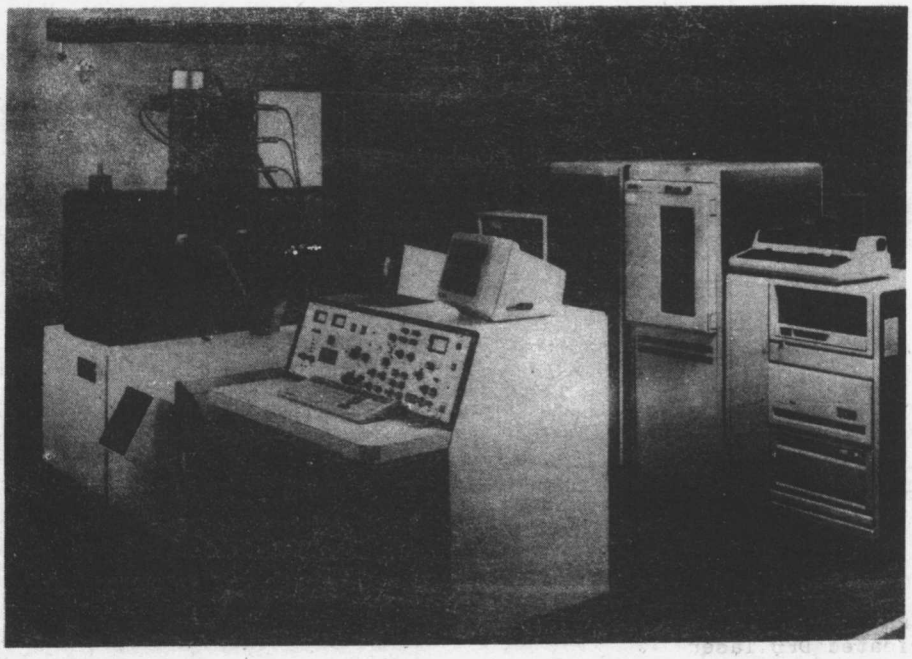

Figure 5 Photograph of the EBMF 2.5 UHR Nanolithography System

Development of a Nanometric E-Beam Lithography System (JBX-5DII)

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Abstract

The production of VHSIC and microwave devices has shown that submicron lithography by E-beam, Optical, or X-ray systems is rapidly becoming feasible. There is, however, a developing demand for a nanolithography tool for producing Josephson, GaAs, optoelectronic devices and for investigating the physics of scaling of semiconductor devices.

We have developed an electron beam lithography system, the JBX-5DII, which is applicable for effective fabrications or both submicron and nanometer devices. The system employs the high brightness single crystal (100 LaB_6 cathode and in-lens type octopole deflector. The functions enable automatic switchings of the accelerating voltages between 50kV and 25kV, of the writing modes between large and small probe currents, and of the different scanning field increments.

The presented paper deals with some characteristics occurring after the switching of writing modes. Experimental results will be reported about the characteristics and stabilities for accelerating voltage, currents of alignment coil and lens excitations, and probe currents, investigating problems associated with the mode switchings. The mark detection technology for nanometer writing will be presented together with experimental results, including measuring results of 80A probe size. We will also demonstrate some exposure results obtained with the JBX-5DII.

Introduction

The drive of VHSIC to push lithography requirements to sub-half micron for GaAs and sub-micron for silicon may or may not be met by optical lithography systems. Even in corporations where optical is chosen over E-beam for pilot production facilities, an advanced E-beam direct write system is a requirement for next generation devices and quick turn around of engineering modifications of present VHSIC chips.

Two of the major requirements for this type of direct write E-beam systems are 1) optimization of optics, beam conditions and writing strategy for nanometric writing and 2) tradeoffs between nanometric writing and throughput requirements to permit rapid turn around of designs into sufficient quantities of chips to permit proper evaluation of new prototypes.

For nanometric writing higher accelerating voltage is required to reduce proximity affects which results in a reduction in scanning field size and resist sensitivity. In addition, the probe size is selected to permit single pass writing. Often, however, a sub-half micron or nanometric lithography device will contain large areas of micron and above patterns covering large areas. If only a nanometric beam is used throughput will be greatly reduced by the use of a small probe size with low beam current.

In response to these requirements, JEOL has engineered an electron beam lithography system optimized to reduce these tradeoffs, the system comes in two models the JBX-5DII(U) and the JBX-5DII(F).

System Concept

Each system allows combinations of 8 different writing modes, including changing the accelerating voltage between 25kV and 50kV. Table 1 summarizes the writing modes the system specifies. These writing modes are stored and automatically set and calibrated from the CPU. The system automatically switches current level when writing patterns of different sizes; from high to low when writing fine patterns, and vise versa. The system employs vector scan with Gaussian beam distribution for writing. An H-P laser interferometer with /120 (0.005um) resolution is used to determine the position of the stage. Beam scanning step ranges from 0.0025 to 0.1um for nanometer writing (JBX-5DII(U)) and from 0.025 to 1.0um in sub-half micron writing (JBX-5DII(F)). Both models are used for direct write. The F type system is designed to include mask or reticle writing capabilities, and is configured for the addition of an automatic loading system to hold twelve work pieces.

Table 1 JBX-5D II WRITING MODES TABLE

TYPE	H.V	MAXIMUM FIELD SIZE	BEAM CURRENT	OBJECTIVE LENS	
F/U	50KV	750μm × 750μm (LARGE FIELD)	HIGH	4th LENS & 2nd DEFLECTOR	FOR SUB-MICRON WRITING
			LOW		
	25KV	1500μm × 1500μm	HIGH		
			LOW		
U	50KV	80μm × 80μm (SMALL FIELD)	HIGH	5th LENS & 1st DEFLECTOR	FOR NANOMETER WRITING
			LOW		
	25KV	100μm × 100μm	HIGH		
			LOW		

System Construction

Figure 1 shows a block diagram of the JBX-5DII. Writing data stored on disk (205 MB) is transferred from the disk to the scanner unit by the DMA. The scanner unit is equipped with data buffer memory to eliminate idling time due to data transfer. Aside from data conversation, two I/O bus lines are provided. One is for manual control of the system (CSL bus line), and allows the operator to set conditions for the electron optics system (EOS) and select the 8 writing modes from the operation console, while the other line is for the CPU to send I/O commands (EBX I/O bus line), and pattern writing data to the EOS.

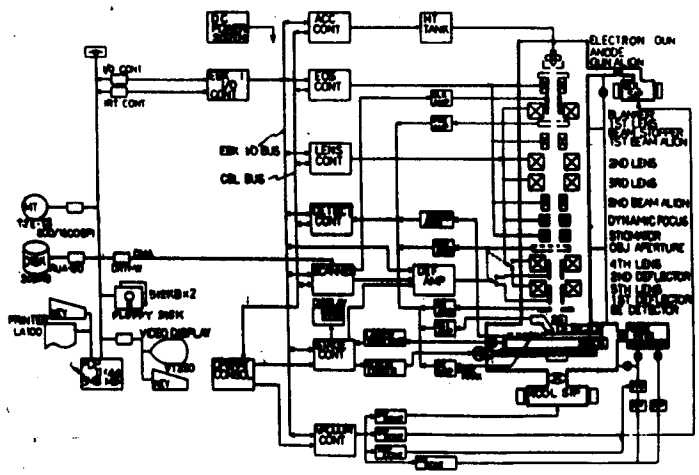


Fig 1 JBX-5D II(U) SYSTEM BLOCK DIAGRAM

Figure 2 shows the construction of the EOS. The EOS is a 4 step demagnifying image forming system which provides probes 8nm to 1um in diameter for the JBX-5DII(U) and 35nm to 1um for the JBX-5DII(F) the LaB_6 source is used. Source is used with circiutery designed to permit of accelerating voltage. The lens system is divided into 3 steps. The first step demagnification lens forms an image of the gun cross-over at the beam blanking position. The second and third step demagnification (2nd and 3rd lenses) controls excitation of the two lenses so that the position of an image formed by the third lens

remains stable. This allows excitation current of the objective lenses (4th and 5th lenses) to remain unchanged, even when beam current is changed by the demagnification lenses, as a result of the objective lenses having in-lens deflection for beam scanning. The system has two types of objective lens; one for sub-micron writing (4th lens) and the other for nanometer writing (5th lens). Each objective lens is equipped with an electrostatic octupole deflector for beam scanning. For nanometer writing, the 5th lens with short working distance and the first deflector are selected; and for sub-half micron writing, the 4th lens with long working distance and the 2nd deflector, thus allowing writing with a large scanning field. The backscattered electron detector uses a P.N junction element to detect chip marks on the wafer even with low current. The system uses the detected signals from the chip marks for chip registration, and automatic focus.

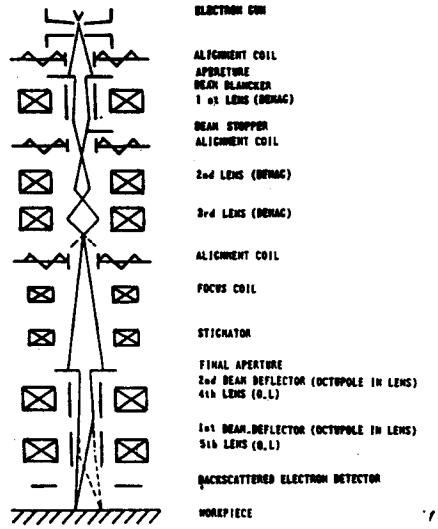


Fig 2 JBX-5D II EOS COLUMN CONSTRUCTION

Writing Modes Selection

As mentioned before, the major advantage of the system is automatic change over of writing modes. The system provides 8 different modes, resulting from combinations of accelerating voltage (25kV/50kV), scanning field size (large/small), and beam current (high/low). The field size is changed by selecting the 4th lens or 5th lens in the EOS; and beam current by changing excitation current of the demagnifying lenses (2nd and 3rd lenses). Each component of the EOS has a register and D/A convertor, so that the CPU can control the changes in the EOS. EOS control parameters for each writing mode is manually set, and the CPU stores the parameters in a 8 EOS parameter file on disk. The CPU will read out the control parameters from the disk file, responding to commands from the writing schedule data, and execute changes of the EOS conditions.

Flow of Nanometer Writing

The system starts pattern writing in the low current mode, then switches to high current and low kV for the coarser geometries Figure 3. In either mode, the system measures beam current before writing, and determines scanning speed based in relation to resist sensitivity and beam scanning step. It then corrects the amplitude of mark detection signals according to beam current. Next, the system measures wafer rotation and expansion and corrects the direction and distance of sample movement as well as beam scanning direction. The system one mark from the three at the first chip position, and adjusts beam focusing. The width and position of beam scanning is corrected by detecting a total of three marks. The same chip marks are used for the coarser geometries after switching to low kV and high beam current. When writing a great number of chips, the system measures beam current and corrects drift. (ie., correction of beam scanning speed and mark detection amplitude) after writing a specified number of chips or as a function of time.

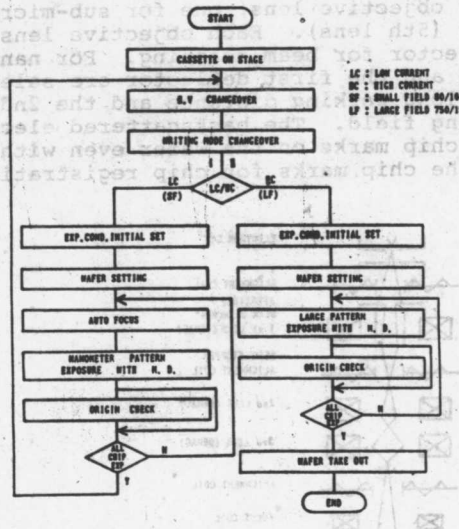


Fig 3 JBX-5D II (U) FLOW CHART OF NANOMETER LITHOGRAPHY

Nanometer writing requires a high-performance backscattered electron detector, as the beam current is quite low. The backscattered electron detector in the JBX detects signals under the following minimum conditions: resist thickness 100nm, gold mark thickness 100nm, accelerating voltage 50kV, probe current min. 30pA, and probe diameter approximately 15nm. The nanometer writing described here are executed under the same conditions.

Evaluation of Nanometer Probe

Located on the stage of the JBX-5DII system is knife edge and faraday cup to measure beam diameter. Figure 4 shows the construction of the knife edge detector. It is essential to have very thin edges for measuring a nanometer size beam, thus a gold coated micro plastic grid is employed. Beam current being very low, the beam current detector is collected by a P/N junction element, and an aperture is placed to screen scattered electrons from the edges. Figure 5 is the results of measurement with the knife edge detector.

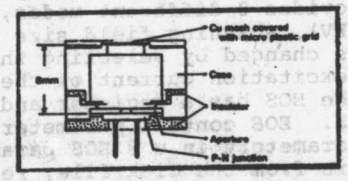
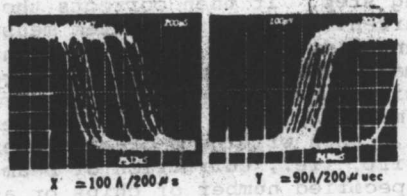


Fig 4 Construction of knife edge detector



X = 100 A/200μs Y = 90A/200μsec

Fig 5 Waveform of nanometer electron beam
Accelerating voltage : 25kV
Beam current : 5pA

Summary

The JBX-5DII Series E-beam Lithography systems have been developed to optimize fine feature writing through high 50kV operation and beam size as small as 8nm without sacrificing high throughput by having the electron optics system switch to 25kV and larger probe size for coarser geometries. The system is fully controlled from the CPU including switching over from fine writing mode to high throughput mode. The system includes autofocus and complete CPU control to permit unattended operation in pilot production operation of devices with features less than 0.1um.

Performance Testing of the Waferwriter™ Electron Beam Direct Write System

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Abstract

Performance tests on the Waferwriter™ system, a high brightness electron beam direct write system, are described. The Waferwriter system is an ultra-high current density, variable size round beam direct write system, capable of exposing existing popular photoresists at higher rates than conventional shaped beam systems in the micron and submicron feature size range. Performance tests are described covering overlay accuracy, alignment, resolution, and throughput. The system is the first to meet the DoD's VHSIC requirements for E-beam direct write systems.

Introduction

Two years ago at this conference we described the Waferwriter™ system[1]. This system is unique in its architecture as compared to other direct write systems being developed in that it utilizes a variable round (gaussian) beam instead of a shaped beam. Its small spot size provides better exposure control than shaped beam systems and, coupled with its very high brightness source, can achieve higher throughput rates at small geometries.

The prototype system was recently delivered to the Naval Ocean Systems Center Microelectronics Laboratory in San Diego, California. Prior to delivery, and for the past twenty-four months, the system underwent performance tests and debugging in round-the-clock operation. In August of last year the system successfully passed in-plant acceptance tests which met the DoD's VHSIC program required goals for overlay, resolution, and throughput.

System Description

The Waferwriter system is a vector-addressed, write-on-the-fly (moving table) direct write system. The system utilizes a thermal field emission source and is capable of providing up to 3,000 amps/cm^2 current density at the writing substrate surface. The electron optical column utilizes only two magnetic lenses, providing high reliability and reduced column maintenance. The pattern control system is comprised of distributed microprocessor controlled subsystems. The pattern computer, which converts digitized patterns into geometry data for the deflection system, can output up to ten million geometries per second, with each pixel individually addressed.

The first Waferwriter system prototype (Waferwriter I) reached system integration in the fall of 1982. Writing tests began in January '83. Table 1 shows the operational history of the development prototype system (designated Waferwriter I) from that period of time through August 1984. We spent much of this time testing, debugging, redesigning, and modifying various subsystems. We sought to maintain the daily schedule (depicted in Table 2) in which maintenance, checkout, hardware testing, software development, and actual writing could be done in a coordinated manner. During this period of time, we maintained records of system availability (for writing). In this development period there was extensive downtime due to modifications and rework of various elements in the system. For periods where major system changes were not occurring, we'd strive to have the system ready to write by the evening shift. Availability of the system for writing over this period of time is indicated in Table 1. (Note: System availability as used here may not have meant the system was utilized in a full writing mode due to the fact that in many cases we were interested in testing one particular aspect of system performance.) Our primary interest was determining the major causes of system downtime on the development prototype so that we could rectify these on the production model.

Figure 1 depicts the causes of system downtime during this period (less downtime caused by system modifications which accounted for 54% of the total). Debug error (someone attempting to fix a problem and fixing the wrong thing was the next most prominent cause of downtime. However, although debug errors are prevalent in a development prototype, they are largely irradicated once a system gets into production and the self-diagnostics are fully in place.

Therefore, the remaining causes for downtime are likely to be the major ones in a production environment. Therefore, we emphasized improving upon these in the design of the production prototype (Waferwriter II). The sequencing system which incorporates mechanical