# Modern MOS Technology:

## *Processes, Devices, and Design*

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**McGraw-Hill Book Company**

*New York St. Louis San Francisco*
*Auckland Bogotá Hamburg*
*Johannesburg London Madrid Mexico*
*Montreal New Delhi Panama Paris*
*São Paulo Singapore Sydney Tokyo*
*Toronto*

Library of Congress Cataloging in Publication Data

Ong, DeWitt G.
Modern MOS technology.

Includes index.
1. Metal oxide semiconductors. 2. Integrated circuits. I. Title. II. Title: Modern M.O.S. technology.
TK7871.99.M44053 1984 621.381'73042 83-11338
ISBN 0-07-047709-4



1234567890 KGP/KGP 89876543

ISBN 0-07-047709-4

The editors for this book were Harry Helms and Joan Cipriano, the designer was Elliot Epstein, and the production supervisor was Thomas G. Kowalczyk. It was set in Baskerville by University Graphics, Inc.

Printed and bound by The Kingsport Press.

# *Preface*

Metal-oxide-semiconductor (MOS) integrated circuit (IC) technology encompasses a wide spectrum of sciences and disciplines, ranging from semiconductor physics to chemistry to circuit design. The goal of this book is to distill the more important concepts and techniques of the various disciplines and present them in a coherent framework. As stated by the subtitle, this body of information is partitioned into device physics (Chaps. 1 to 6), wafer processing (Chaps. 7 and 8), and circuit design (Chaps. 9 to 14).

Chapter 1 gives an overview of the MOS technology and its importance in the IC industry. Chapter 2 reviews semiconductor physics with an emphasis on the *pn* junction for its similarity in using the concept of band bending. Threshold voltage is introduced in Chap. 3 as part of the discussion on the surface properties of silicon. A separate chapter (Chap. 4) is devoted to *CV* (capacitance-voltage) plots, not only because of their importance as an analysis tool in MOS work but also because they are a vehicle for discussing nonideal effects. Included in the chapter are practical tips in doing *CV* plots and a computer program (written in BASIC) for analyzing the plots. Chapter 5 covers physics and characteristics of MOS transistors, and Chap. 6 probes the subject further with regard to small geometry effects.

Chapter 7 describes the various MOS processes that are in volume production now or will be in the foreseeable future. Chapter 8 describes the individual processing steps in wafer fabrication. Attention is focused on the newer processing techniques such as ion implantation, dry etching, and noncontact exposure.

The section on circuit design starts off in Chap. 9 with digital IC design, the mainstay of the MOS business. Chapter 10 covers analog MOS design, an area of growing importance and interest. Switched capacitors and charge-coupled devices (CCDs) are the two main methods of implementation.

CMOS is discussed separately in Chap. 11 because it is increasingly specified as the technology to use, particularly for larger scale integration. Chapter 12 uses the commercially available ASPEC circuit simulation program to provide one specific example of computer design aids. Chapter 13 explains the rest of the design and manufacturing cycle, namely layout, mask generation, and assembly. Finally, the book closes in Chap. 14 with yield and reliability, two key subjects inseparable from any study of integrated circuits.

For the convenience of the reader, each chapter is designed to be self-contained, with minimum referencing back and forth to other sections of the book. However, the order of the chapters is found from experience to be pedagogically effective for easy understanding and long-term retention. The book strives for logical progression from the familiar to the unfamiliar, from the understanding of a device, to its fabrication, then to its use.

Each chapter is written at a level appropriate for the intended reader. For example, the review of semiconductor physics is presented in very basic terminology for those with no background in that area, whereas the section on digital circuit design assumes familiarity with logic manipulations.

This book uses charts, graphs, and tables to convey specific technical information useful to practicing professionals in the field. At the same time, it is suitable as a textbook for a one-semester course. It is appropriate at either the senior or first-year graduate level, depending on the depth of coverage desired. As an aid in teaching, there are problem sets at the ends of the chapters. However, they are really an integral part of the book. They amplify the materials in the text, illustrate numerical values, reinforce the explanations, and introduce additional concepts.

I am indebted to Professor Lex Akers of Arizona State University for writing Chap. 6, "Small-Geometry Effects," a subject of timely importance.

I am also indebted to many reviewers for their enlightening comments and discussions on various materials in the book. They include Dr. J. R. Brews and Dr. J. A. Cooper, Jr., of Bell Laboratories; Dr. E. T. Gaw, Dr. W. W. Fisher, Dr. S. T. Nieh, Dr. M. H. Woods, Mr. F. J. Burris, and Dr. J. Mar of Intel Corporation; Professors P. R. Gray and R. W. Brodersen of University of California in Berkeley; and Mr. S. L. Smith, Mr. M. Smith, Mr. R. Allgood, and Dr. J. B. Price of Motorola Incorporated. I am very appreciative of the work of Mrs. Kathy Gear in typing the whole manuscript on the word processor and of Mr. Eric Maass in generating a solution set for the problems.

Last, I would like to thank my wife, Josephine, and my children. Their encouragement and patience during the many evenings and weekends that went into the writing of this book make them the unseen coworkers of this writing project.

*DeWitt G. Ong*

# Contents

# 1

# *Overview of MOS*

## 1-1 INTRODUCTION

Metal-oxide semiconductor (MOS) integrated circuits (ICs) have become the dominant technology in the semiconductor industry, overtaking the bipolar integrated circuits in sales volume in recent years (see Fig. 1-1).[1] With MOS, it is now possible to have more than 100,000 transistors on a single chip, allowing the fabrication of a complete 32-bit microprocessor[2] with a three-chip set (see Fig. 1-2) or a quarter of a million bits of memory on a chip.[3] The main reason behind MOS IC's pervasiveness is that MOS ICs exceed the bipolar transistors in functional density, that is, the number of functions performed on a single chip, and at a competitive price as well. That, in turn, is due to the fact that MOS transistors are smaller in size and somewhat simpler to fabricate.

At this point, it should be noted that by and large, MOS products are sold almost exclusively in integrated-circuit form. Very few single transistors are marketed, and those are primarily specialized power transistors and RF mixer transistors. By contrast, in the bipolar semiconductor market, there is a sizable demand for discrete transistors and diodes.

## 1-2 WHAT IS A MOS TRANSISTOR?

As the name metal-oxide semiconductor implies, the MOS transistor consists of semiconductor material (silicon) on which is grown a thin layer (250 to 1000 Å) of insulating oxide, topped by a gate electrode. Such a structure is shown in Fig. 1-3. The gate electrode was originally metal, specifically aluminum, but is now more commonly a layer of polycrystalline silicon (referred to as *polysilicon*). Source and drain junctions are formed with a

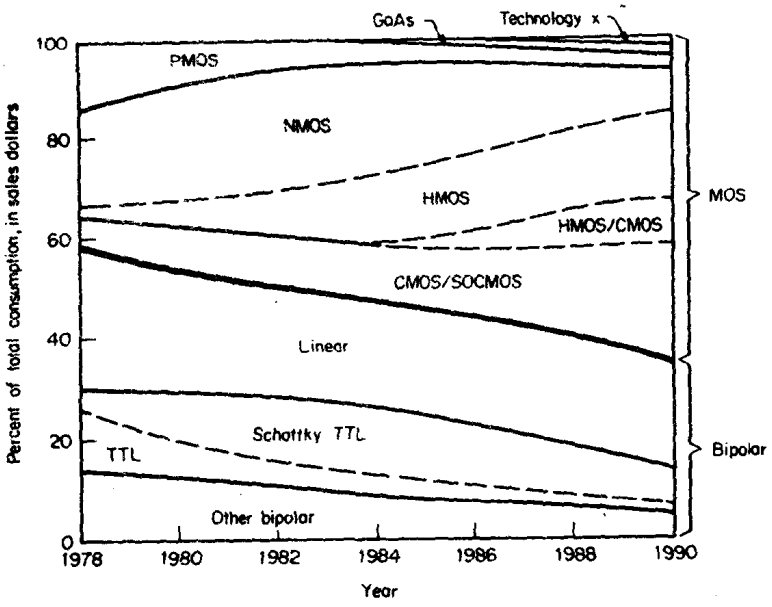


**Figure 1-1** **Market share for different semiconductor technologies.** ***(After Ref. 1. Copyright 1983. ICE Corporation.)***

small overlap with the gate. A generic term for such a device might be IGFET, which stands for insulated gate field-effect transistor. Though the two terms are used interchangeably, MOSFET is used more commonly.

In the discussion to follow, and throughout the rest of the book, we shall use $n$-channel transistors for our analysis. The analysis for the $p$-channel transistor follows simply by invoking duality; i.e., all semiconductor types are reversed, as well as the polarity of applied voltages.

In the $n$-channel transistor of Fig. 1-3, the semiconductor body (or substrate) is $p$-type and the source and drain diffusions are $n$-type. With no voltage applied to the gate, there is no conduction path between the source and drain because they are merely back-to-back diodes. When a voltage, positive with respect to the substrate, is applied to the gate and is of such a magnitude that it is greater than a certain threshold voltage $V_T$, then electrons are attracted to the surface of the semiconductor. (Note that electrons are minority carriers in the $p$-type substrate.) In fact, so many electrons are attracted to the surface that an extremely thin (approximately 50-Å) channel is formed, where the semiconductor actually changes from $p$- to $n$-type. Now, when a voltage is applied between source and drain, current can flow. The current flow is via majority carriers, since electrons flow through all $n$-type materials. (Bipolar transistor current carriers are minority carriers in the base region; they are affected by recombination phenomenon.) Transistor gain results from the ability of the gate voltage to modulate the channel conductivity. The electrons pile up at the oxide-semiconductor interface (i.e.,

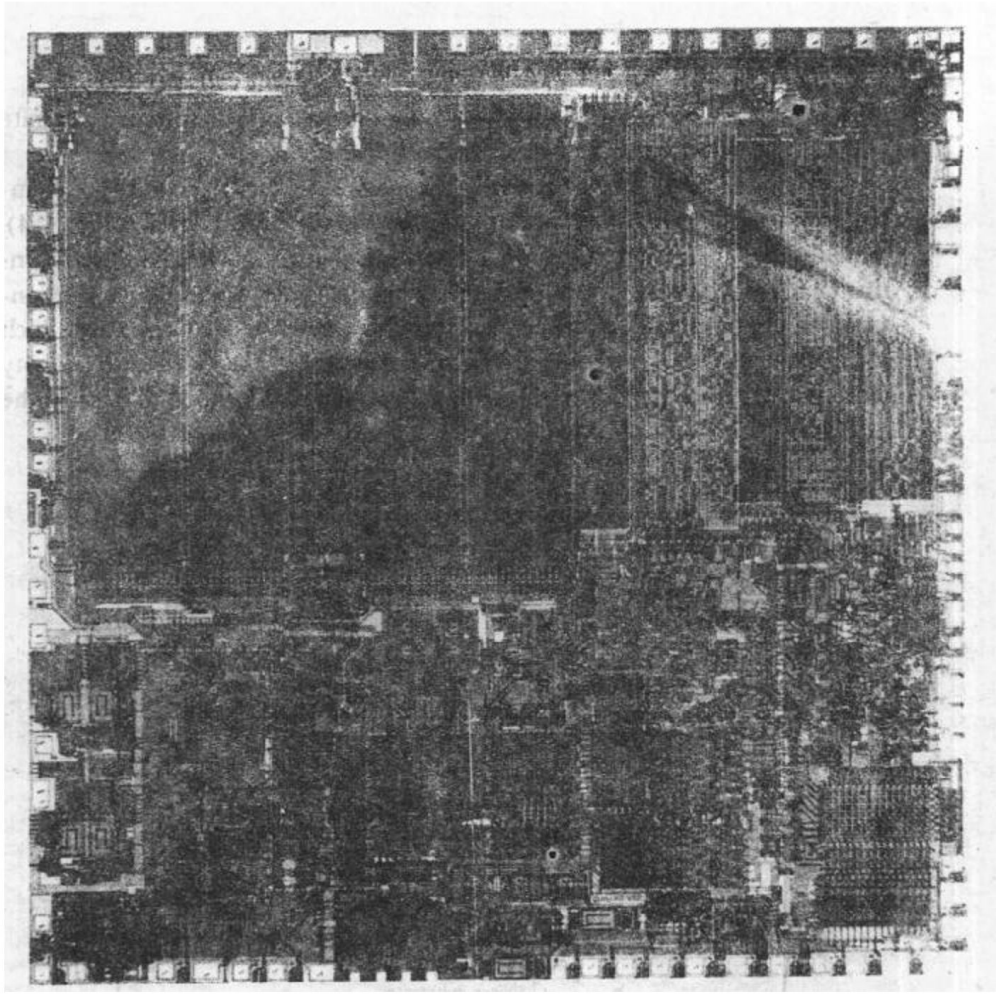

**Figure 1-2** The instruction decoder unit of Intel 432, a 32-bit microprocessor. It contains 110,000 transistors on a die size of 320 mils on a side. (*Intel Corp.*)

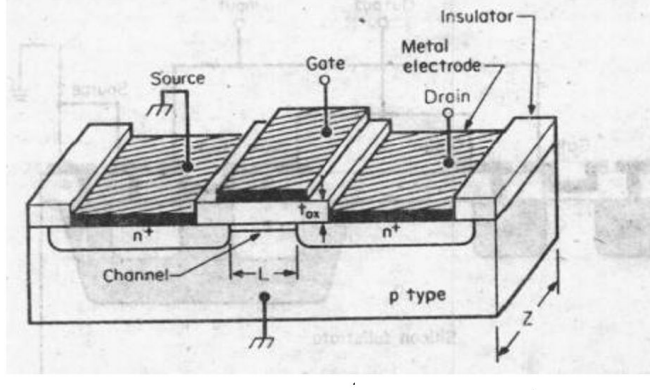


**Figure 1-3** An *n*-channel MOS transistor. (*After S. M. Sze, Physics of Semiconductor Devices. 2d ed., John Wiley and Sons, Chap. 8, 1981.*)

the silicon surface) rather than flow through the gate circuit because the gate oxide prevents any dc gate current from flowing.

The device just described requires a voltage to be applied before the channel is formed and is called an *enhancement-mode transistor* (see Fig. 1-4). Sometimes, when there are built-in positive charges at the oxide-semiconductor interface or when charges are deliberately introduced by ion implantation, a channel will be formed even when no gate voltage is applied. Such a transistor is called a *depletion-mode transistor,* because a reverse polarity (in this case, negative) gate voltage would have to be applied to deplete the

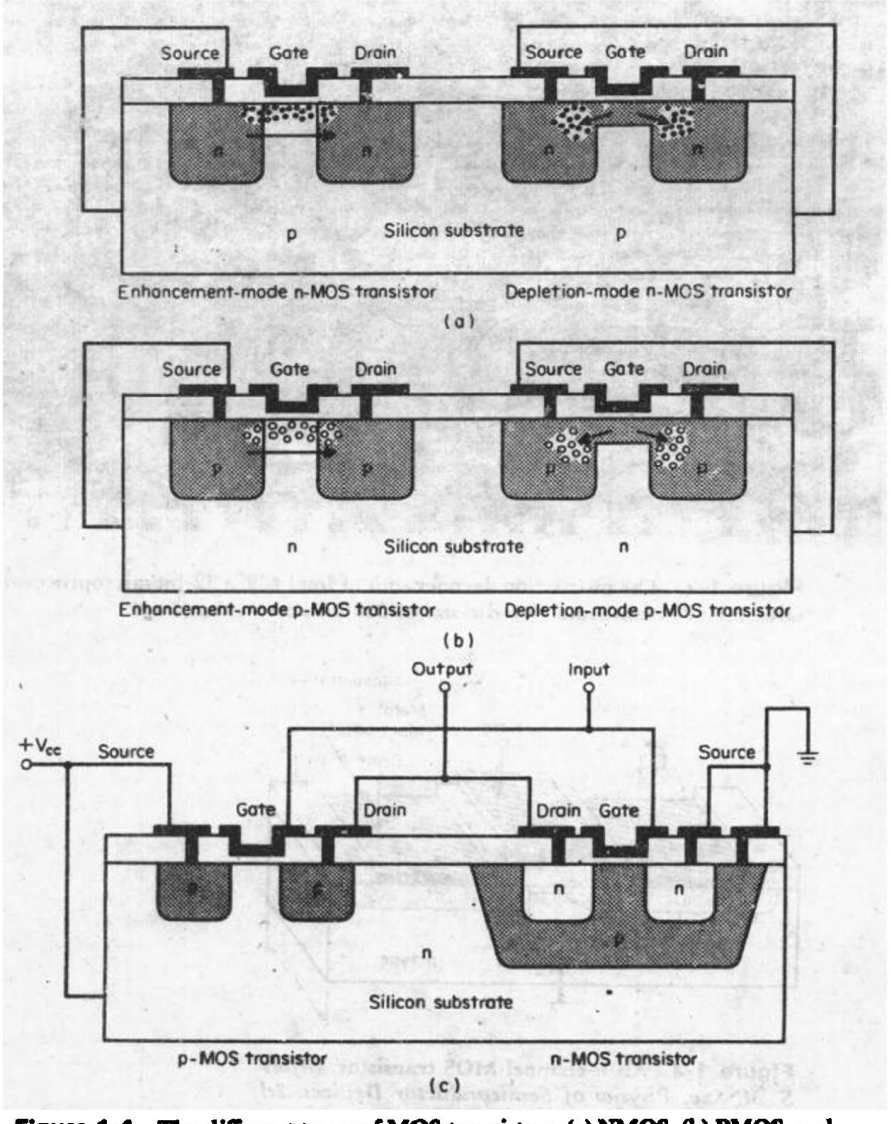


**Figure 1-4** **The different types of MOS transistors: (a) NMOS, (b) PMOS, and (c) CMOS.** ***(From J. D. Meindl, Scientific American, pp. 70–81, Sept. 1977.)***

channel of electrons and shut the device off. Its threshold voltage is thus negative. Note that the depletion-mode *n-channel devices still conduct via* electrons.

Transistors such as that of Fig. 1-3 which conduct via electrons are called *n-channel devices* (NMOS). One can build a similar set of *p*-channel (PMOS) devices that conduct via holes by reversing all voltage polarities and semiconductor types. That is, source and drain are *p*-type on *n*-type substrate, and the threshold voltage is negative for enhancement devices and positive for depletion devices, as shown in Fig. 1-4.

Notice that MOS transistors are always four-terminal devices. In the discussion so far, and in most applications, the substrate is often tied to the source, but one must always be conscious of tying the substrate (fourth terminal) some place.

If one were to fabricate PMOS and NMOS devices on the same substrate to build complementary MOS (CMOS) circuits, there would be a basic inconsistency in substrates. This is solved by using a *p*-tub diffusion to create the background for the *n*-channel devices, as shown in Fig. 1-4. Again note where the fourth terminal for each device is tied.

There are many symbols in use for MOS transistors. The more common ones are listed in Fig. 1-5 with set (*a*) being the most widely used. A good aid for remembering the symbols is that the arrow always points toward the *n* region, be it the *n* channel or the *n*-type semiconductor.

## 1-3 CHARACTERISTICS OF A MOS TRANSISTOR

Some of the characteristics of a MOS transistor are

1. ***Bilaterally Symmetric*** This means that the source and drain are electrically interchangeable. In NMOS, the more positive of the two is the drain. This is contrasted with bipolar transistors where the transistor gain would be severely degraded if the emitter and collector leads were interchanged.

2. ***Unipolar*** MOS transistors conduct exclusively via one type of carrier. This contrasts with bipolar transistors which, although they conduct primarily via one type of carrier (e.g., electrons in *npn*), do have both types of carriers flowing at the same time.

3. ***High-Input Impedance*** Because of the gate oxide, there is no dc path between the gate and the other terminals. The input impedance is then extremely high, and is primarily capacitive. Its dc resistance is greater than $10^{14}\ \Omega$.

4. ***Voltage-Controlled*** MOS devices are voltage-controlled. When that is coupled with the fact of high-input impedance, the result is a device

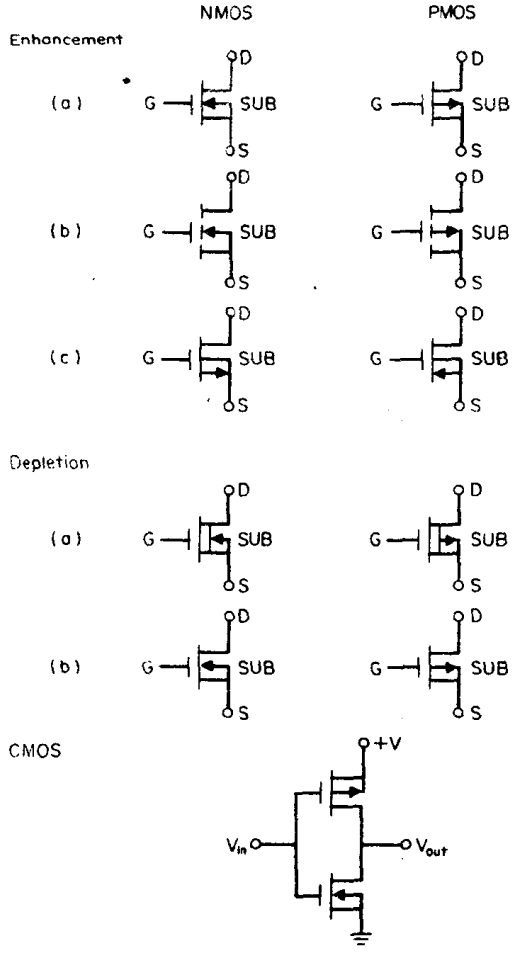


**Figure 1-5** **Logic symbols for MOS.**

with extremely low input power. One MOS transistor can then drive many other transistors similar to it, i.e., it has high fan-out capability. Bipolar transistors, on the other hand, are current-controlled devices.

5. ***Self-Isolating*** MOS ICs can be very dense because the MOS transistors are self-isolating. The drain of one device is naturally isolated from the drain or source of the others by means of back-to-back diodes. This eliminates the need for the deep, and hence also wide, isolation diffusions in bipolar processes.

## 1-4 MOS TRANSISTOR TRANSFER CHARACTERISTICS

If one ties the substrate to the source, then the transfer characteristics ($I_D$ versus $V_D$) of a MOS transistor would look like Fig. 1-6. For a given applied gate voltage that is greater than the threshold voltage $V_T$, the drain

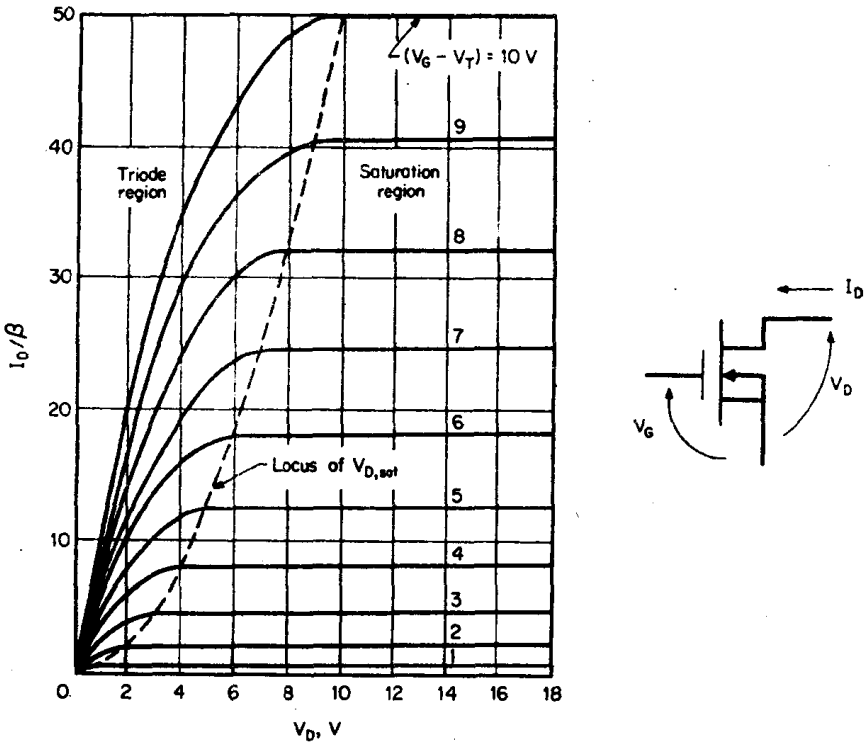


**Figure 1-6** **Idealized transfer characteristics ($I_D$ versus $V_D$) of a MOS transistor.**

current will rise linearly with increasing drain-to-source voltage. However, the rate of rise decreases until the drain current soon saturates to a constant value. At a higher gate voltage, the same shaped curve will result except the current values will be higher.

There are two regions in the transfer characteristics plot. The first, where current is rising, is the triode (or linear) region, where the drain current is described by

$$I_D = \beta[(V_G - V_T)V_D - \tfrac{1}{2}V_D^2] \tag{1-1}$$

where $\beta$ is a constant. The second region is the saturation region where the drain current does not depend on $V_D$:

$$I_D = \tfrac{1}{2}\beta(V_G - V_T)^2 \tag{1-2}$$

The point where the two lines meet is at the saturation drain voltage:

$$V_D = V_{D,sat} = V_G - V_T \tag{1-3}$$

## 1-5 COMPARISON BETWEEN MOS AND BIPOLAR TRANSISTORS

MOS transistors are generally smaller than bipolar transistors. Figure 1-7 shows a comparison between single MOS and bipolar transistors in terms

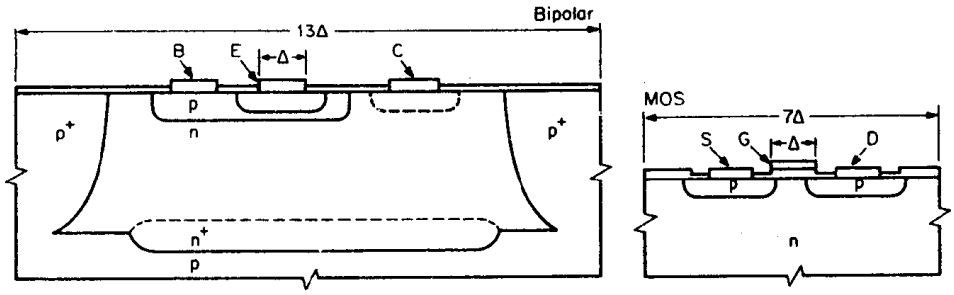


**Figure 1-7** Layout comparison of a bipolar transistor and a MOS transistor. *(After Ref. 4.)*

of size. For any given processing resolution Δ, the bipolar transistor will require a larger area because of the additional alignment tolerances from having three separate emitter, base, and collector masking and etching layers. But what really uses up the largest area is the isolation diffusion. In order to penetrate the deep $n$-epitaxial layer, the $p^+$ isolation diffusion has to spread laterally by approximately 70 percent of the layer depth. Recently, the use of an oxide trench to replace the isolation diffusion has increased the density of bipolar circuits significantly. And by using integrated injection logic ($I^2L$) for digital circuits, the density is increased to that approaching MOS. This is accomplished by operating the transistor in the inverse gain mode and using the $n$-epitaxial layer as emitter, so it can be made common to all transistors in the circuit.

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## PROBLEMS

1. What do we mean when we say MOSFETs are
   (a) Bilaterally symmetric?
   (b) Unipolar?
2. An $n$-channel enhancement-mode MOSFET conducts via (holes or electrons) and has a (positive or negative) threshold voltage. When the threshold voltage is made