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# **ULSI** Technology

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- S. M. SZE is UMC Chair Professor of the Electronics Engineering Dept. and Director of Microelectronics and Information Systems Research Center, the National Chiao Tung University, Taiwan, R.O.C. For many years he was a member of the technical staff at AT&T Bell Laboratories, Murray Hill, New Jersey. Dr. Sze has made pioneering contributions to semiconductor devices and processing technologies, including the invention of the nonvolatile memory (1967) and the fabrication of MOSFETs in the 0.1 µm regime (1982). Author or coauthor of more than 100 technical papers, Dr. Sze has written three books on semiconductor devices and edited six books on VLSI technology, high-speed devices, semiconductor sensors, and related topics. He has been elected Fellow of IEEE, member of the Academia Sinica, and member of the National Academy of Engineering.

To Our Colleagues and Students—
Past, Present, and Future
On the Centennial of Our University—
The National Chiao Tung University

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J. T. Yue Advanced Micro Devices Sunnyvale, California, USA ULSI Technology describes the theoretical and practical aspects of the most advanced state of electronics technology—ultralarge-scale integration (ULSI), where an integrated circuit (IC) chip contains over 10 million semiconductor devices. With ULSI technology, the cost of electronics products will decrease while the system functionality and performance will increase. The ULSI chips will result in the realization of smart and brilliant electronic systems, and in the improvement of quality of life and global productivity.

To fabricate IC chips with such complexity, we have to employ the most sophisticated process equipment, to follow the most precise process steps, and to adopt the most stringent cleanroom specifications. The basic process steps for ICs were considered in *VLSI Technology*, 2nd Edition (McGraw-Hill, 1988). Because of their importance to ULSI circuits, topics such as cleanroom technology, wafer-cleaning technology, manufacturing technology, and the rapid thermal process, which were essentially not covered in the 1988 VLSI book, are extensively discussed in *ULSI Technology*. In addition, many key processes, such as lithography, etching, metalization, and process integration, have been totally revised and updated. However, because of space limitations, certain classic topics such as crystal growth, conventional thermal processes, analytical technologies, and yield are covered only briefly or not covered at all. We suggest that our readers consult *VLSI Technology*, 2nd Edition for details.

In *ULSI Technology*, each chapter has an introduction that provides a general discussion of a specific aspect of ULSI processing. Subsequent sections present the basic science underlying individual process steps, the necessity for particular steps in achieving required parameters, and the tradeoffs in optimizing device performance and manufacturability. The problems at the end of each chapter form an integral part of the development of the topic.

The book is intended as a textbook for senior undergraduate or first-year graduate students in applied physics, electronics engineering, and materials science; it assumes that the reader has already acquired an introductory understanding of the physics and technology of semiconductor devices. Because it elaborates on IC processing technology in a detailed and comprehensive manner, it can also serve as a reference for those actively involved in integrated circuit fabrication and process development.

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#### **GROWTH OF THE INDUSTRY**

The United States has the largest electronics industry in the world, with a global market share of over 40%. Since 1958, the beginning of the integrated-circuit (IC) era, the factory sales of electronic products have increased by about thirty times [see Fig. 1, curve  $(a)^{1,2}$ ]. Electronics sales, which were \$303 billion in 1993, are projected to increase at an average annual rate of 8.5% and reach a half-trillion-dollar level by the year 2000. In the same period, the IC market itself has increased at an even higher rate [see Fig. 1, curve  $(b)^{1,2}$ ].\* IC sales in the United States were \$28 billion in 1993 and are expected to grow by 13% annually, reaching \$65 billion by the year 2000. The main impetuses for such phenomenal market growth are the intrinsic pervasiveness of electronic products and the continued technological breakthroughs in integrated circuits.

The world markets of electronics and semiconductor industries will grow at comparable rates. Figure 2 shows the 1993 world electronics industry with a global sales volume of \$679.7 billion. Also shown are the market shares of the six major electronics applications: computer and peripherals equipment at 32.3%, consumer electronics at 21.2%, telecommunication equipment at 16.5%, industrial electronics at 14.3%, defense and space at 11.5%, and transportation at 4.2%. By the year 2000, the world electronics industry is projected to reach \$1200 billion, which will surpass the automobile, chemical, and steel industries in sales volume.

Figure 3 shows the 1993 world semiconductor industry, with total sales of \$85.6 billion. Only 14% is related to optoelectronics and discrete semiconductor devices. IC sales constitute 86% of the total volume, with the largest segment being memory ICs, followed by microprocessor and microcontroller units, logic ICs, and analog ICs. In 2000, the semiconductor industry is projected to reach \$200 billion, with over \$170 billion in integrated circuits.

Figure 4 shows the market shares of the three major IC groups: MOSFET, bipolar transistor, and ICs made from III–V compound semiconductors.<sup>3</sup> At the beginning of the IC era, the IC market was broadly based on bipolar transistors. However, because of the advantages in device miniaturization, low power consumption, and high yield, sales volume of MOS-based ICs has increased steadily and in 1993 amounted to 75% of the total IC market. By the year 2000, MOS ICs will capture the largest market share (88%) of all ICs sold. This book, therefore, emphasizes MOS-related ULSI technology.

<sup>\*</sup>There were only two years in which the growths were negative: in 1974, due to the Middle East oil embargo, and in 1985, due to overproduction of personal computers.

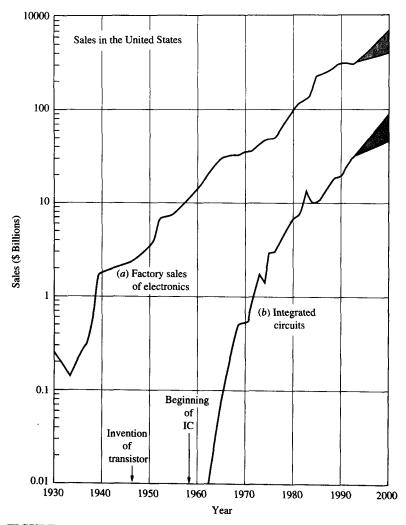


FIGURE 1
(a) Factory sales of electronics in the United States for the 64 years between 1930 and 1993 and projected to 2000. (b) Integrated circuit market in the United States for 32 years between 1962 and 1993 and projected to 2000. (After Refs. 1 and 2.)

## DEVICE MINIATURIZATION

Figure 5, curve (a), shows the rapid growth in the number of components per MOS memory chip.<sup>4,5</sup> Note that the MOS IC complexity has advanced from small-scale integration (SSI), to medium-scale integration (MSI), to large-scale integration (LSI), to very-large-scale integration (VLSI), and finally to ultralarge-scale integration (ULSI), which has 10<sup>7</sup> or more components per chip. We note that since 1975 the growth has been maintained at a rate of about 40% annually; in other words, the

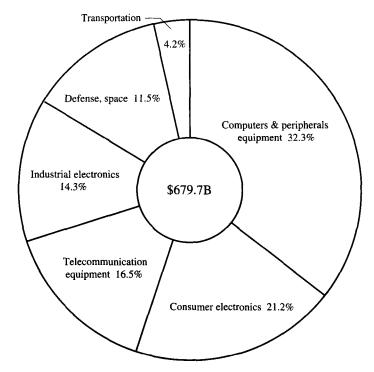


FIGURE 2
1993 world electronics industry. (After Dataguest, 1994.)

number of components has doubled every two years. At this rate, over 100 million components per chip will be available before the year 2000; in the early 21st century we will move into the gigabit range, with IC chips having more than one billion components.<sup>6,7</sup> Also shown in Fig. 5 is the growth of the number of components for bipolar, MESFET, and MODFET ICs. They are about two orders of magnitude lower in complexity compared with MOS-based ICs.

The most important factor in achieving the ULSI complexity is the continued reduction of the minimum device-feature length [see Fig. 6, curve (a)]. Since 1960, the annual rate of reduction has been 13%, which corresponds to a reduction by a factor of two every six years. At this rate, the minimum feature length will shrink from its present length of  $0.5~\mu m$  to  $0.2~\mu m$  in the year 2000. The junction depth of the source and drain junctions, and the gate oxide thickness are also being reduced at a similar rate as shown in curves (b) and (c) of Fig. 6, respectively.

The reduction of the device feature length and related dimensions has resulted in reduced overall device size and unit price per function. Figure 7 shows the relative price and size reductions. In the past fifty years, prices have gone down by 100 million times, and the size has been reduced by a factor of one billion. By 2000 the price per bit is expected to be less than 0.1 millicent for a 64-megabit memory chip. Similar price reductions are expected for logic ICs. Additional benefits from device

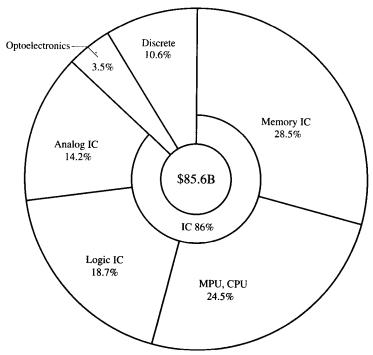


FIGURE 3
1993 world semiconductor industry. (After Dataquest, 1994.)

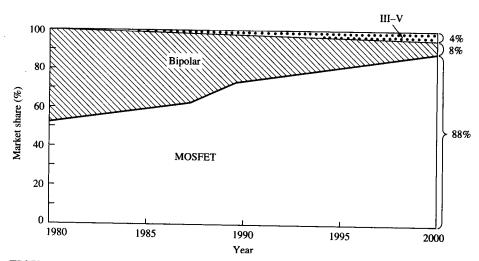


FIGURE 4
World IC market (1980–2000). (After Zdebel, Ref.3.)

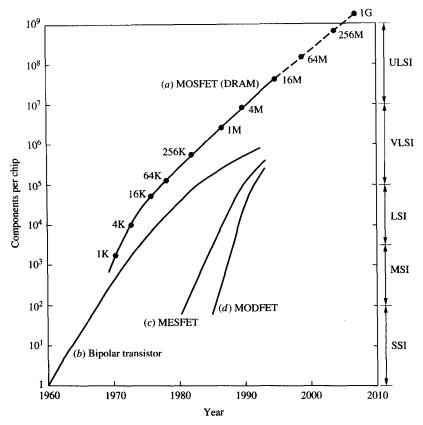
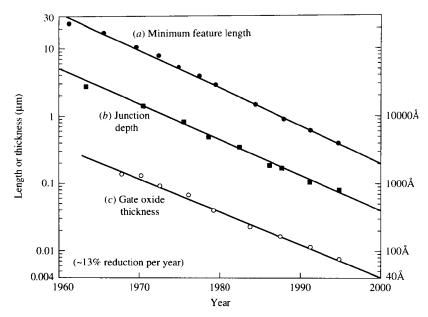


FIGURE 5 (a) Exponential growth of the number of components per MOS IC chip. (After Moore, Ref. 4, and Myers, Ref. 5.) (b), (c). and (d) Components per chip versus year for bipolar, MESFET, and MODFET ICs, respectively.

miniaturization include improvement of device speed (which varies inversely with the device feature length) and reduction of power consumption (which varies approximately with the square of the feature length). Higher speeds lead to expanded IC functional throughput rates, so that future ICs can perform data processing, numerical computation, and signal conditioning at 100 and higher gigabit-per-second rates. 9 Reduced power consumption results in lowering the energy required for each switching operation. Since 1960 the required energy, called the power-delay product, has decreased by six orders of magnitude. 10

## ORGANIZATION OF THE BOOK

Figure 8 shows how the 12 chapters of this book are organized. Chapter 1 considers cleanroom technology. The continued miniaturization in ULSI devices implies more



**FIGURE 6** Exponential decrease of (a) minimum feature length, (b) junction depth, and (c) gate oxide thickness of MOSFET.

stringent requirements with respect to contamination control. Without an ultraclean processing environment, ULSI circuits simply cannot be realized.<sup>11</sup>

ULSI technology is synonymous with *silicon* ULSI technology. The unique combination of silicon's adequate bandgap, stable oxide, and abundance in nature ensures that in the foreseeable future no other semiconductor will seriously challenge its preeminent position in ULSI applications. Some important properties of silicon are listed in Appendix A.

Once the silicon wafers are in the cleanroom, we enter into the wafer-processing sequence, described in Chapters 2 through 8 and depicted in the wafer-shaped central circle of Fig. 8. Each of these chapters considers a specific process step. Of course, many processing steps are repeated many times in IC fabrication; for example, lithography and etching steps may be repeated 10 to 20 times. In ULSI technology the wafer-cleaning technology is as important as the cleanroom technology. Without a contamination-free wafer surface, the ICs will suffer from low yield and poor reliability. Because of limitations on the total length of the book, many classic topics, such as crystal growth, oxidation, diffusion, and ion implantation, are only briefly mentioned. The reader may consult textbooks on VLSI technology for details. 12

The individual processing steps described in Chapters 2 through 8 are combined in Chapter 9 to form devices and integrated circuits. Chapter 9 considers the fundamental building process modules and four important IC families: CMOS (complementary MOSFET), bipolar ICs, BiCMOS (a combination of bipolar and CMOS),

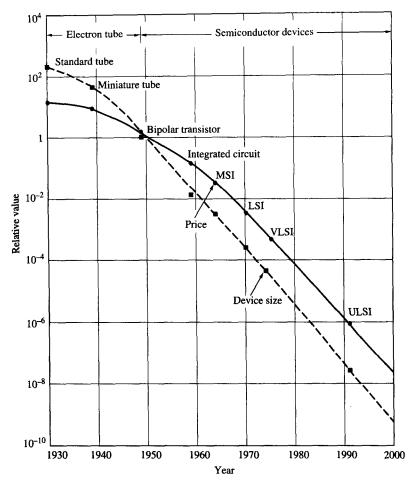
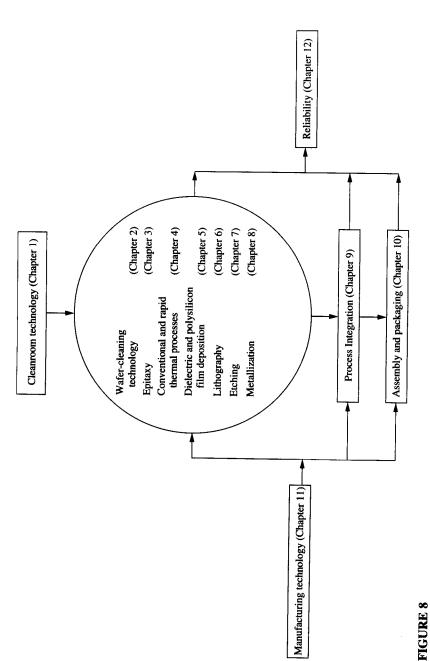


FIGURE 7
Price and size reduction of active electronic compents. (After Shoda, Ref. 8.)

and MOS memory ICs. After the completely processed wafers are tested, those chips that pass the tests are ready to be packaged. Chapter 10 describes the assembly and packaging of ULSI chips. Chapter 11 considers the manufacturing technology, that is, the strategy and logistics to implement various technologies to produce ULSI chips that meet customers' specifications in a timely fashion and to generate adequate return on investment for the IC manufacturer. Chapter 12 describes a multitude of reliability issues related to ULSI processes. As device dimensions move to the sub-half-micron and sub-quarter-micron regime, ULSI processing becomes more automated, resulting in tighter control of all processing parameters. At every step of production, from wafer cleaning to device packaging, numerous requirements are being imposed to improve the device performance and reliability.

To keep the notation simple in this book, we sometimes found it necessary to use a symbol more than once, with different meanings. However, within each chapter a



Organization of this book.

symbol has only one meaning and is defined the first time it appears. Many symbols do have the same or similar meanings consistently throughout this book; they are summarized in Appendix B.\*

ULSI technology is presently moving at a rapid pace. The number of ULSI publications has doubled every year since 1990, the beginning of the ULSI era. Many topics, such as lithography, rapid thermal processing, and metallization, are still under intensive study. Their ultimate capabilities are not fully understood. The material presented in this book is intended to serve as a foundation. The references listed at the end of each chapter can supply more information.

#### REFERENCES

- 1. 1994 Electronic Market Data Book, Electronic Industries Association, Washington, D.C., 1994.
- 2. 1994 Annual Report of Semiconductor Industry, Industrial Technology Research Institute, Hsinchu, Taiwan, ROC, 1994.
- 3. P. J. Zdebel, "Current Status of High Performance Silicon Bipolar Technology," 14th Annual IEEE GaAs IC Symp. Tech. Digest, 15 (1992).
- 4. G. Moore, "VLSI, What Does the Future Hold," Electron Aust., 42, 14 (1980).
- 5. W. Myers, "The Drive to the Year 2000," *IEEE Micro*, **11**, 10 (1991).
- 6. P. K. Chatterjee and G. B. Larrabee, "Gigabit Age Microelectronics and Their Manufacture," *IEEE Trans. VLSI Syst.* 1, 7 (1993).
- 7. K. Mori, H. Yamada, and S. Takizawa, "System on Chip Age," Proceedings of the International Symposium on VLSI Technology, Systems, and Applications, k15 (1993).
- 8. K. Shoda, "Home Electronics in the 1990s," Proceedings of the International Symposium on VLSI Technology, Systems, and Applications, 1(1991).
- 9. H. Komiya, M. Yoshimoto, and H. Ishikura, "Future Technological and Economic Prospects for VLSI," *IEICE Trans. Electron.* **E76-C**, 1555 (1993).
- 10. R. W. Keyes, "Limitations of Small Devices and Large Systems," in N. G. Einspruch, Ed., VLSI Electronics, Academic, New York, 1981, Vol. 1, p. 186.
- 11. T. Ohmi, "ULSI Reliability through Ultraclean Processing," *Proc. IEEE*, 81, 716 (1993).
- 12. For example, S. M. Sze, Ed., VLSI Technology, 2nd Ed., McGraw-Hill, New York, 1988.

<sup>\*</sup>Also included are the International System of Units (Appendix C) and Physical Constants (Appendix D).

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