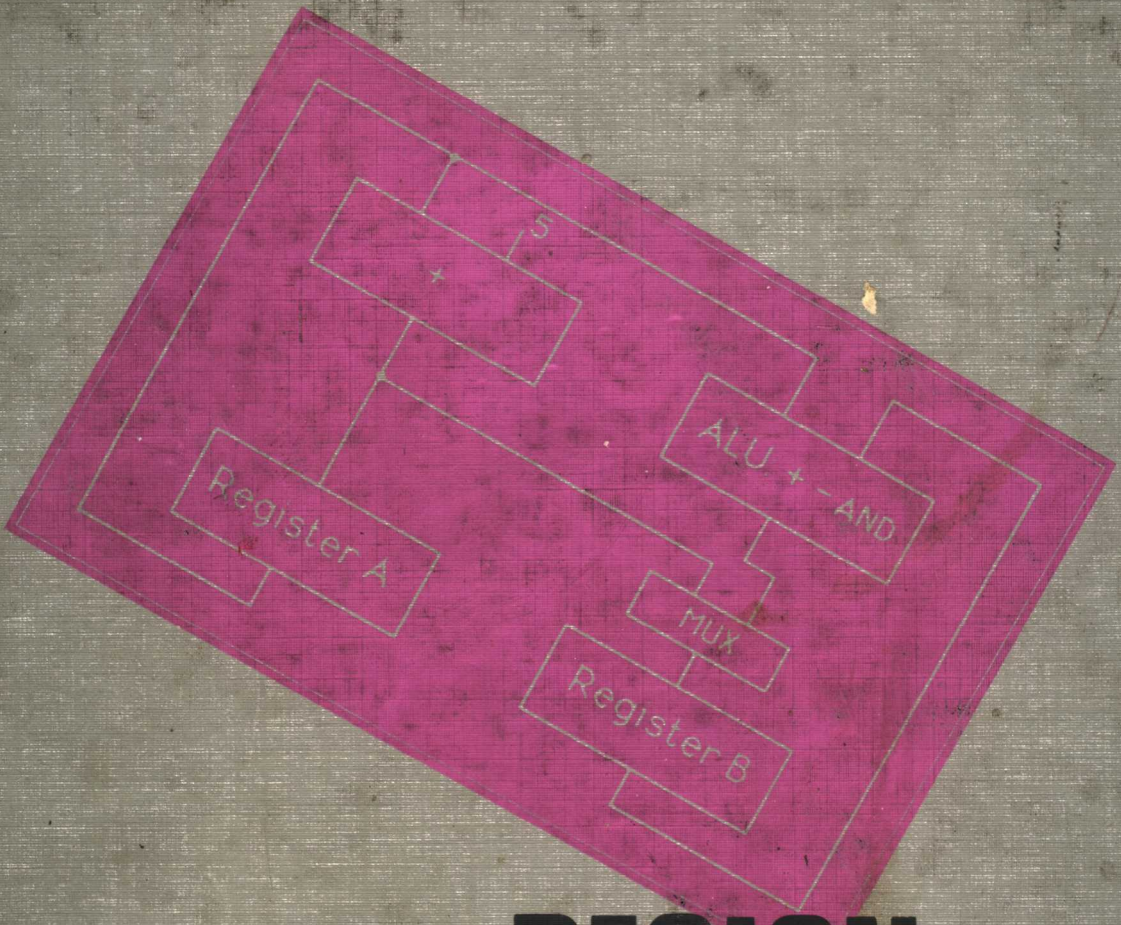
ADVANCES IN CAD FOR VLSI, Volume 6



DESIGN METHODOLOGIES

Edited by S. Goto

North-Holland

Design Methodologies

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INTRODUCTION TO THE SERIES

VLSI technology has matured to the extent that hundreds of thousands or even millions of transistors can be integrated in a single silicon chip, and VLSIs are now the key to the design of efficient electronic systems. It therefore follows that the problems of designing integrated circuits are also becoming increasingly complex. A wide variety of topics on computer aided design (CAD) have emerged. This is a period when no-one can be a specialist in all of the topics in CAD for VLSI, and the whole area is beyond the scope of a single volume. The requirement for information and communication is increasing.

In 1982, Dr. R. Morel, at that time Acquisition Editor at North-Holland, conceived a range of projects to relieve this problem. Initially this resulted in "INTEGRATION, the VLSI journal", a quarterly aimed at speeding up communication among VLSI designers. It was further decided to launch a book series in the field, an idea enthusiastically supported by Dr. L. Spaanenburg, Editor-in-Chief of Integration. Dr. Morel approached me to edit this series.

It was agreed that the book series should be aimed towards a comprehensive reference for those already active in areas of VLSI CAD. Each volume editor was asked to compile a present state of the art, scattered in many journals. The book series therefore should help CAD specialists to get a better understanding of the problems in neighbouring areas by reading particular volumes. At the same time, it should give novices a foothold for doing research in areas of VLSI CAD, although a basic knowledge of VLSI technologies and design methods will aid understanding.

The book series, entitled "Advances in CAD for VLSI" consists of the following seven volumes:

Vol. 1	Process and Device Modeling	W. Engl (RTWH Aachen, FRG)
Vol. 2	Logic Design and Simulation	E. Hörbst (Siemens, Munich, FRG)
Vol. 3	Circuit Analysis, Simulation and Design (Part I and II)	A. Ruehli (IBM, Yorktown Heights, USA)
Vol. 4	Layout Design and Verification	T. Ohtsuki (Waseda University, Tokyo, Japan)
Vol. 5	VLSI Testing	T. Williams (IBM, Boulder, USA)
Vol. 6	Design Methodologies	S. Goto (NEC, Kawasaki, Japan)
Vol. 7	Hardware Description Languages	R. Hartenstein (Univ. of Kaiserslautern, FRG)

The first five volumes deal with major phases of VLSI design separately. The following two volumes are devoted to recent approaches which span the whole design phase. The integrated approach combining system design and VLSI design is also treated in these volumes, and it will suggest a major trend in the future. Each volume is reasonably self-contained so that it can be read independently.

All of the volumes were intended to include up-to-date results, and the latest developments with a good balance between theory and practice. Moreover, emphasis was placed on basic techniques, methods and algorithms rather than on descriptions of existing design tools. This, I hope, will prevent obsolescence at the time of publication. Only the readers however, can judge to what extent our intentions were successful.

Selecting the volume editors was not an easy task. In order to produce a quality book series, it was necessary to utilise authorities well known in their respective fields who in turn would attract outstanding contributors. Those active in VLSI design had other commitments. I was relying on their volunteering spirit, and they in turn faced the same dilemma with their authors. It was a great pleasure to me that ultimately we were able to attract such an excellent team of editors and authors.

The Series Editor wishes to thank all of the volume editors and authors for the time and effort they put into the book series, and especially Prof. W. Engl for his assistance in arranging other volume editors. I also thank Dr. E. Fredriksson, Dr. J. Julianus and Dr. R. Morel of North-Holland for their continuing effort to bring the book series from the initial planning stage to final publication.

Waseda University
Tokyo, Japan
1985

Tatsuo Ohtsuki

PREFACE

Recent advances in microelectronics technology have drastically changed design methodologies in VLSI design. Design methodologies adopted in dealing with a more than 100,000 element VLSI should be essentially different from those for small scale integrated circuits. Establishing an efficient methodology is one of the keys to successful VLSI chip design at the present time. A great number of approaches have been tried in an attempt to manage the ever increasing VLSI complexities up to now. These approaches are classified into the three following categories:

(1) Design styles and strategies
(2) VLSI architecture and implementation techniques
(3) New design tools

These approaches are imperative to ensure functional, logical, electrical and geometrical correctness while maintaining a short design time. This volume discusses VLSI design methodologies according to the above three categories.

The first part deals with design styles and strategies, which exploit circuit structure in the form of regularity and hierarchy to manage the complexity. Various layout styles and strategies have been proposed up to now and have been in practical use for custom or semi-custom LSIs. Gate Array, Master Slice, Master Image, Standard Cell and PLA are typical layout design styles. The choice regarding each layout style to embark on is a result of careful consideration on many factors, such as chip size, power dissipation, delay time, design cost and design turnaround time.

Three papers are presented for the design styles in the first part. They discuss advantages or disadvantages between different design styles. "Custom and Semi-Custom Design" by Erdelyi et al. describes gate array, master slice master image and hand-honed design. "PLA and Custom Design" by Obrebska et al. deals with random logic design, microprogrammed design and PLA design. "Gate Array and Standard Cell" by DeCamp et al. addresses gate array and standard cell.

A key to design strategies is the use of hierarchy in the design process. Hierarchical design is to breakdown a complex system into manageable components. Two papers are presented on this problem. One is "Hierarchical Design Methodologies: A VLSI Necessity" by Lang and McCormick and the other one is "Abstraction Requirements in Hierarchical Design Methods" by Niessen.

The second part deals with VLSI architecture and implementation techniques, which establish a new architecture or a new logic design technology for achieving efficient VLSI hardware. Since many large and complicated systems can be implemented in VLSI chips, their architecture and implementation techniques should be essentially different from existing ones in regard to quality.

Seven papers herein cover this area, from theoretical and practical points of view. Two of them deal with hardware algorithms, one with self-checking processor design, one with signal processing architecture, one with signal processor architecture, and the last two deal with 32 bit microprocessor design.

A hardware algorithm is a parallel algorithm to be implemented as hardware. Design of hardware algorithms is an essential job in logic design, since the efficiency of hardware implemented in VLSI largely depends upon the feature of algorithms. "Design and Analysis of Hardware Algorithms" by Yasuura summarizes recent results in this area, and "Towards a Computerized Opitmal Design of VLSI Systolic Arrays" by Moldovan reports a methodology for algorithmically designing specialized systolic arrays.

"Design Approach to Self-Checking VLSI Processors" by Nanya presents a new design methodology for strong fault secure processors with its evalutation Intel's 8080 microprocessor.

"Recursive and Concurrent VLSI Architectures for Signal Processing" by Yung and Allen deals with algorithm specification and VLSI implementation for major constituents of signal processing systems, which includes multiplier, adder and matrix computation.

"Signal Processor Design Methodology" by Nishitani describes digital signal processing requirements and design features on single chip software controllable signal processors with its evaluation for NEC 7720.

The last two papers in the second part deal with 32 bit microprocessor design. "Experience with Design of a 32 bit Microprocessor" by Suzuki describes VLSI architecture for a general purpose, bytecode-emulating microprocessor tuned to execute Smalltalk bytecodes efficiently. "32 bit Microprocessor Design" by Yoshimura et al. discusses design strategy and design automation tools in the development of VLSI microprocessors together with the configuration and design technologies.

The last part deals with new design tools, which are required to manage the increasingly extensive VLSI complexities. Four advanced design tools are herein presented, such as automatic synthesizer, artificial intelligent based CAD system, design automation machine and design database in networked workstations.

"Automatic Data Path Synthesis" by Thomas describes automatic synthesis at the system level of design, which includes various synthesizer based on expert system, graph model or mathematical programming.

"Artificial Intelligent Approach to VLSI Design" by Fujita et al. gives an overview on this subject. It discusses algorithmic approaches and artificial intelligent approaches, and describes a new interactive routing system for VLSI design based on artificial intelligent approach.

"Design Automation Machine" by Koike and Ohmori, discusses special purpose CAD machines for logic simulation, routing, design rule checking and circuit simulation with emphasis on architectural support or hardware support for CAD algorithms.

The last paper is "Design Database" by Katz, which describes VLSI design data base and its management system in a dispersed computer environment of networked workstations and design database server.

Reflecting the rapid progress achieved in VLSI technology, VLSI design methodologies are becoming more and more important. VLSI design methodologies are still in the infancy stage, and are still making very fast progress. I believe this book will help the readers to catch up with major progress in this field.

Satoshi Goto
NEC Corporation
Kawaski, Japan
October 1985

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PART 1

DESIGN STYLES AND STRATEGIES

DESIGN METHODOLOGIES
S. Goto (Editor)

Chapter 1

CUSTOM AND SEMI-CUSTOM DESIGN

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MEANING OF CUSTOM AND SEMI-CUSTOM IN VLSI

INTRODUCTION

Customization implies uniqueness. Custom homes, automobiles, or clothes usually carry a connotation of better quality, higher cost and limited affordability. These attributes are also expected when one begins to talk about custom integrated circuits. Millions of integrated circuits are being fabricated; most can be classified as one of several hundred large volume part numbers that are readily available off-the-shelf. The large volume results in good economies of fabrication and, consequently, low prices.

A similar scenario can be painted for home and commercial computing systems, measuring instruments, home appliances, etc. In each case the predetermined and usually optimized configuration appeals to a large number of users by which it assures a large market which is the necessary prerequisite for setting up volume production and the resultant low market price of the product.

Why would one want to buy anything but this type of a volume produced product? Some of the reasons:

- New needs, not anticipated in the offering of existing products.
- Unsatisfactory performance of volume products.
- Desire for still lower cost.
- Desire to find the optimal solution to a given need.

Customization generally applies only to some aspect of the design activity. For example, a custom home usually has a unique design and landscaping features as well as some unique floor or ceiling material, but typically uses ordinary framing lumber, plyscore, wallboards and nails, just to mention a few building materials.

Customizing only certain aspects of the design also applies to Very Large Scale Integration (VLSI). A totally unique, customized architecture may be implemented with gate arrays or some standard cell library. On the other hand, a common architecture may be implemented by utilizing highly customized circuit or logical macros. Full customization of all aspects of the design is rarely practical because they are interdependent to a large degree. The logic designer cannot start customizing until the architecture is defined; the circuit designer must also wait for the logical functions to be defined before beginning the custom design. The desire for rapid progress usually requires paralleling some design activity, which in turn requires some standardization; e.g., wiring pitches, signal levels and basic circuit elements.

The term Very Large Scale Integration refers to the large number of logical functions, circuits, and transistors that are integrated onto a single chip by unique methods of fabrication. Typically, the same architecture and logical functions can be implemented with different degrees of integration. But, when the total function for a chip is specified, the technology choices become limited. All circuit components and interconnections must be able to fit on the chip, and the combined power dissipation must be such that the chip temperature remains below some specific value. The maximum allowable complexity of a chip is limited by the following factors:

- Chip size
- Minimum design geometries allowed by process
- Chip power dissipation capability limitations
- Data volume limitations of the design tools

Customization involves the accommodation of the above factors to achieve the desired design objectives. Major physical design approaches (gate array, master slice, master image, hand-honed macros, and hand-honed design) need to be discussed to appreciate the effect of customization.

GATE ARRAYS

A simple form of a VLSI chip has a large number of identical transistors that are arranged in an array; design aids are provided to interconnect these transistors to form the desired circuits and logic functions [1,2]. Arranging the transistors and the connection points very regularly provides the best possible general connectivity and relative ease of design automation. As the design progresses, the interconnections become more and more difficult to route. Some late nets end up with long

metal paths and produce undesirable delay characteristics in the finished chip. Figure 1 shows the diffusion and polysilicon levels of a gate array layout. The regularity of the pattern is very noticeable.

While the logical function and the architecture may be highly customized, the physical implementation of the circuits is totally at the mercy of the wiring program. In gate arrays, there is no customization of the circuits or the individual transistors. Only contact and metallization levels are unique to a particular design.

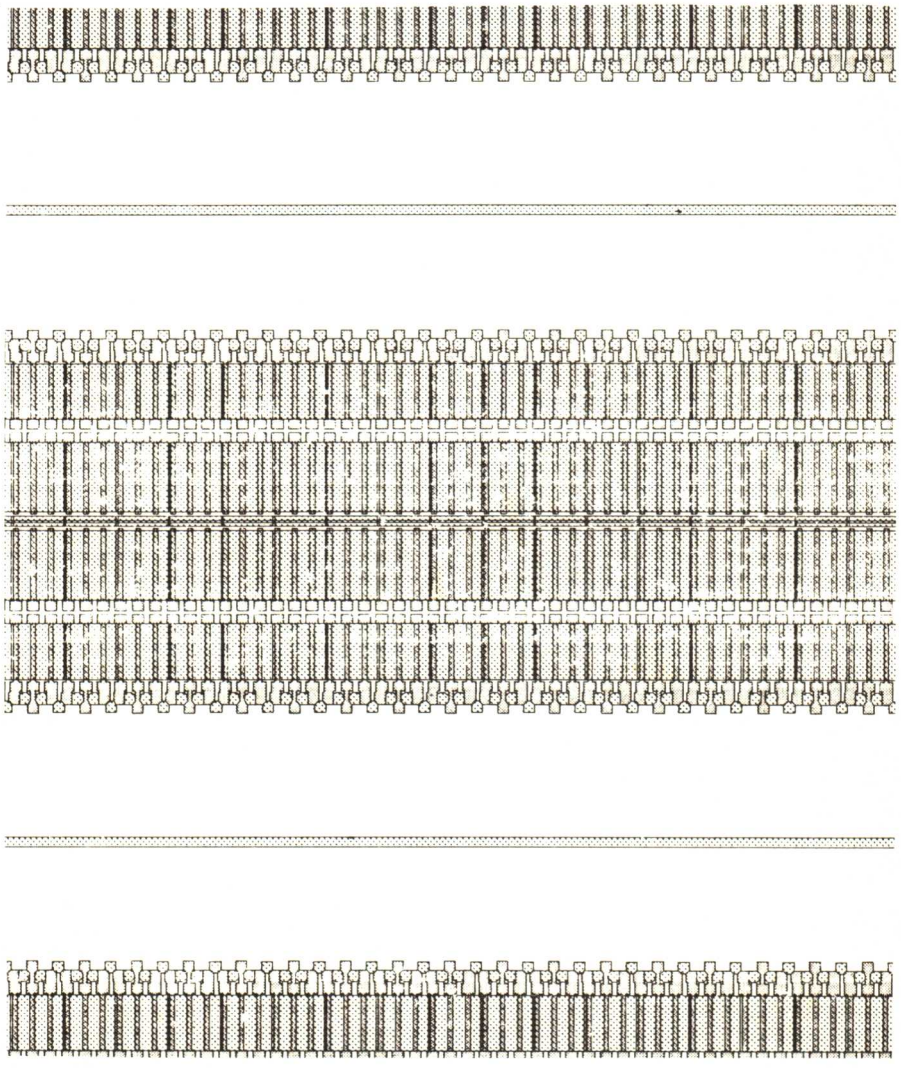

Figure 1. Gate Array Layout Structure

MASTER SLICE

If the physical dimensions of the transistors are not all the same but different sizes are used to provide different current capability, there will be a preferred set of interconnections of device groups to form logic circuits [3]. The anticipated interconnections imply a preferred placement of the devices and result in better implementation of particular functions than would be possible with the simple gate array. Generally, the small clusters of devices can implement a variety of simple logic functions, which then can be interconnected to form the desired overall chip function. Usually, the silicon-based levels which are prefabricated are common to many designs. The uniqueness of the design is determined by the metallization and related mask levels. While customization of device sizes and placements produces some advantages compared to the gate arrays, there is also a penalty. This arises from the fact that the device set for the most complex cell must also be present in the least complex cell because all background cells are the same. Figure 2 shows a typical master slice layout with repeating cell patterns.

MASTER IMAGE

This is an improvement over the master slice; i. e., the background levels can also be personalized. As a result, only the needed devices are put into each cell. There is a good variety of predesigned functional cells such as NAND functions, NOR functions and latches. Usually a design system places and interconnects these cells into the necessary configuration [4].

In this mode of design, every chip is unique but the layout is very regular, conforming to a set of constraints. The design of every function is customized at all levels to the best implementation of the function. However, the same function is always implemented with that one physical layout anytime it is used on the chip or on any other chip as long as that particular master image design system is used. The constraints on the layout assure that the pieces will fit together. Such constraints are the number of wiring channels and connection points that can be made to a cell as well as the locations of the connection points. Figure 3 shows a master image layout.

While this layout has a cellular structure, it is difficult to recognize because adjacent cells are generally not alike. Programmable Logic Arrays (PLAs) are found as macros on master image designs for implementing large pieces of combinatorial logic.

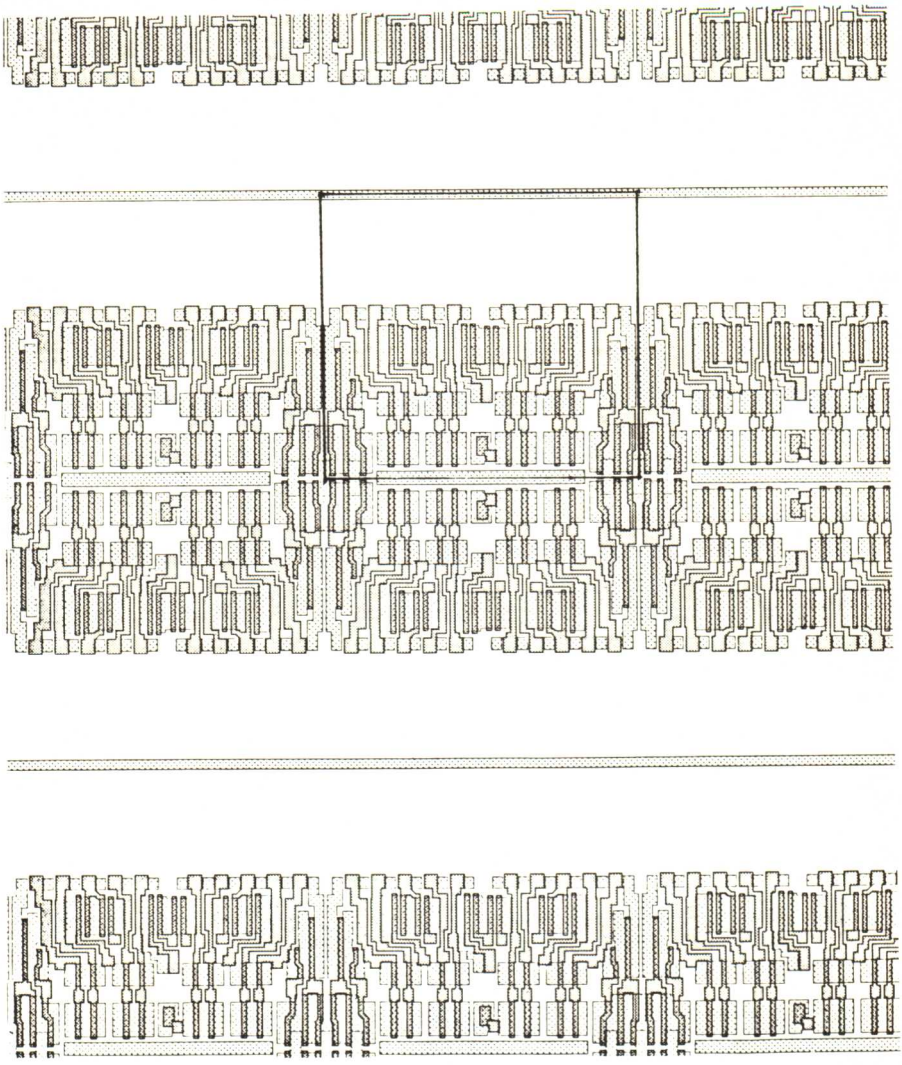

Figure 2. Master Slice Layout Structure