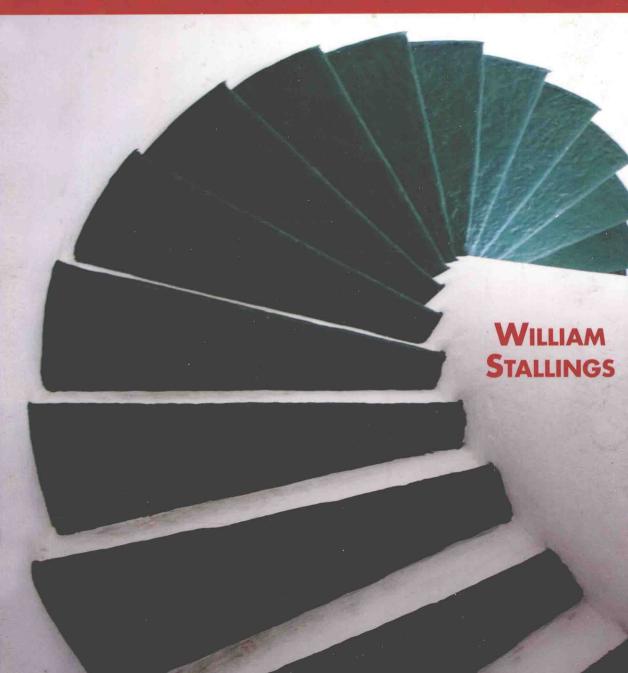


COMPUTER ORGANIZATION AND ARCHITECTURE

Designing for Performance



COMPUTER ORGANIZATION AND ARCHITECTURE DESIGNING FOR PERFORMANCE EIGHTH EDITION

William Stallings

Library of Congress Cataloging-in-Publication Data On File

Vice President and Editorial Director: Marcia J. Horton

Editor-in-Chief: Michael Hirsch Executive Editor: Tracy Dunkelberger Associate Editor: Melinda Haggerty Marketing Manager: Erin Davis

Senior Managing Editor: Scott Disanno Production Editor: Rose Kernan Operations Specialist: Lisa McDowell

Art Director: Kenny Beck Cover Design: Kristine Carney

Director, Image Resource Center: Melinda Patelli Manager, Rights and Permissions: Zina Arabia

Manager, Visual Research: Beth Brenzel

Manager, Cover Visual Research & Permissions: Karen Sanatar

Composition: Rakesh Poddar, Aptara[®], Inc.

Cover Image: Picturegarden/Image Bank/Getty Images, Inc.

Copyright © 2010, 2006 by Pearson Education, Inc., Upper Saddle River, New Jersey, 07458.

Pearson Prentice Hall. All rights reserved. Printed in the United States of America. This publication is protected by Copyright and permission should be obtained from the publisher prior to any prohibited reproduction, storage in a retrieval system, or transmission in any form or by any means, electronic, mechanical, photocopying, recording, or likewise. For information regarding permission(s), write to: Rights and Permissions Department.

Pearson Prentice Hall^{IM} is a trademark of Pearson Education, Inc. Pearson[®] is a registered trademark of Pearson plc Prentice Hall[®] is a registered trademark of Pearson Education, Inc.

Pearson Education LTD. London Pearson Education Singapore, Pte. Ltd Pearson Education, Canada, Ltd Pearson Education—Japan Pearson Education Australia PTY, Limited Pearson Education North Asia Ltd Pearson Educación de Mexico, S.A. de C.V. Pearson Education Malaysia, Pte. Ltd Pearson Education, Upper Saddle River, New Jersey

Prentice Hall is an imprint of



To Tricia (ATS),
my loving wife the kindest
and gentlest person



WEB SITE FOR COMPUTER ORGANIZATION AND ARCHITECTURE, EIGHTH EDITION

The Web site at WilliamStallings.com/COA/COA8e.html provides support for instructors and students using the book. It includes the following elements.



Course Support Materials

- A set of **PowerPoint** slides for use as lecture aids.
- Copies of figures from the book in PDF format.
- Copies of tables from the book in PDF format.
- Computer Science Student Resource Site: contains a number of links and documents that students may find useful in their ongoing computer science education.
 The site includes a review of basic, relevant mathematics; advice on research, writing, and doing homework problems; links to computer science research resources, such as report repositories and bibliographies; and other useful links.
- An errata sheet for the book, updated at most monthly.



Supplemental Documents

- A set of supplemental homework problems with solutions. Students can enhance their understanding of the material by working out the solutions to these problems and then checking their answers.
- Three online chapters: number systems, digital logic, and IA-64 architecture
- Nine online appendices that expand on the treatment in the book. Topics include recursion, and various topics related to memory.
- All of the Intel x86 and ARM architecture material from the book reproduced in two PDF documents for easy reference.
- · Other useful documents



COA Courses

The Web site includes links to Web sites for courses taught using the book. These sites can provide useful ideas about scheduling and topic ordering, as well as a number of useful handouts and other materials.



Useful Web Sites

The Web site includes links to relevant Web sites. The links cover a broad spectrum of topics and will enable students to explore timely issues in greater depth.



Internet Mailing List

An Internet mailing list is maintained so that instructors using this book can exchange information, suggestions, and questions with each other and the author. Subscription information is provided at the book's Web site.



Simulation Tools for COA Projects

The Web site includes a number of interactive simulation tools, which are keyed to the topics of the book. The Web site also includes links to the SimpleScalar and SMPCache web sites. These are two software packages that serve as frameworks for project implementation. Each site includes downloadable software and background information.

ABOUT THE AUTHOR

William Stallings has made a unique contribution to understanding the broad sweep of technical developments in computer security, computer networking and computer architecture. He has authored 17 titles, and counting revised editions, a total of 42 books on various aspects of these subjects. His writings have appeared in numerous ACM and IEEE publications, including the *Proceedings of the IEEE* and *ACM Computing Reviews*.

He has 10 times received the award for the best Computer Science textbook of the year from the Text and Academic Authors Association.

In over 30 years in the field, he has been a technical contributor, technical manager, and an executive with several high-technology firms. He has designed and implemented both TCP/IP-based and OSI-based protocol suites on a variety of computers and operating systems, ranging from microcomputers to mainframes. As a consultant, he has advised government agencies, computer and software vendors, and major users on the design, selection, and use of networking software and products.

He created and maintains the **Computer Science Student Resource Site** at WilliamStallings.com/StudentSupport.html. This site provides documents and links on a variety of subjects of general interest to computer science students (and professionals). He is a member of the editorial board of Cryptologia, a scholarly journal devoted to all aspects of cryptology.

Dr. Stallings holds a PhD from M.I.T. in Computer Science and a B.S. from Notre Dame in electrical engineering.

PREFACE

OBJECTIVES

This book is about the structure and function of computers. Its purpose is to present, as clearly and completely as possible, the nature and characteristics of modern-day computer systems.

This task is challenging for several reasons. First, there is a tremendous variety of products that can rightly claim the name of computer, from single-chip microprocessors costing a few dollars to supercomputers costing tens of millions of dollars. Variety is exhibited not only in cost, but also in size, performance, and application. Second, the rapid pace of change that has always characterized computer technology continues with no letup. These changes cover all aspects of computer technology, from the underlying integrated circuit technology used to construct computer components, to the increasing use of parallel organization concepts in combining those components.

In spite of the variety and pace of change in the computer field, certain fundamental concepts apply consistently throughout. The application of these concepts depends on the current state of the technology and the price/performance objectives of the designer. The intent of this book is to provide a thorough discussion of the fundamentals of computer organization and architecture and to relate these to contemporary design issues.

The subtitle suggests the theme and the approach taken in this book. It has always been important to design computer systems to achieve high performance, but never has this requirement been stronger or more difficult to satisfy than today. All of the basic performance characteristics of computer systems, including processor speed, memory speed, memory capacity, and interconnection data rates, are increasing rapidly. Moreover, they are increasing at different rates. This makes it difficult to design a balanced system that maximizes the performance and utilization of all elements. Thus, computer design increasingly becomes a game of changing the structure or function in one area to compensate for a performance mismatch in another area. We will see this game played out in numerous design decisions throughout the book.

A computer system, like any system, consists of an interrelated set of components. The system is best characterized in terms of structure—the way in which components are interconnected, and function—the operation of the individual components. Furthermore, a computer's organization is hierarchical. Each major component can be further described by decomposing it into its major subcomponents and describing their structure and function. For clarity and ease of understanding, this hierarchical organization is described in this book from the top down:

- Computer system: Major components are processor, memory, I/O.
- Processor: Major components are control unit, registers, ALU, and instruction execution unit.
- **Control Unit:** Provides control signals for the operation and coordination of all processor components. Traditionally, a microprogramming implementation has been used, in which major components are control memory, microinstruction sequencing logic, and registers. More recently, microprogramming has been less prominent but remains an important implementation technique.

The objective is to present the material in a fashion that keeps new material in a clear context. This should minimize the chance that the reader will get lost and should provide better motivation than a bottom-up approach.

Throughout the discussion, aspects of the system are viewed from the points of view of both architecture (those attributes of a system visible to a machine language programmer) and organization (the operational units and their interconnections that realize the architecture).

EXAMPLE SYSTEMS

This text is intended to acquaint the reader with the design principles and implementation issues of contemporary operating systems. Accordingly, a purely conceptual or theoretical treatment would be inadequate. To illustrate the concepts and to tie them to real-world design choices that must be made, two processor families have been chosen as running examples:

- Intel x86 architecture: The x86 architecture is the most widely used for non-embedded computer systems. The x86 is essentially a complex instruction set computer (CISC) with some RISC features. Recent members of the x86 family make use of superscalar and multicore design principles. The evolution of features in the x86 architecture provides a unique case study of the evolution of most of the design principles in computer architecture.
- ARM: The ARM embedded architecture is arguably the most widely used embedded
 processor, used in cell phones, iPods, remote sensor equipment, and many other devices. The ARM is essentially a reduced instruction set computer (RISC). Recent
 members of the ARM family make use of superscalar and multicore design principles.

Many, but by no means all, of the examples are drawn from these two computer families: the Intel x86, and the ARM embedded processor family. Numerous other systems, both contemporary and historical, provide examples of important computer architecture design features.

PLAN OF THE TEXT

The book is organized into five parts (see Chapter 0 for an overview)

- Overview
- The computer system
- The central processing unit
- The control unit
- Parallel organization, including multicore

The book includes a number of pedagogic features, including the use of interactive simulations and numerous figures and tables to clarify the discussion. Each chapter includes a list of key words, review questions, homework problems, suggestions for further reading, and recommended Web sites. The book also includes an extensive glossary, a list of frequently used acronyms, and a bibliography.

INTENDED AUDIENCE

The book is intended for both an academic and a professional audience. As a textbook, it is intended as a one- or two-semester undergraduate course for computer science, computer engineering, and electrical engineering majors. It covers all the topics in *CS 220 Computer Architecture*, which is one of the core subject areas in the *IEEE/ACM Computer Curricula 2001*.

For the professional interested in this field, the book serves as a basic reference volume and is suitable for self-study.

INSTRUCTIONAL SUPPORT MATERIALS

To support instructors, the following materials are provided:

- Solutions manual: Solutions to end-of-chapter Review Questions and Problems
- Projects manual: Suggested project assignments for all of the project categories listed below
- PowerPoint slides: A set of slides covering all chapters, suitable for use in lecturing
- PDF files: Reproductions of all figures and tables from the book
- Test bank: Includes true/false, multiple choice, and fill-in-the-blanks questions and answers

All of these support materials are available at the Instructor Resource Center (IRC) for this textbook. To gain access to the IRC, please contact your local Prentice Hall sales representative via prenhall.com/replocator or call Prentice Hall Faculty Services at 1-800-526-0485. You can also locate the IRC through http://www.pearsonhighered.com/stallings.

INTERNET SERVICES FOR INSTRUCTORS AND STUDENTS

There is a Web site for this book that provides support for students and instructors. The site includes links to other relevant sites and a set of useful documents. See the section, "Web Site for Computer Organization and Architecture," preceding this Preface, for more information. The Web page is at williamstallings.com/COA/COA8e.html.

New to this edition is a set of homework problems with solutions publicly available at this Web site. Students can enhance their understanding of the material by working out the solutions to these problems and then checking their answers.

An Internet mailing list has been set up so that instructors using this book can exchange information, suggestions, and questions with each other and with the author. As soon as typos or other errors are discovered, an errata list for this book will be available at WilliamStallings.com. Finally, I maintain the Computer Science Student Resource Site at WilliamStallings.com/StudentSupport.html.

PROJECTS AND OTHER STUDENT EXERCISES

For many instructors, an important component of a computer organization and architecture course is a project or set of projects by which the student gets hands-on experience to reinforce concepts from the text. This book provides an unparalleled degree of support for including a projects component in the course. The instructor's support materials available through Prentice Hall not only includes guidance on how to assign and structure the projects but also includes a set of user's manuals for various project types plus specific assignments, all written especially for this book. Instructors can assign work in the following areas:

- Interactive simulation assignments: Described subsequently.
- **Research projects:** A series of research assignments that instruct the student to research a particular topic on the Internet and write a report.

- Simulation projects: The IRC provides support for the use of the two simulation packages: SimpleScalar can be used to explore computer organization and architecture design issues. SMPCache provides a powerful educational tool for examining cache design issues for symmetric multiprocessors.
- **Assembly language projects:** A simplified assembly language, CodeBlue, is used and assignments based on the popular Core Wars concept are provided.
- **Reading/report assignments:** A list of papers in the literature, one or more for each chapter, that can be assigned for the student to read and then write a short report.
- Writing assignments: A list of writing assignments to facilitate learning the material.
- Test bank: Includes T/F, multiple choice, and fill-in-the-blanks questions and answers.

This diverse set of projects and other student exercises enables the instructor to use the book as one component in a rich and varied learning experience and to tailor a course plan to meet the specific needs of the instructor and students. See Appendix A in this book for details.

INTERACTIVE SIMULATIONS

New to this edition is the incorporation of interactive simulations. These simulations provide a powerful tool for understanding the complex design features of a modern computer system. A total of 20 interactive simulations are used to illustrate key functions and algorithms in computer organization and architecture design. At the relevant point in the book, an icon indicates that a relevant interactive simulation is available online for student use. Because the animations enable the user to set initial conditions, they can serve as the basis for student assignments. The instructor's supplement includes a set of assignments, one for each of the animations. Each assignment includes a several specific problems that can be assigned to students.

WHAT'S NEW IN THE EIGHTH EDITION

In the four years since the seventh edition of this book was published, the field has seen continued innovations and improvements. In this new edition, I try to capture these changes while maintaining a broad and comprehensive coverage of the entire field. To begin this process of revision, the seventh edition of this book was extensively reviewed by a number of professors who teach the subject and by professionals working in the field. The result is that, in many places, the narrative has been clarified and tightened, and illustrations have been improved. Also, a number of new "field-tested" homework problems have been added.

Beyond these refinements to improve pedagogy and user friendliness, there have been substantive changes throughout the book. Roughly the same chapter organization has been retained, but much of the material has been revised and new material has been added. The most noteworthy changes are as follows:

• Interactive simulation: Simulation provides a powerful tool for understanding the complex mechanisms of a modern processor. The eighth edition incorporates 20 separate interactive, Web-based simulation tools covering such areas as cache memory, main memory, I/O, branch prediction, instruction pipelining, and vector processing. At appropriate places in the book, the simulators are highlighted so that the student can invoke the simulation at the proper point in studying the book.

- Embedded processors: The eighth edition now includes coverage of embedded processors and the unique design issues they present. The ARM architecture is used as a case study.
- Multicore processors: The eighth edition now includes coverage of what has become
 the most prevalent new development in computer architecture: the use of multiple
 processors on a single chip. Chapter 18 is devoted to this topic.
- Cache memory: Chapter 4, which is devoted to cache memory, has been extensively
 revised, updated, and expanded to provide broader technical coverage and improved pedagogy through the use of numerous figures, as well as interactive simulation tools.
- Performance assessment: Chapter 2 includes a significantly expanded discussion of performance assessment, including a new discussion of benchmarks and an analysis of Amdahl's law.
- Assembly language: A new appendix has been added that covers assembly language and assemblers.
- Programmable logic devices: The discussion of PLDs in Chapter 20 on digital logic has been expanded to include an introduction to field-programmable gate arrays (FPGAs).
- DDR SDRAM: DDR has become the dominant main memory technology in desktops and servers, particularly DDR2 and DDR3. DDR technology is covered in Chapter 5, with additional details in Appendix K.
- Linear tape open (LTO): LTO has become the best selling "super tape" format and is
 widely used with small and large computer systems, especially for backup, LTO is covered in Chapter 6, with additional details in Appendix J.

With each new edition it is a struggle to maintain a reasonable page count while adding new material. In part this objective is realized by eliminating obsolete material and tightening the narrative. For this edition, chapters and appendices that are of less general interest have been moved online, as individual PDF files. This has allowed an expansion of material without the corresponding increase in size and price.

ACKNOWLEDGEMENTS

This new edition has benefited from review by a number of people, who gave generously of their time and expertise. The following people reviewed all or a large part of the manuscript: Azad Azadmanesh (*University of Nebraska–Omaha*); Henry Casanova (*University of Hawaii*); Marge Coahran (*Grinnell College*); Andree Jacobsen (*University of New Mexico*); Kurtis Kredo (*University of California–Davis*); Jiang Li (*Austin Peay State University*); Rachid Manseur (*SUNY*, *Oswego*); John Masiyowski (*George Mason University*); Fuad Muztaba (*Winston-Salem State University*); Bill Sverdlik (*Eastern Michigan University*); and Xiaobo Zhou (*University of Colorado Colorado Springs*).

Thanks also to the people who provided detailed technical reviews of a single chapter: Tim Mensch, Balbir Singh, Michael Spratte (Hewlett-Packard), François-Xavier Peretmere, John Levine, Jeff Kenton, Glen Herrmannsfeldt, Robert Thorpe, Grzegorz Mazur (Institute of Computer Science, Warsaw University of Technology), Ian Ameline, Terje Mathisen, Edward Brekelbaum (Varilog Research Inc), Paul DeMone, and Mikael Tillenius. I would also like to thank Jon Marsh of ARM Limited for the review of the material on ARM.

xviii PREFACE

Professor Cindy Norris of Appalachian State University, Professor Bin Mu of the University of New Brunswick, and Professor Kenrick Mock of the University of Alaska kindly supplied homework problems.

Aswin Sreedhar of the University of Massachusetts developed the interactive simulation assignments and also wrote the test bank.

Professor Miguel Angel Vega Rodriguez, Professor Dr. Juan Manuel Sánchez Pérez, and Prof. Dr. Juan Antonio Gómez Pulido, all of University of Extremadura, Spain prepared the SMPCache problems in the instructors manual and authored the SMPCache User's Guide.

Todd Bezenek of the University of Wisconsin and James Stine of Lehigh University prepared the SimpleScalar problems in the instructor's manual, and Todd also authored the SimpleScalar User's Guide.

Thanks also to Adrian Pullin at Liverpool Hope University College, who developed the PowerPoint slides for the book.

Finally, I would like to thank the many people responsible for the publication of the book, all of whom did their usual excellent job. This includes my editor Tracy Dunkelberger, her assistant Melinda Haggerty, and production manager Rose Kernan. Also, Jake Warde of Warde Publishers managed the reviews; and Patricia M. Daly did the copy editing.

CONTENTS

Web	Site	for	the	Book	iv

About the Author xi

Preface xiii

Chapter 0 Re	ader's Guide 1
--------------	----------------

- 0.1 Outline of the Book 2
- 0.2 A Roadmap for Readers and Instructors 2
- 0.3 Why Study Computer Organization and Architecture 3
- 0.4 Internet and Web Resources 4

PART ONE OVERVIEW 7

Chapter 1 Introduction 8

- 1.1 Organization and Architecture 9
- 1.2 Structure and Function 10
- 1.3 Key Terms and Review Questions 15

Chapter 2 Computer Evolution and Performance 16

- 2.1 A Brief History of Computers 17
- 2.2 Designing for Performance 38
- 2.3 The Evolution of the Intel x86 Architecture 44
- 2.4 Embedded Systems and the ARM 46
- 2.5 Performance Assessment 50
- 2.6 Recommended Reading and Web Sites 57
- 2.7 Key Terms, Review Questions, and Problems 59

PART TWO THE COMPUTER SYSTEM 63

Chapter 3 A Top-Level View of Computer Function and Interconnection 65

- 3.1 Computer Components 66
- 3.2 Computer Function 68
- 3.3 Interconnection Structures 83
- 3.4 Bus Interconnection 85
- 3.5 PCI 95
- 3.6 Recommended Reading and Web Sites 104
- Key Terms, Review Questions, and Problems 104
 Appendix 3A Timing Diagrams 108

Chapter 4 Cache Memory 110

- 4.1 Computer Memory System Overview 111
- 4.2 Cache Memory Principles 118
- 4.3 Elements of Cache Design 121
- 4.4 Pentium 4 Cache Organization 140
- 4.5 ARM Cache Organization 143

vi CONTENTS

9.7

4.6	Recommended Reading 145
4.7	Key Terms, Review Questions, and Problems 146
	Appendix 4A Performance Characteristics of Two-Level Memories 151
Chapter 5	Internal Memory Technology 158
5.1	Semiconductor Main Memory 159
5.2	Error Correction 169
5.3	Advanced DRAM Organization 173
5.4	Recommended Reading and Web Sites 179
5.5	Key Terms, Review Questions, and Problems 180
Chapter 6	External Memory 184
6.1	Magnetic Disk 185
6.2	RAID 194
6.3	Optical Memory 203
6.4	Magnetic Tape 210
6.5	Recommended Reading and Web Sites 212
6.6	Key Terms, Review Questions, and Problems 214
Chapter 7	Input/Output 217
7.1	External Devices 219
7.2	I/O Modules 222
7.3	Programmed I/O 224
7.4	Interrupt-Driven I/O 228
7.5	Direct Memory Access 236
7.6	I/O Channels and Processors 242
7.7	The External Interface: FireWire and Infiniband 244
7.8	Recommended Reading and Web Sites 253
7.9	Key Terms, Review Questions, and Problems 254
Chapter 8	Operating System Support 259
8.1	Operating System Overview 260
8.2	Scheduling 271
8.3	Memory Management 277
8.4 8.5	Pentium Memory Management 288
8.6	ARM Memory Management 293 Precommended Precipitation and Web Sites 208
8.7	Recommended Reading and Web Sites 298 Key Terms, Review Questions, and Problems 299
0.7	Rey Terms, Neview Questions, and Problems 277
PART THE	DEE THE CENTRAL PROCESSING HART 202
Chapter 9	REE THE CENTRAL PROCESSING UNIT 303 Computer Arithmetic 305
•	
9.1	The Arithmetic and Logic Unit (ALU) 306
9.2 9.3	Integer Representation 307 Integer Arithmetic 312
9.4	Floating-Point Representation 327
9.5	Floating-Point Arithmetic 334
9.6	Recommended Reading and Web Sites 342
	- coommended reading and web sites 372

Key Terms, Review Questions, and Problems 344

Chapter 10	Instruction Sets: Characteristics and Functions 348
10.1	Machine Instruction Characteristics 349
10.2	Types of Operands 356
10.3	Intel x86 and ARM Data Types 358
10.4	Types of Operations 362
10.5	Intel x86 and ARM Operation Types 374
10.6	Recommended Reading 384
10.7	Key Terms, Review Questions, and Problems 385
	Appendix 10A Stacks 390
	Appendix 10B Little, Big, and Bi-Endian 396
Chapter 11	Instruction Sets: Addressing Modes and Formats 400
11.1	Addressing 401
11.2	x86 and ARM Addressing Modes 408
11.3	Instruction Formats 413
11.4	x86 and ARM Instruction Formats 421
11.5	Assembly Language 426
11.6	Recommended Reading 428
11.7	Key Terms, Review Questions, and Problems 428
Chapter 12	Processor Structure and Function 432
12.1	Processor Organization 433
12.2	Register Organization 435
12.3	The Instruction Cycle 440
12.4	Instruction Pipelining 444
12.5	The x86 Processor Family 461
12.6	The ARM Processor 469
12.7	Recommended Reading 475
12.8	Key Terms, Review Questions, and Problems 476
Chapter 13	Reduced Instruction Set Computers (RISCs) 480
13.1	Instruction Execution Characteristics 482
13.2	The Use of a Large Register File 487
13.3	Compiler-Based Register Optimization 492
13.4	Reduced Instruction Set Architecture 494
13.5	RISC Pipelining 500
13.6	MIPS R4000 504
13.7	SPARC 511
13.8	The RISC versus CISC Controversy 517
13.9 13.10	Recommended Reading 518 Voy Torms Proving Operations and Broblems 518
	Key Terms, Review Questions, and Problems 518
	Instruction-Level Parallelism and Superscalar Processors 522
14.1	Overview 524
14.2	Design Issues 528
14.3	Pentium 4 538
14.4 14.5	ARM Cortex-A8 544 P. ecomponded P. ending 552
14.5	Recommended Reading 552 Key Terms, Review Questions, and Problems 554

viii CONTENTS

PART FOUR	THE CONTROL	UNIT 559	9

Chapter	15	Control	Unit	Operation	561

- 15.1 Micro-operations 563
- 15.2 Control of the Processor 569
- 15.3 Hardwired Implementation 581
- 15.4 Recommended Reading 584
- 15.5 Key Terms, Review Questions, and Problems 584

Chapter 16 Microprogrammed Control 586

- 16.1 Basic Concepts 587
- 16.2 Microinstruction Sequencing 596
- 16.3 Microinstruction Execution 602
- 16.4 TI 8800 614
- 16.5 Recommended Reading 624
- 16.6 Key Terms, Review Questions, and Problems 625

PART FIVE PARALLEL ORGANIZATION 627

Chapter 17 Parallel Processing 628

- 17.1 The Use of Multiple Processors 630
- 17.2 Symmetric Multiprocessors 632
- 17.3 Cache Coherence and the MESI Protocol 640
- 17.4 Multithreading and Chip Multiprocessors 646
- 17.5 Clusters 653
- 17.6 Nonuniform Memory Access Computers 660
- 17.7 Vector Computation 664
- 17.8 Recommended Reading and Web Sites 676
- 17.9 Key Terms, Review Questions, and Problems 677

Chapter 18 Multicore Computers 684

- 18.1 HardwarePerformance Issues 685
- 18.2 Software Performance Issues 690
- 18.3 Multicore Organization 694
- 18.4 Intel x86 Multicore Organization 696
- 18.5 ARM11 MPCore 699
- 18.6 Recommended Reading and Web Sites 704
- 18.7 Key Terms, Review Questions, and Problems 705

Appendix A Projects for Teaching Computer Organization and Architecture 707

- A.1 Interactive Simulations 708
- A.2 Research Projects 708
- A.3 Simulation Projects 710
- A.4 Assembly Language Projects 711
- A.5 Reading/Report Assignments 711
- A.6 Writing Assignments 712
- A.7 Test Bank 712

Appendix B	Assembly Language and Related Topics 713		
B.1	Assembly Language 714		
B.2	Assemblers 723		
B.3	Loading and Linking 728		
B.4	Recommended Reading and Web Sites 735		
B.5	Key Terms, Review Questions, and Problems 736		
	ONLINE CHAPTERS		
	WilliamStallings.com/COA/COA8e.html		
Chapter 19	Number Systems 19-1		
19.1	The Decimal System 19-2		
	The Binary System 19-2		
	Converting between Binary and Decimal 19-3		
19.4	Hexadecimal Notation 19-5		
19.5	Key Terms, Review Questions, and Problems 19-8		
Chapter 20	Digital Logic 20-1		
20.1	Boolean Algebra 20-2		
	Gates 20-4		
20.3	Combinational Circuits 20-7		
20.4	Sequential Circuits 20–24		
20.5	Programmable Logic Devices 20-33		
20.6	Recommended Reading and Web Site 20-38		
20.7	Key Terms and Problems 20-39		
Chapter 21	The IA-64 Architecture 21-1		
21.1	Motivation 21-3		
	General Organization 21-4		
	Predication, Speculation, and Software Pipelining 21-6		
	IA-64 Instruction Set Architecture 21-23		
21.5	Itanium Organization 21-28		
21.6	Recommended Reading and Web Sites 21-31		
21.7	Key Terms, Review Questions, and Problems 21-32		
	ONLINE APPENDICES		
	WilliamStallings.com/COA/COA8e.html		
Appendix C	Hash Tables		
Appendix D	Victim Cache Strategies		
	Victim Cache		
	Selective Victim Cache		
Appendix E	Interleaved Memory		
Appendix F	International Reference Alphabet		
Appendix G	Virtual Memory Page Replacement Algorithms		

此为试读,需要完整PDF请访问: www.ertongbook.com