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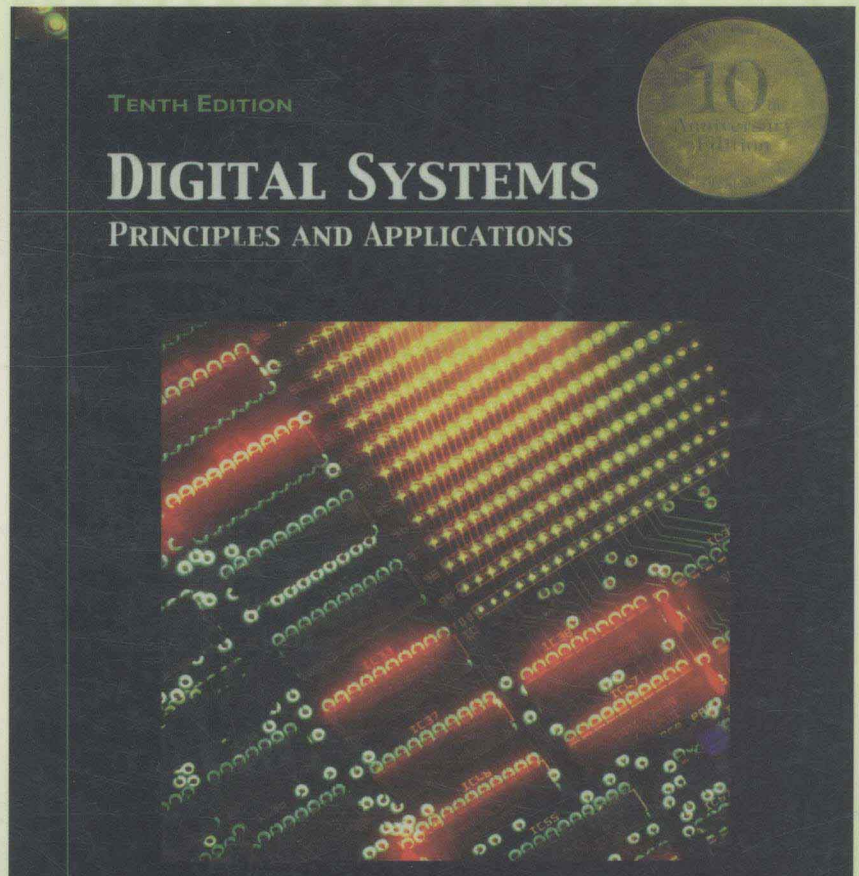
数字系统原理与应用

（英文版 · 第10版）



附赠光盘

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机械工业出版社
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Digital Systems
Principles and Applications
(Tenth Edition)

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PREFACE

This book is a comprehensive study of the principles and techniques of modern digital systems. It teaches the fundamental principles of digital systems and covers thoroughly both traditional and modern methods of applying digital design and development techniques, including how to manage a systems-level project. The book is intended for use in two- and four-year programs in technology, engineering, and computer science. Although a background in basic electronics is helpful, most of the material requires no electronics training. Portions of the text that use electronics concepts can be skipped without adversely affecting the comprehension of the logic principles.

General Improvements

The tenth edition of *Digital Systems* reflects the authors' views of the direction of modern digital electronics. In industry today, we see the importance of getting a product to market very quickly. The use of modern design tools, CPLDs, and FPGAs allows engineers to progress from concept to functional silicon very quickly. Microcontrollers have taken over many applications that once were implemented by digital circuits, and DSP has been used to replace many analog circuits. It is amazing that microcontrollers, DSP, and all the necessary glue logic can now be consolidated onto a single FPGA using a hardware description language with advanced development tools. Today's students must be exposed to these modern tools, even in an introductory course. It is every educator's responsibility to find the best way to prepare graduates for the work they will encounter in their professional lives.

The standard SSI and MSI parts that have served as "bricks and mortar" in the building of digital systems for nearly 40 years are now nearing obsolescence. Many of the techniques that have been taught over that time have focused on optimizing circuits that are built from these outmoded devices. The topics that are uniquely suited to applying the old technology *but do not contribute to an understanding of the new technology* must be removed from

the curriculum. From an educational standpoint, however, these small ICs do offer a way to study simple digital circuits, and the wiring of circuits using breadboards is a valuable pedagogic exercise. They help to solidify concepts such as binary inputs and outputs, physical device operation, and practical limitations, using a very simple platform. Consequently, we have chosen to continue to introduce the conceptual descriptions of digital circuits and to offer examples using conventional standard logic parts. For instructors who continue to teach the fundamentals using SSI and MSI circuits, this edition retains those qualities that have made the text so widely accepted in the past. Many hardware design tools even provide an easy-to-use design entry technique that will employ the functionality of conventional standard parts with the flexibility of programmable logic devices. A digital design can be described using a schematic drawing with pre-created building blocks that are equivalent to conventional standard parts, which can be compiled and then programmed directly into a target PLD with the added capability of easily simulating the design within the same development tool.

We believe that graduates will actually apply the concepts presented in this book using higher-level description methods and more complex programmable devices. The major shift in the field is a greater need to understand the description methods, rather than focusing on the architecture of an actual device. Software tools have evolved to the point where there is little need for concern about the inner workings of the hardware but much more need to focus on what goes in, what comes out, and how the designer can describe what the device is supposed to do. We also believe that graduates will be involved with projects using state-of-the-art design tools and hardware solutions.

This book offers a strategic advantage for teaching the vital new topic of hardware description languages to beginners in the digital field. VHDL is undisputedly an industry standard language at this time, but it is also very complex and has a steep learning curve. Beginning students are often discouraged by the rigorous requirements of various data types, and they struggle with understanding edge-triggered events in VHDL. Fortunately, Altera offers AHDL, a less demanding language that uses the same basic concepts as VHDL but is much easier for beginners to master. So, instructors can opt to use AHDL to teach introductory students or VHDL for more advanced classes. This edition offers more than 40 AHDL examples, more than 40 VHDL examples, and many examples of simulation testing. All of these design files are available on the enclosed CD-ROM.

Altera's latest software development system is Quartus II. The MAX+PLUS II software that has been used for many years is still popular in industry and is supported by Altera. Its main drawback is that it does not program the latest devices. The material in this text does not attempt to teach a particular hardware platform or the details of using a software development system. New revisions of software tools appear so frequently that a textbook cannot remain current if it tries to describe all of the details. We have tried to show what this tool can do, rather than train the reader how to use it. However, tutorials have been included on the accompanying CD-ROM that make it easy to learn either software package. The AHDL and VHDL examples are compatible with either Quartus or MAX+PLUS systems. The timing simulations were developed using MAX+PLUS but can also be done with Quartus.

Many laboratory hardware options are available to users of this book. A number of CPLD and FPGA development boards are available for students to use in the laboratory. There are several earlier generation boards similar to Altera's UP2 that contain MAX7000 family CPLDs. A more recent example of an available board is the UP3 board from Altera's university program (see Figure P-1), which contains a larger FPGA from the Cyclone family. An even

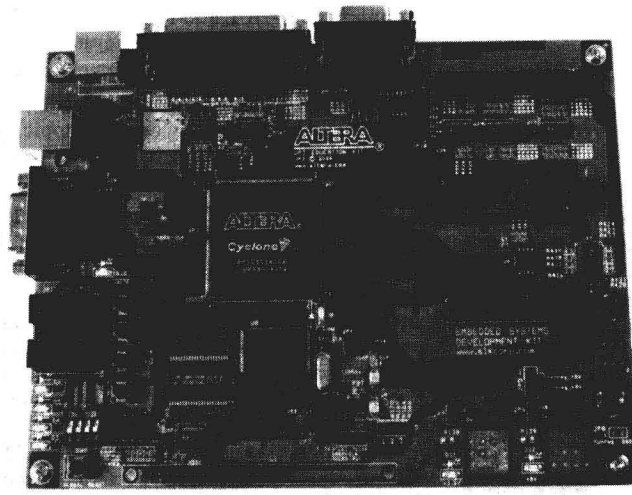


FIGURE P-1 Altera's UP3 development board.

newer board from Altera is called the DE2 board (see Figure P-2), which has a powerful new 672-pin Cyclone II FPGA and a number of basic features such as switches, LEDs, and displays as well as many additional features for more advanced projects. More development boards are entering the market every year, and many are becoming very affordable. These boards, along with powerful educational software, offer an excellent way to teach and demonstrate the practical implementation of the concepts presented in this text.

The most significant improvements in the tenth edition are found in Chapter 7. Although asynchronous (ripple) counters provide a good introduction to sequential circuits, the real world uses synchronous counter circuits. Chapter 7 and subsequent examples have been rewritten to emphasize synchronous counter ICs and include techniques for analysis, cascading, and using HDL to describe them. A section has also been added to improve the coverage of state machines and the HDL features used to describe them. Other improvements include analysis techniques for combinational circuits, expanded coverage of 555 timer applications, and better coverage of signed binary numbers.

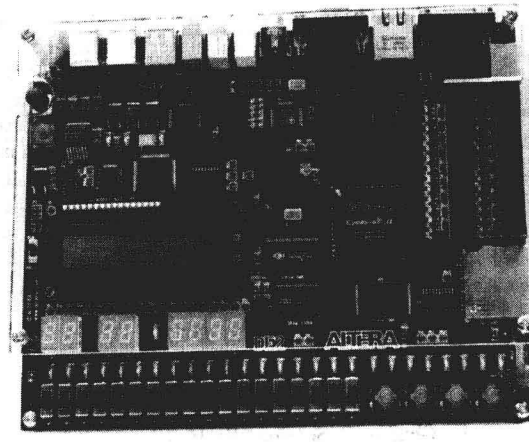


FIGURE P-2 Altera's DE2 development board.

Our approach to HDL and PLDs gives instructors several options:

1. The HDL material can be skipped entirely without affecting the continuity of the text.
2. HDL can be taught as a separate topic by skipping the material initially and then going back to the last sections of Chapters 3, 4, 5, 6, 7, and 9 and then covering Chapter 10.
3. HDL and the use of PLDs can be covered as the course unfolds—chapter by chapter—and woven into the fabric of the lecture/lab experience.

Among all specific hardware description languages, VHDL is clearly the industry standard and is most likely to be used by graduates in their careers. We have always felt that it is a bold proposition, however, to try to teach VHDL in an introductory course. The nature of the syntax, the subtle distinctions in object types, and the higher levels of abstraction can pose obstacles for a beginner. For this reason, we have included Altera's AHDL as the recommended introductory language for freshman courses. We have also included VHDL as the recommended language for more advanced classes or introductory courses offered to more mature students. We do not recommend trying to cover both languages in the same course. Sections of the text that cover the specifics of a language are clearly designated with a color bar in the margin. The HDL code figures are set in a color to match the color-coded text explanation. The reader can focus only on the language of his or her choice and skip the other. Obviously, we have attempted to appeal to the diverse interests of our market, but we believe we have created a book that can be used in multiple courses and will serve as an excellent reference after graduation.

Chapter Organization

It is a rare instructor who uses the chapters of a textbook in the sequence in which they are presented. This book was written so that, for the most part, each chapter builds on previous material, but it is possible to alter the chapter sequence somewhat. The first part of Chapter 6 (arithmetic operations) can be covered right after Chapter 2 (number systems), although this will lead to a long interval before the arithmetic circuits of Chapter 6 are encountered. Much of the material in Chapter 8 (IC characteristics) can be covered earlier (e.g., after Chapter 4 or 5) without creating any serious problems.

This book can be used either in a one-term course or in a two-term sequence. In a one-term course, limits on available class hours might require omitting some topics. Obviously, the choice of deletions will depend on factors such as program or course objectives and student background. A list of sections and chapters that can be deleted with minimal disruption follows:

- Chapter 1: All
- Chapter 2: Section 6
- Chapter 3: Sections 15–20
- Chapter 4: Sections 7, 10–13
- Chapter 5: Sections 3, 23–27
- Chapter 6: Sections 5–7, 11, 13, 16–23
- Chapter 7: Sections 9–14, 21–24
- Chapter 8: Sections 10, 14–19

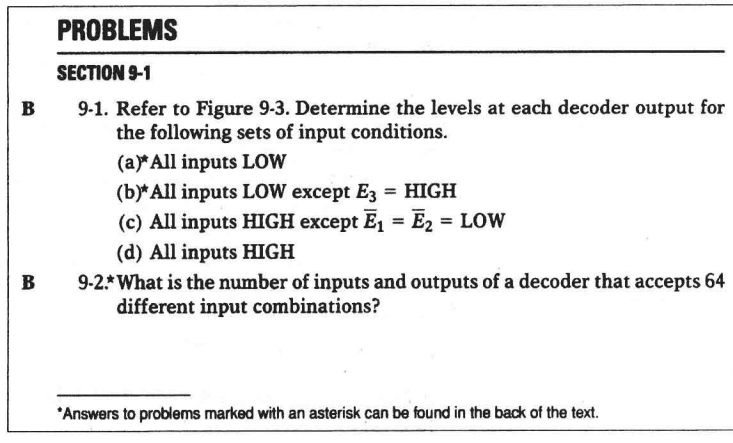
- Chapter 9: Sections 5, 9, 15–20
- Chapter 10: All
- Chapter 11: Sections 7, 14–17
- Chapter 12: Sections 17–21
- Chapter 13: All

PROBLEM SETS This edition includes six categories of problems: basic (B), challenging (C), troubleshooting (T), new (N), design (D), and HDL (H). Undesignated problems are considered to be of intermediate difficulty, between basic and challenging. Problems for which solutions are printed in the back of the text or on the enclosed CD-ROM are marked with an asterisk (see Figure P-3).

PROJECT MANAGEMENT AND SYSTEM-LEVEL DESIGN Several real-world examples are included in Chapter 10 to describe the techniques used to manage projects. These applications are generally familiar to most students studying electronics, and the primary example of a digital clock is familiar to everyone. Many texts talk about top-down design, but this text demonstrates the key features of this approach and how to use the modern tools to accomplish it.

DATA SHEETS The CD-ROM containing Texas Instruments data sheets that accompanied the ninth edition has been removed. The information that was included on this CD-ROM is now readily available online.

SIMULATION FILES This edition also includes simulation files that can be loaded into Electronics Workbench Multisim®. The circuit schematics of many of the figures throughout the text have been captured as input files for this popular simulation tool. Each file has some way of demonstrating the operation of the circuit or reinforcing a concept. In many cases, instruments are attached to the circuit and input sequences are applied to demonstrate the concept presented in one of the figures of the text. These circuits can then be modified as desired to expand on topics or create assignments and tutorials



PROBLEMS

SECTION 9-1

B 9-1. Refer to Figure 9-3. Determine the levels at each decoder output for the following sets of input conditions.

(a)* All inputs LOW

(b)* All inputs LOW except E_3 = HIGH

(c) All inputs HIGH except $\overline{E}_1 = \overline{E}_2$ = LOW

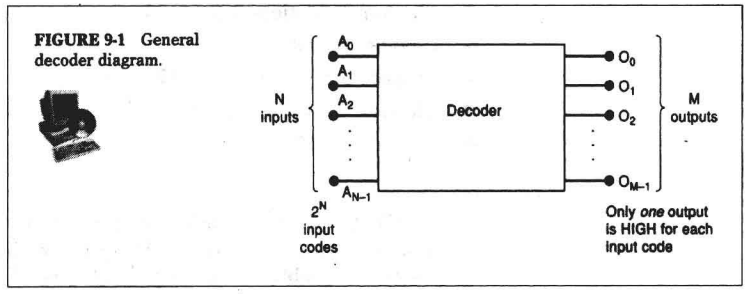
(d) All inputs HIGH

B 9-2.* What is the number of inputs and outputs of a decoder that accepts 64 different input combinations?

*Answers to problems marked with an asterisk can be found in the back of the text.

FIGURE P-3 Letters denote categories of problems, and asterisks indicate that corresponding solutions are provided at the end of the text.

FIGURE P-4 The icon denotes a corresponding simulation file on the CD-ROM.



for students. All figures in the text that have a corresponding simulation file on the CD-ROM are identified by the icon shown in Figure P-4.

IC TECHNOLOGY This new edition continues the practice begun with the last three editions of giving more prominence to CMOS as the principal IC technology in small- and medium-scale integration applications. This depth of coverage has been accomplished while retaining the substantial coverage of TTL logic.

Specific Changes

The major changes in the topical coverage are listed here.

- **Chapter 1.** Many explanations covering digital/analog issues have been updated and improved.
- **Chapter 2.** The octal number system has been removed and the Gray code has been added. A complete standard ASCII code table has been included, along with new examples that relate ASCII characters, hex representation, and computer object code transfer files. New material on framing ASCII characters for asynchronous data transfer has also been added.
- **Chapter 3.** Along with some new practical examples of logic functions, the major improvement in Chapter 3 is a new analysis technique using tables that evaluate intermediate points in the logic circuit.
- **Chapter 4.** Very few changes were necessary in Chapter 4.
- **Chapter 5.** A new section covers digital pulses and associated definitions such as pulse width, period, rise time, and fall time. The terminology used for latch circuit inputs has been changed from Clear to Reset in order to be compatible with Altera component descriptions. The definition of a master/slave flip-flop has been removed as well. The discussion of Schmitt trigger applications has been improved to emphasize their role in eliminating the effects of noise. The inner workings of the 555 timer are now explained, and some improved timing circuits are proposed that make the device more versatile. The HDL coverage of SR and D latches has been rewritten to use a more intuitive behavioral description, and the coverage of counters has been modified to focus on structural techniques to interconnect flip-flop blocks.
- **Chapter 6.** Signed numbers are covered in more detail in this edition, particularly regarding sign extension in 2's complement numbers and arithmetic overflow. A new calculator hint simplifies negation of binary numbers represented in hex. A number circle model is used to compare

signed and unsigned number formats and help students to visualize add/subtract operation using both.

- **Chapter 7.** This chapter has been heavily revised to emphasize synchronous counter circuits. Simple ripple counters are still introduced to provide a basic understanding of the concept of counting and asynchronous cascading. After examining the limitations of ripple counters in Section 2, synchronous counters are introduced in Section 3 and used in all subsequent examples throughout the text. The IC counters presented are the 74160, '161, '162, and '163. These common devices offer an excellent assortment of features that teach the difference between synchronous and asynchronous control inputs and cascading techniques. The 74190 and '191 are used as an example of a synchronous up/down counter IC, further reinforcing the techniques required for synchronous cascading. A new section is devoted to analysis techniques for synchronous circuits using JK and D flip-flops. Synchronous design techniques now also include the use of D flip-flop registers that best represent the way sequential circuits are implemented in modern PLD technology. The HDL sections have been improved to demonstrate the implementation of synchronous/asynchronous loading, clearing, and cascading. A new emphasis is placed on simulation and testing of HDL modules. State machines are now presented as a topic, the traditional Mealy and Moore models are defined, and a new traffic light control system is presented as an example. Minor improvements have been made in the second half of Chapter 7 also. All of the problems at the end of Chapter 7 have been rewritten to reinforce the concepts.
- **Chapter 8.** This chapter remains a very technical description of the technology available in standard logic families and digital components. The mixed-voltage interfacing sections have been improved to cover low-voltage technology. The latest Texas Instruments life-cycle curve shows the history and current position of various logic series between introduction and obsolescence. Low-voltage differential signaling (LVDS) is introduced as well.
- **Chapter 9.** The many different building blocks of digital systems are still covered in this chapter and demonstrated using HDL. Many other HDL techniques, such as tristate outputs and various HDL control structures, are also introduced. A 74ALS148 is described as another example of an encoder. The examples of systems that use counters have all been updated to synchronous operation. The serial transmission system using MUX and DEMUX is particularly improved. The technique of using a MUX to implement SOP expressions has been explained in a more structured way as an independent study exercise in the end-of-the-chapter problems.
- **Chapter 10.** Chapter 10, which was new to the ninth edition, has remained essentially unchanged.
- **Chapter 11.** The material on bipolar DACs has been improved, and an example of using DACs as a digital amplitude control for analog waveforms is presented. The more common A/D converter accuracy specification in the form of +/− LSB is explained in this edition.
- **Chapter 12.** Minor improvements were made to this chapter to consolidate and compress some of the material on older technologies of memory such as UV EPROM. Flash technology is still introduced using a first-generation example, but the more recent improvements, as well as some of the applications of flash technology in modern consumer devices, are described.
- **Chapter 13.** This chapter, which was new to the ninth edition, has been updated to introduce the new Cyclone family of PLDs.

Retained Features

This edition retains all of the features that made the previous editions so widely accepted. It utilizes a block diagram approach to teach the basic logic operations without confusing the reader with the details of internal operation. All but the most basic electrical characteristics of the logic ICs are withheld until the reader has a firm understanding of logic principles. In Chapter 8, the reader is introduced to the internal IC circuitry. At that point, the reader can interpret a logic block's input and output characteristics and "fit" it properly into a complete system.

The treatment of each new topic or device typically follows these steps: the principle of operation is introduced; thoroughly explained examples and applications are presented, often using actual ICs; short review questions are posed at the end of the section; and finally, in-depth problems are available at the end of the chapter. These problems, ranging from simple to complex, provide instructors with a wide choice of student assignments. These problems are often intended to reinforce the material without simply repeating the principles. They require students to demonstrate comprehension of the principles by applying them to different situations. This approach also helps students to develop confidence and expand their knowledge of the material.

The material on PLDs and HDLs is distributed throughout the text, with examples that emphasize key features in each application. These topics appear at the end of each chapter, making it easy to relate each topic to the general discussion earlier in the chapter or to address the general discussion separately from the PLD/HDL coverage.

The extensive troubleshooting coverage is spread over Chapters 4 through 12 and includes presentation of troubleshooting principles and techniques, case studies, 25 troubleshooting examples, and 60 *real* troubleshooting problems. When supplemented with hands-on lab exercises, this material can help foster the development of good troubleshooting skills.

The tenth edition offers more than 200 worked-out examples, more than 400 review questions, and more than 450 chapter problems/exercises. Some of these problems are applications that show how the logic devices presented in the chapter are used in a typical microcomputer system. Answers to a majority of the problems immediately follow the Glossary. The Glossary provides concise definitions of all terms in the text that have been highlighted in boldface type.

An IC index is provided at the back of the book to help readers locate easily material on any IC cited or used in the text. The back endsheets provide tables of the most often used Boolean algebra theorems, logic gate summaries, and flip-flop truth tables for quick reference when doing problems or working in the lab.

Supplements

An extensive complement of teaching and learning tools has been developed to accompany this textbook. Each component provides a unique function, and each can be used independently or in conjunction with the others.

CD-ROM A CD-ROM is packaged with each copy of the text. It contains the following material:

- **MAX+PLUS® II Educational Version software from Altera.** This is a fully functional, professional-quality, integrated development environment for

digital systems that has been used for many years and is still supported by Altera. Students can use it to write, compile, and simulate their designs at home before going to the lab. They can use the same software to program and test an Altera CPLD.

- **Quartus II Web Version software from Altera.** This is the latest development system software from Altera, which offers more advanced features and supports new PLD devices such as the Cyclone family of FPGAs, found on many of the newest educational boards.
- **Tutorials.** Gregory Moss has developed tutorials that have been used successfully for several years to teach introductory students how to use Altera MAX+PLUS II software. These tutorials are available in PDF and PPT (Microsoft® PowerPoint® presentation) formats and have been adapted to teach Quartus II as well. With the help of these tutorials, anyone can learn to modify and test all the examples presented in this text, as well as develop his or her own designs.
- **Design files from the textbook figures.** More than 40 design files in each language are presented in figures throughout the text. Students can load these into the Altera software and test them.
- **Solutions to selected problems: HDL design files.** A few of the end-of-chapter problem solutions are available to students. (All of the HDL solutions are available to instructors in the *Instructor's Resource Manual.)* Solutions for Chapter 7 problems include some large graphic and HDL files that are not published in the back of the book but are available on the enclosed CD-ROM.
- **Circuits from the text rendered in Multisim®.** Students can open and work interactively with approximately 100 circuits to increase their understanding of concepts and prepare for laboratory activities. The Multisim circuit files are provided for use by anyone who has Multisim software. Anyone who does not have Multisim software and wishes to purchase it in order to use the circuit files may do so by ordering it from www.prenhall.com/ewb.
- **Supplemental material introducing microprocessors and microcontrollers.** For the flexibility to serve the diverse needs of the many different schools, an introduction to this topic is presented as a convenient bridge between a digital systems course and an introduction to microprocessors/microcontrollers course.

STUDENT RESOURCES

- ***Lab Manual: A Design Approach.*** This lab manual, written by Gregory Moss, contains topical units with lab projects that emphasize simulation and design. It utilizes the Altera MAX+PLUS II or Quartus II software in its programmable logic exercises and features both schematic capture and hardware description language techniques. The new edition contains many new projects and examples. (ISBN 0-13-188138-8)
- ***Lab Manual: A Troubleshooting Approach.*** This manual, written by Jim DeLoach and Frank Ambrosio, is presented with an analysis and troubleshooting approach and is fully updated for this edition of the text. (ISBN 0-13-188136-1)
- **Companion Website (www.prenhall.com/tocci).** This site offers students a free online study guide with which they can review the material learned in the text and check their understanding of key topics.

INSTRUCTOR RESOURCES

- ***Instructor's Resource Manual.*** This manual contains worked-out solutions for all end-of-chapter problems in this textbook. (ISBN 0-13-172665-X)
- ***Lab Solutions Manual.*** Worked-out lab results for both lab manuals are featured in this manual. (ISBN 0-13-172664-1)
- **PowerPoint® presentations.** Figures from the text, in addition to Lecture Notes for each chapter, are available on CD-ROM. (ISBN 0-13-172667-6)
- **TestGen.** A computerized test bank is available on CD-ROM. (ISBN 0-13-172666-8)

To access supplementary materials online, instructors need to request an instructor access code. Go to **www.prenhall.com,** click the **Instructor Resource Center** link, and then click **Register Today** for an instructor access code. Within 48 hours after registering, you will receive a confirming e-mail including an instructor access code. When you have received your code, go to the site and log on for full instructions on downloading the materials you wish to use.

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We also are greatly indebted to Professor Frank Ambrosio, Monroe Community College, for his usual high-quality work on the indexes and the *Instructor's Resource Manual;* and Professor Thomas L. Robertson, Purdue University, for providing his magnetic levitation system as an example; and Professors Russ Aubrey and Gene Harding, Purdue University, for their technical review of topics and many suggestions for improvements. We appreciate the cooperation of Mike Phipps and the Altera Corporation for their support in granting permission to use their software package and their figures from technical publications.

A writing project of this magnitude requires conscientious and professional editorial support, and Prentice Hall came through again in typical fashion. We thank the staffs at Prentice Hall and TechBooks/GTS for their help to make this publication a success.

And finally, we want to let our wives and our children know how much we appreciate their support and their understanding. We hope that we can eventually make up for all the hours we spent away from them while we worked on this revision.

Ronald J. Tocci
Neal S. Widmer
Gregory L. Moss

BOOLEAN THEOREMS

1. $x \cdot 0 = 0$
2. $x \cdot 1 = x$
3. $x \cdot x = x$
4. $x \cdot \bar{x} = 0$
5. $x + 0 = x$
6. $x + 1 = 1$
7. $x + x = x$
8. $x + \bar{x} = 1$
9. $x + y = y + x$
10. $x \cdot y = y \cdot x$
11. $x + (y + z) = (x + y) + z = x + y + z$
12. $x(yz) = (xy)z = xyz$

13a. $x(y + z) = xy + xz$

13b. $(w + x)(y + z) = wy + xy + wz + xz$

14. $x + xy = x$

15a. $x + \bar{x}y = x + y$

15b. $\bar{x} + xy = \bar{x} + y$

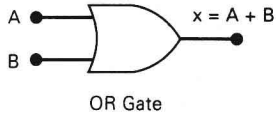
16. $\overline{x + y} = \bar{x}\,\bar{y}$

17. $\overline{xy} = \bar{x} + \bar{y}$

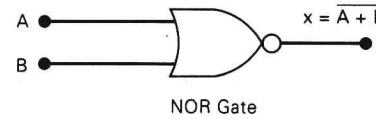
LOGIC GATE TRUTH TABLES

A	B	OR $A+B$	NOR $\overline{A+B}$	AND $A \cdot B$	NAND $\overline{A \cdot B}$	XOR $A \oplus B$	XNOR $\overline{A \oplus B}$
0	0	0	1	0	1	0	1
0	1	1	0	0	1	1	0
1	0	1	0	0	1	1	0
1	1	1	0	1	0	0	1

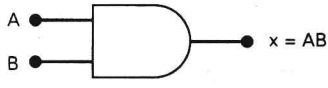
LOGIC GATE SYMBOLS



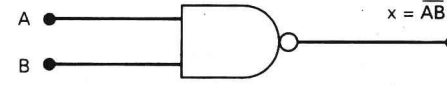
OR Gate



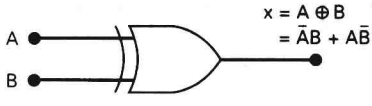
NOR Gate



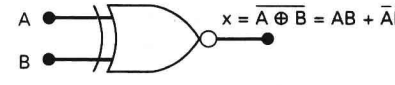
AND Gate



NAND Gate



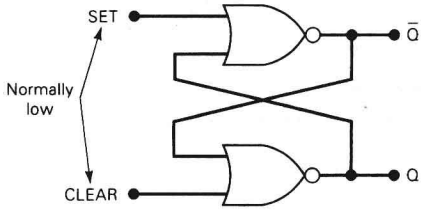
XOR

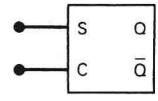


XNOR

FLIP-FLOPS

NOR Latch

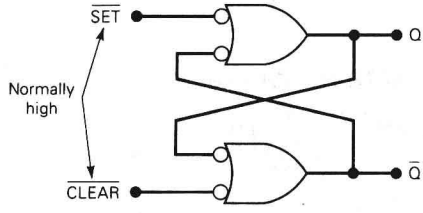


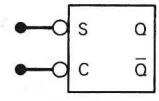


(Alternate symbol)

S	C	Q
0	0	No change
1	0	Q = 1
0	1	Q = 0
1	1	Invalid

NAND Latch

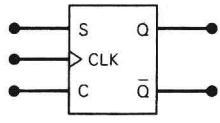




(Alternate symbol)

S	C	Q
0	0	Invalid
1	0	Q = 0
0	1	Q = 1
1	1	No change

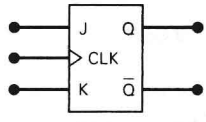
Clocked S-C



S	C	CLK	Q
0	0	↑	Q_0 (no change)
1	0	↑	1
0	1	↑	0
1	1	↑	Ambiguous

↓ of CLK has no effect on Q

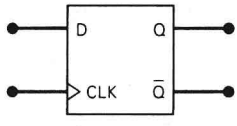
Clocked J-K



J	K	CLK	Q
0	0	↑	Q_0 (no change)
1	0	↑	1
0	1	↑	0
1	1	↑	$\overline{Q_0}$ (toggles)

↓ of CLK has no effect on Q

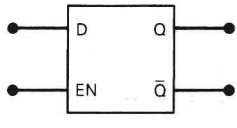
Clocked D



D	CLK	Q
0	↑	0
1	↑	1

↓ of CLK has no effect on Q

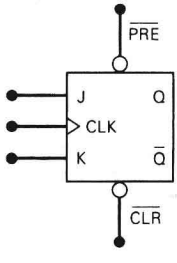
D Latch



EN	D	Q*
0	X	No change
1	0	0
1	1	1

*Q follows D input while EN is HIGH

Asynchronous Inputs



$\overline{PRE}$	$\overline{CLR}$	Q*
1	1	No effect; FF can respond to J, K and CLK
1	0	Q = 0 independent of J, K, CLK
0	1	Q = 1 independent of J, K, CLK
0	0	Ambiguous (not used)

*CLK can be in any state

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