

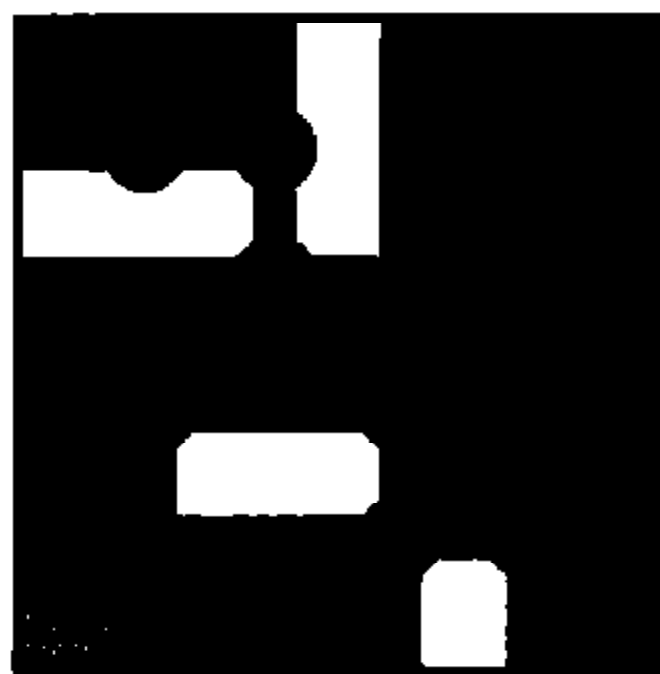
**Fundamentals of**  
**Logic Design**  
**Fourth Edition**

**Charles H. Roth, Jr.**



■ F O U R T H E D I T I O N

# Fundamentals of Logic Design



**CHARLES H. ROTH, JR.** \_\_\_\_\_

University of Texas at Austin



**PWS Publishing Company**

**I T P** An International Thomson Publishing Company

Boston • Albany • Bonn • Cincinnati • Detroit • London • Madrid • Melbourne • Mexico City  
New York • Pacific Grove • Paris • San Francisco • Singapore • Tokyo • Toronto • Washington



**PWS PUBLISHING COMPANY**  
20 Park Plaza, Boston, MA 02116-4324

---

Copyright © 1995 by PWS Publishing Company,  
a division of International Thomson Publishing, Inc.

Copyright © 1975, 1979, 1985, 1992 by West Publishing  
Company.

**All rights reserved.** No part of this book may be repro-  
duced, stored in a retrieval system, or transcribed in any  
form or by any means – electronic, mechanical, photo-  
copying, recording, or otherwise – without the prior  
written permission of PWS Publishing Company.

**ITP**

International Thomson Publishing  
The trademark ITP is used under license.

**For more information, contact:**  
**PWS Publishing Company**  
20 Park Plaza  
Boston, MA 02116

International Thomson Publishing Europe  
Berkshire House 168-173  
High Holborn  
London WC1V 7AA  
England

Thomas Nelson Australia  
102 Dodds Street  
South Melbourne, 3205  
Victoria, Australia

Nelson Canada  
1120 Birchmont Road  
Scarborough, Ontario  
Canada M1K 5G4

Sponsoring Editor: *Bill Barter*

Marketing Manager: *Nathan Wilbur*

Manufacturing Buyer: *Andrew Christensen*

Production Editor: *Pamela Rockwell*

Cover Designer: *Christine C. Bentley & Edward M. Rose,*  
Visual Graphic Systems, Ltd.

Text and Cover Printer: *Quebecor/Hawkins*

Printed and bound in the United States of America.

01 02 03 04 — 10

International Thomson Editores  
Campos Eliseos 385, Piso 7  
Col. Polanco  
11560 Mexico D.F., Mexico

International Thomson Publishing GmbH  
Konigswinterer Strasse 418  
53227 Bonn, Germany

International Thomson Publishing Asia  
221 Henderson Road  
#05-10 Henderson Building  
Singapore 0315

International Thomson Publishing Japan  
Hirakawacho Kyowa Building, 31  
2-2-1 Hirakawacho  
Chiyoda-ku, Tokyo 102  
Japan

ISBN: 0-534-95472-3

#### Library of Congress Cataloging-in-Publication Data

Roth, Charles H.

Fundamentals of logic design / Charles H. Roth, Jr.—4th ed.

p. cm.

Includes bibliographical references and index.

ISBN 0-314-92218-0 (hard)

1. Logic circuits. 2. Logic design. I. Title.

TK7868.L6R67 1992

621.39'5—dc20

91-30668





# Preface

---

After studying this text, you should be able to apply switching theory to the solution of logic design problems. This means that you will learn both the basic theory of switching networks and how to apply it. After a brief introduction, you will study Boolean algebra, which provides the basic mathematical tool needed to analyze and synthesize an important class of switching networks. Starting from a problem statement, you will learn to design networks of logic gates which have a specified relationship between signals at the input and output terminals. Then you will study the logical properties of flip-flops, which serve as memory devices in sequential switching networks. By combining flip-flops with networks of logic gates, you will learn to design counters, adders, sequence detectors and similar networks.

This text is designed so that it can be used in either a standard lecture course or in a self-paced course. In addition to the standard reading material and problems, study guides and other aids for self-study are included in the text. The content of the text is divided into 27 study units. These units form a logical sequence so that mastery of the material in one unit is generally a prerequisite to the study of succeeding units. Each unit consists of four parts. First, a list of objectives states precisely what you are expected to learn by studying the unit. Next, the study guide contains reading assignments and study questions. As you work through the unit, you should write out the answers to these study questions. The text material and problem set which follow are similar to a conventional textbook.

When you complete a unit, you should review the objectives and make sure that you have met them.

The 27 study units are divided into three main groups. The first 10 units treat Boolean algebra and the design of combinational logic networks. Units 11 through 22 are mainly concerned with the analysis and design of clocked sequential logic networks, including networks for arithmetic operations. Units 23 through 27 cover the special problems encountered in the analysis and design of asynchronous sequential networks. The first 21 units can typically be covered in a one semester course taught at the Sophomore or Junior level. The remaining units can then be used as enrichment material for the better students, or they can be covered in the first part of a second course in digital systems design.

Several of the units include simulation or laboratory exercises. These exercises provide an opportunity to design a logic network and then test its operation. A number of logic simulators, which run on personal computers, may be used to verify the logic designs. The lab equipment required for testing includes a logic patchboard with flip-flops and several types of logic gates. If such equipment is not available, the lab exercises can be simulated or just assigned as design problems. This is especially important for Units 10, 16, and 27 since the comprehensive design problems in these units help to review and tie together the material in several of the preceding units.

This text is written for a first course in the logic design of digital systems. It is written on the premise that the student should understand and learn thoroughly certain fundamental concepts in a first course. Examples of such fundamental concepts are the use of Boolean algebra to describe the signals and interconnections in a logic network, use of systematic techniques for simplification of a logic network, interconnection of simple components to perform a more complex logic function, analysis of a sequential logic network in terms of timing charts or a state graph, and use of a control network to control the sequence of events in a digital system.

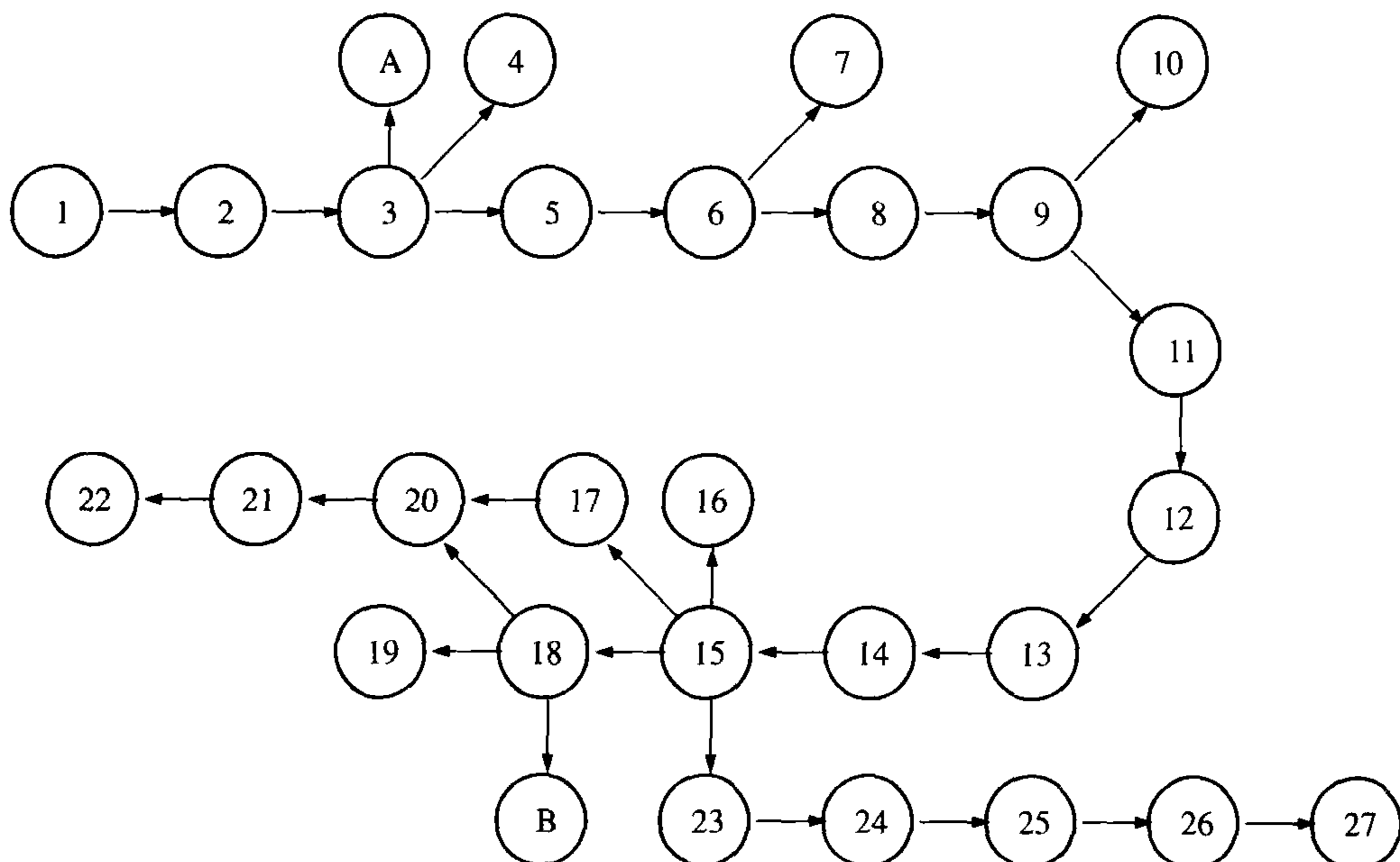
The text attempts to achieve a balance between theory and application. For this reason, the text does not overemphasize the mathematics of switching theory; however, it does present the theory which is necessary for understanding the fundamental concepts of logic design. After completing this text, the student should be prepared for a more advanced digital systems design course which stresses more intuitive concepts like the development of algorithms for digital processes, partitioning of digital systems into subsystems, and implementation of digital systems using currently available hardware. Alternatively, the student should be prepared to go on to a more advanced course in switching theory which further develops the theoretical concepts which have been introduced here.

Although the technology used to implement digital systems has changed significantly since the first edition of this text was published, the fundamental principles of logic design have not. Truth tables and state tables are still used to specify the behavior of logic networks, and Boolean algebra is still a basic mathematical tool for logic design. Even though programmable logic devices (PLDs) may be used instead of individual gates and flip-flops, reduction of logic equations is still necessary in order

to fit the equations into a small number of PLDs. Making a good state assignment is still required, because without a good assignment, the logic equations may not fit into one of the available PLDs.

This new edition offers a number of improvements over the third edition. Mixed logic and direct polarity notation are introduced and used for analysis and design of logic networks. Greater emphasis is placed on the use of programmable logic devices, and programmable gate arrays are introduced. The role of simulation and computer-aided design is discussed. New exercises and problems have been added to every unit, and several sections have been rewritten to clarify the presentation.

The text is suitable for both computer science and engineering students. All material relating to circuit aspects of logic gates is contained in Appendix A so that this material can conveniently be omitted by computer science students or other students with no background in electronic circuits. The text is organized so that Unit 4 on Algebraic Simplification and Unit 7 on the Quine-McCluskey procedure may be omitted without loss of continuity. Instructors who wish to place less emphasis on logic simplification can omit one or both of these units to allow more time for study of digital design techniques presented in the later units. The following diagram illustrates the unit prerequisite structure for the fourth edition:



Although many texts are available in the areas of switching theory and logic design, this text was developed specifically to meet the needs of a self-paced course in which students are expected to study the material on their own. Each of the units has undergone extensive class testing in a self-paced environment and has been revised based on student feedback.

Study guides and text material have been expanded as required so that students can learn from the text without the aid of lectures and so that almost all of the students can achieve mastery of all of the objectives. Supplementary materials were developed as the text was being written. An instructor's manual is available which includes suggestions for using the text in a standard or self-paced course, quizzes on each of the units, and suggestions for laboratory equipment and procedures. The instructor's manual also contains solutions to problems, to unit quizzes, and to lab exercises.

Since the computer plays an important role in the logic design process, integration of computer usage into the first logic design course is highly desirable. A computer-aided logic design program, called *LogicAid*<sup>™</sup>, is suggested for use with this textbook. *LogicAid* allows the student to easily derive simplified logic equations from minterms, truth tables, and state tables. This relieves the student of some of the more tedious computations and permits the solution of more complex design problems in a shorter time. *LogicAid* also provides tutorial help for Karnaugh maps and derivation of state graphs.



# How to Use This Book for Self-Study

---

If you wish to learn all of the material in this text to mastery level, the following study procedures are recommended for each unit:

1. Read the *Objectives* of the unit. These objectives provide a concise summary of what you should be able to do when you complete study of the unit.
2. Work through the *Study Guide*. After reading each section of the text, write out the answers to the corresponding study guide questions. In many cases, blank spaces are left in the study guide so that you can write your answers directly in this book. By doing this, you will have the answers conveniently available for later review. The study guide questions will generally help emphasize some of the important points in each section or will guide you to a better understanding of some of the more difficult points. If you cannot answer some of the study guide questions, this indicates that you need to study the corresponding section in the text more before proceeding. The answers to selected study guide questions are given in the back of this book; answers to the remaining questions can generally be found within the text.
3. Several of the units (Units 3, 4, 6, 7, 11, 13, 14, 21, 24, and 25) contain one or more programmed exercises. Each programmed exercise will guide you step-by-step through the solution of one of the more difficult types of problems encountered in this text. When working through a programmed exercise, be sure to write down your answer



for each part in the space provided before looking at the answer and continuing with the next part of the exercise.

4. Work the assigned *Problems* at the end of the unit. Check your answers against those at the end of the book and rework any problems which you missed.
5. Reread the *Objectives* of the unit to make sure that you can meet all of them. If in doubt, review the appropriate sections of the text.
6. If you are using this text in a self-paced course, you will need to pass a readiness test on each unit before proceeding with the next unit. The purpose of the readiness test is to make sure that you have mastered the objectives of one unit before moving on to the next unit. The questions on the test will relate directly to the objectives of the unit, so that if you have worked through the study guide and written out answers to all of the study guide questions and to all of the problems, you should have no difficulty passing the test.





# Contents

---

PREFACE	v
HOW TO USE THIS BOOK FOR SELF-STUDY	ix

---

<b>1</b>	<b>Introduction</b>	
	<b>Number Systems and Conversion</b>	
	Objectives	1
	Study Guide	2
1.1	Digital Systems and Switching Networks	4
1.2	Number Systems and Conversion	7
1.3	Binary Arithmetic	10
1.4	Binary Codes	12
	Problems	15

---

<b>2</b>	<b>Boolean Algebra</b>	
	Objectives	17
	Study Guide	18
2.1	Introduction	24
2.2	Basic Operations	24
2.3	Boolean Expressions and Truth Tables	27
2.4	Basic Theorems	29



2.5	Commutative, Associative, and Distributive Laws	31
2.6	Simplification Theorems	33
2.7	Multiplying Out and Factoring	34
	Problems	37
	Laws and Theorems of Boolean Algebra	40

### 3 Boolean Algebra (Continued)

	Objectives	41
	Study Guide	42
3.1	Inversion	47
3.2	Duality	49
3.3	Multiplying Out and Factoring Expressions	50
3.4	Exclusive - OR and Equivalence Operations	51
3.5	Positive and Negative Logic	54
	Programmed Exercises and Problems	57

### 4 Algebraic Simplification

	Objectives	63
	Study Guide	64
4.1	The Consensus Theorem	66
4.2	Algebraic Simplification of Switching Expressions	68
4.3	Proving Validity of an Equation	70
	Programmed Exercises and Problems	72

### 5 Applications of Boolean Algebra

	Objectives	79
	Study Guide	80
5.1	Conversion of English Sentences to Boolean Equations	86
5.2	Combinational Network Design Using a Truth Table	88
5.3	Minterm and Maxterm Expansions	89
5.4	General Minterm and Maxterm Expansions	92
5.5	Incompletely Specified Functions	95
5.6	Examples of Truth Table Construction	96
	Problems	99

### 6 Karnaugh Maps

	Objectives	105
	Study Guide	106
6.1	Minimum Forms of Switching Functions	116
6.2	2- and 3-Variable Karnaugh Maps	118
6.3	4-Variable Karnaugh Maps	123



6.4	Determination of Minimum Expressions Using Essential Prime Implicants	126
6.5	5- and 6-Variable Karnaugh Maps	131
6.6	Other Uses of Karnaugh Maps	135
6.7	Other Forms of Karnaugh Maps	136
	Programmed Exercises and Problems	138

## **7 Quine-McCluskey Method**

	Objectives	149
	Study Guide	150
7.1	Determination of Prime Implicants	155
7.2	The Prime Implicant Chart	158
7.3	Petrick's Method	161
7.4	Simplification of Incompletely Specified Functions	163
7.5	Simplification Using Map-Entered Variables	164
7.6	Conclusion	166
	Programmed Exercises and Problems	167

## **8 Multi-Level Gate Networks NAND and NOR Gates**

	Objectives	173
	Study Guide	174
8.1	Multi-Level Gate Networks	180
8.2	Other Types of Logic Gates	185
8.3	Functionally Complete Sets of Logic Gates	187
8.4	Design of Two-Level NAND- and NOR-Gate Networks	189
8.5	Design of Multi-Level NAND- and NOR-Gate Networks	192
8.6	Network Conversion Using Alternative Gate Symbols	194
8.7	Mixed Logic and Polarity Indication	197
	Problems	204

## **9 Multiple-Output Networks Multiplexers, Decoders, Read-Only Memories, and Programmable Logic Arrays**

	Objectives	209
	Study Guide	210
9.1	Introduction	216
9.2	Design of Two-Level Multiple-Output Networks	217
9.3	Multi-Output NAND and NOR Networks	222
9.4	Multiplexers	223
9.5	Decoders	227
9.6	Read-Only Memories	229
9.7	Programmable Logic Devices	234
	Problems	244



---

# 10

## Combinational Network Design

Objectives	249
Study Guide	250
10.1 Review of Combinational Network Design	252
10.2 Design of Networks with Limited Gate Fan-in	253
10.3 Simulation and Testing of Logic Networks	256
Design Problems	259

---

# 11

## Flip-Flops

Objectives	265
Study Guide	266
11.1 Gate Delays and Timing Diagrams	270
11.2 The Set-Reset Flip-Flop	272
11.3 The Trigger Flip-Flop	276
11.4 The Clocked T Flip-Flop	277
11.5 The J-K Flip-Flop	278
11.6 The Clocked J-K Flip-Flop	279
11.7 The D Flip-Flop	282
11.8 Clocked Flip-Flops with Clear and Preset Inputs	282
11.9 Characteristic Equations	284
Problems and Programmed Exercises	286

---

# 12

## Counters and Similar Sequential Networks

Objectives	293
Study Guide	294
12.1 Design of a Binary Counter	298
12.2 Counters for Other Sequences	301
12.3 Counter Design Using S-R Flip-Flops	305
12.4 Counter Design Using J-K Flip-Flops	308
12.5 Short-Cut Method for Deriving J-K Flip-Flop Input Equations	311
12.6 Counter Design Using D Flip-Flops	313
12.7 Design of a Code Converter	313
12.8 Shift Registers	315
12.9 Derivation of Flip-Flop Input Equations—Summary	316
Problems	319

---

# 13

## Analysis of Clocked Sequential Networks

Objectives	323
Study Guide	324
13.1 A Sequential Parity Checker	330
13.2 Analysis by Signal Tracing and Timing Charts	333
13.3 State Tables and Graphs	337



13.4	General Models for Sequential Networks	342
	Programmed Exercises and Problems	345

## 14 Derivation of State Graphs and Tables

	Objectives	355
	Study Guide	356
14.1	Design of a Sequence Detector	359
14.2	More Complex Design Problems	364
14.3	Guidelines for Construction of State Graphs	368
14.4	Serial Data Code Conversion	371
	Programmed Exercises and Problems	375

## 15 Reduction of State Tables State Assignment

	Objectives	385
	Study Guide	386
15.1	Elimination of Redundant States	393
15.2	Equivalent States	396
15.3	Determination of State Equivalence Using an Implication Table	397
15.4	Equivalent Sequential Networks	401
15.5	Incompletely Specified State Tables	403
15.6	Derivation of Flip-Flop Input Equations	404
15.7	Equivalent State Assignments	407
15.8	Guidelines for State Assignment	412
	Problems	417

## 16 Sequential Network Design

	Objectives	425
	Study Guide	426
16.1	Summary of Design Procedure	428
16.2	Design Example—Code Converter	428
16.3	Simulation and Testing of Sequential Networks	433
16.4	Overview of Computer-aided Design	437
	Design Problems	441

## 17 Iterative Networks

	Objectives	449
	Study Guide	450
17.1	Design of a Parity Checker	453
17.2	Design of a Comparator	455
17.3	Design of a Pattern Detector	458



17.4	Iterative Networks with Outputs from Each Cell	460
	Problems	462

---

## 18 MSI Integrated Circuits in Sequential Network Design

	Objectives	465
	Study Guide	466
18.1	Integrated Circuit Shift Registers	469
18.2	Integrated Circuit Counters	472
18.3	Design of Sequential Networks Using Counters	477
18.4	Register Transfers and 3-State Logic	480
	Problems	483

---

## 19 Sequential Network Design with Programmable Logic Devices (PLDs)

	Objectives	487
	Study Guide	488
19.1	Design of Sequential Networks Using ROMs and PLAs	490
19.2	Design of Sequential Networks Using PALs	492
19.3	Other Sequential Programmable Logic Devices (PLDs)	498
19.4	Programmable Gate Arrays (PGAs)	503
	Problems	509

---

## 20 Networks for Addition and Subtraction

	Objectives	515
	Study Guide	516
20.1	Representation of Negative Numbers	519
20.2	Design of Binary Adders	524
20.3	Binary Subtractors	531
	Problems	533

---

## 21 Networks for Arithmetic Operations

	Objectives	537
	Study Guide	538
21.1	Serial Adder with Accumulator	540
21.2	Design of a Parallel Multiplier	543
21.3	Design of a Binary Divider	548
	Programmed Exercises and Problems	553

---

## 22 State Machine Design with SM Charts

	Objectives	565
	Study Guide	566



22.1	State Machine Charts	567
22.2	Derivation of SM Charts	573
22.3	Realization of SM Charts	579
	Problems	583

## 23 Analysis of Asynchronous Sequential Networks

	Objectives	589
	Study Guide	590
23.1	Introduction	592
23.2	Analysis of an Asynchronous Network with S-R Flip-Flops	594
23.3	Analysis of an Asynchronous Gate Network	598
23.4	Race Conditions and Cycles	601
	Problems	603

## 24 Derivation and Reduction of Primitive Flow Tables

	Objectives	607
	Study Guide	608
24.1	Derivation of Primitive Flow Tables	609
24.2	Reduction of Primitive Flow Tables	613
	Programmed Exercise and Problems	619

## 25 State Assignment and Realization of Flow Tables

	Objectives	625
	Study Guide	626
25.1	Introductory Example	629
25.2	State Assignments for 3- and 4-Row Tables	634
25.3	Shared-Row Assignments	637
25.4	Completion of the Output Table	641
25.5	The One-Hot Assignment	643
	Programmed Exercise and Problems	645

## 26 Hazards

	Objectives	653
	Study Guide	654
26.1	Hazards in Combinational Networks	657
26.2	Detection of Static 0- and 1-Hazards	660
26.3	Dynamic Hazards	663
26.4	Design of Hazard-Free Combinational Networks	664
26.5	Essential Hazards	666
26.6	Hazard-Free Realizations Using S-R Flip-Flops	668
	Problems	673



## 27 Asynchronous Sequential Network Design

Objectives	677
Study Guide	678
27.1 Summary of Design Procedure	679
27.2 Short-Cut Method for Deriving S-R Flip-Flop	
Input Equations	680
27.3 Design Example	681
27.4 Testing Asynchronous Sequential Networks	689
Design Problems	690

## Appendixes

### A Discrete and Integrated Circuit Logic Gates

Objectives	695
Study Guide	696
A.1 Diode AND and OR Gates	699
A.2 Transistor Logic Circuits	701
A.3 TTL Integrated Circuit Logic	704
A.4 MOS and CMOS Logic	707
Problems	711

### B IEEE Standard Logic Symbols

B.1 Alternative Symbols for Gates and Flip-Flops	713
B.2 Representation of MSI Functions	715

### C Proofs of Theorems

C.1 Essential Prime Implicants	719
C.2 State Equivalence Theorem	720
C.3 Justification of Short-Cut Method for Deriving S-R Input Equations	720

REFERENCES	723
------------	-----

ANSWERS TO SELECTED STUDY GUIDE QUESTIONS AND PROBLEMS	727
--	-----

INDEX	765
-------	-----