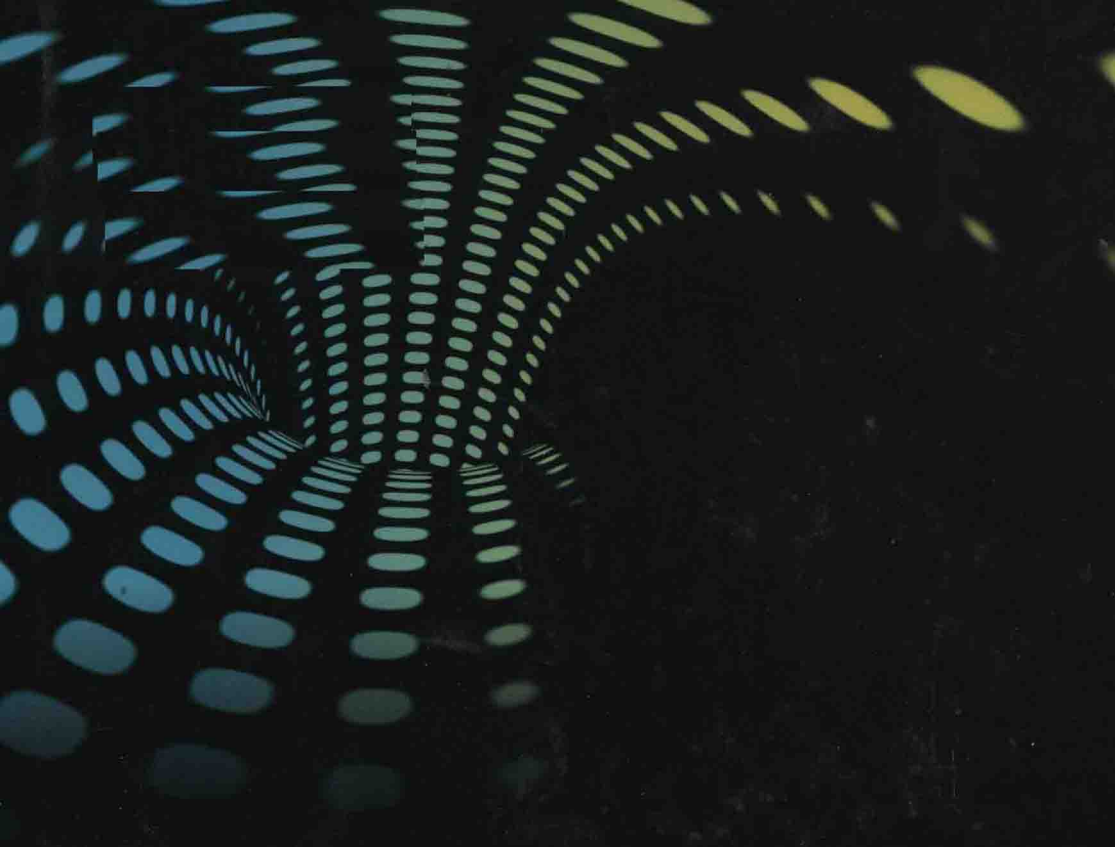

Microprocessors

8086 with Support Chips and 80386 in Protected Mode

P K Mukherjee

Alpha Science

MICROPROCESSORS

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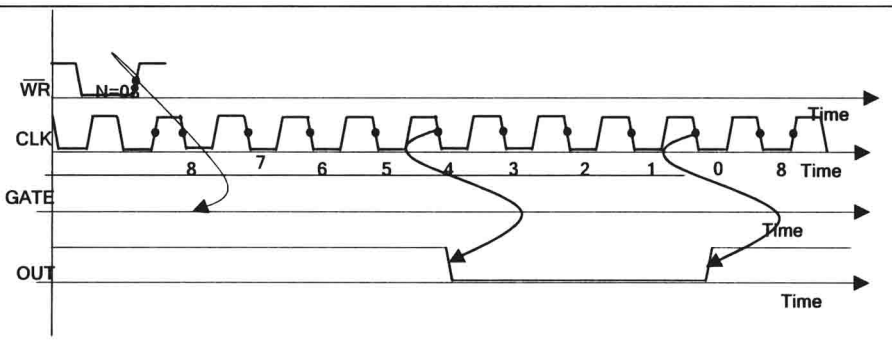
ERRATA

(Microprocessors by P.K. Mukherjee)

Page No 2.11	In Line No 10	lower byte to be changed to **lower**
Page No 2.11	In Line No 12	upper byte to be changed to **upper**
Page No 4.12	In Fig. 4.8	The Lines coming from 8086 to 8288 are $\overline{S}_2$ - $\overline{S}_0$ and the line going from 8288 to 8282 (s) through Inverter is **DEN**
Page No 5.8	In Fig. 5.3	MOD (3) to be changed to **MOD (2)**
		REG (2) to be changed to **REG (3)**
Page No 5.9	In Section 5.4.1	MOD (3) to be changed to **MOD (2)**
		REG (2) to be changed to **REG (3)**
Page No 9.5	In Fig. 9.2	PBC Address to be changed to **PCB Address**
Page No 9.8	In Fig. 9.6	The FQP for P. ID 3 should be **2** instead of 6
		The FQP for P. ID 6 should be **0** instead of 2
		The FQP for P. ID 9 should be **6** instead of blank
		The FQP for P. ID 10 should be **blank** instead of 6
Page No 10.9	In Fig. 10.8	Right most extra lines are not required
Page No 10.11	In Fig. 10.10	The line going from 8288 to the NAND gate is DEN and the input to 8259 from 8086 is **A_1 of the processor coming to A_0 of PIC**
Page No 10.18	In Fig. 10.22	The gate, where $\overline{SP}/\overline{EN}$ from 8259-A is going should be a **NAND** gate (instead of AND), and the other input of NAND is **DEN** coming from 8288 In last column, the middle chip is **RAM** (and not ROM)
Page No 11.1	In Fig. 11.1	The three inputs coming to 8255-A (not shown in the Figure) are **$\overline{RD}$, $\overline{WR}$ and $\overline{CS}$**
Page No 11.4	In Fig. 11.2	LSB of the control word is **PC_L** (and not PC_1)
Page No 12.4	In 2nd para 1st line	the ESC code is followed by **3 bits** (and not 5 bits)
Page No 12.5	In Fig. 12.3	The line going out of 8282(s) above A19-A0 is **$\overline{BHE}$** (and not $\overline{DEN}$)
		In first para second line- **the I/O processor can fetch** (and not execute)
Page No 12.6	In Fig. No 12.4	It is Connection between 8086 and **8089** (and not between 8086 and 8087)
Page No 12.6	In Fig. 12.4	In left column the bottom most chip is **8089** (and not 8087)
		In mid column the chip at the bottom is **8259-A** (and not 8288-A)
Page No 12.7	In Fig. 12.5	**A module in Loosely coupled configuration** (and not The $\overline{AEN}$ connection between 8289 and 8288)
Page No 12.13	In Fig. 12.9	BPRO from Arbiter 1 is going to **BPRN of Arbiter 2**
Page No 12.14	In Fig. 12.12	In 8288 the line coming from 8289 is **$\overline{AEN}$** (and not CLK)
Page No 12.18	In last but one para of 12.5.2- in last line	a **(space)** between transceiver and instead
Page No 12.19	In Fig. 12.16	The top chip on the left side is **8282** (and not 8285), next chip below it is **8286** (shown correctly).

		The top chip on the right side is **8289** (and not 8286), next chip below it is **8282** (and not 8288). The chip below that is **8286** (and not 8288).
Page No 12.19	In Fig. 12.16	MCE/PDEN should be changed to **MCE/$\overline{\text{PDEN}}$**
Page No 12.20	In Fig. 11.17	Fig 11.17 should be **Fig 12.17**
Page No 12.20	In Fig. 12.17	The top chip on the left side is **8282** (and not 8285), next chip below it is **8286** (shown correctly). The chip below that is **8288** (not mentioned)
		The top chip on the right side is **8289** (and not 8286), next chip below it is **8282** (and not 8288). The chip below that is **8286** (and not 8288).
Page No 13.6	In Fig. 13.9	A **(connection)** between Sync character 2 and Sync character 1 block
Page No 13.7	In Fig. 13.10	SYNCDET/BRKDET pin is **Bidirectional**
Page No 13.19	In Fig. 13.19	The number of pins in 9 Pin DB Connector is **9** (and not 25 as shown)
Page No 14.2	In Fig. 14.1	**Pin Outs of 8254** (and not 8285)
Page No 14.7	In Fig. 14.9	The correct Figure **is as shown below** (and not one given in the book)



Page No 14.9	In Fig. 14.12	The third pin from bottom on the left side is **$\overline{\text{IOW}}$** (and not $\overline{\text{LOW}}$)
Page No 14.17	In Fig. 14.15 (a)	It is Mode **Register** (and not Mode Rigister)
Page No 14.22	In Fig. 14.20	The **Q output of FF1** will go to **HOLD of 8086** The **output of N (2)** will go to **$\overline{\text{OE}}$ pin of 8282(1).** The bottom chip is **8237**
Page No 15.10	In Fig. 15.12	Around Q_1 some additional lines are not required
Page No 15.11	In Fig. 15.13	Around Q_1 some additional lines are not required
Page No 17.8	In Fig. 17.6	CS [ ] [11] [ ] should be changed to CS [ ] [TI] [ ]
Page No 19.3	In Fig. 19.2	The vertical line should be at **2 LSB** (and not at 1 LSB)
Page No 19.17	In Fig. 19.16	Tag bits for Set No 2, Slot No 0 should be **10** (and not 100)

To my wife who left a bit too early

Preface

I was introduced to Microprocessors and related topics by great teachers like Prof. R N Biswas, Prof. S K Bose, Prof. G Barua, Prof. A Joshi, Prof. Raghuram, Prof. Srivatsan and many other eminent professors of IIT Kanpur during my two long term summer school in 1985 and 1992. Since then, I have been teaching Microprocessors at the Department of Electronics Engineering, Institute of Technology, Banaras Hindu University, Varanasi to B.Tech and M.Tech students.

There are some very good books on Microprocessors by eminent authors like Douglas V Hall, Liu and Gibbson, Ray and Bhurchandi, Bery B Bray, Antanokos, Singh and Trebble, Kenneth J Ayala, John Uffenbeck, S K Bose, Raffiquzamman, B P Singh and many more.

It was a long time desire of my students that I write a book on Microprocessors and that too exactly the way I teach in the class. With that in mind, I am trying to write this book.

I am sure it will be helpful to the undergraduate and post graduate students studying the course.

I am thankful to many of my students, who's interaction, within and out of the class compelled me to read the subject.

My gratitude to those teachers, who taught me teach.

P K Mukherjee

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