Prestopnik

Laboratory Manual for

DIGITAL ELECTRONICS

Concepts and Applications for Digital Design

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Prestopnik: Lab Manual for DIGITAL ELECTRONICS: CONCEPTS AND APPLICATIONS FOR DIGITAL DESIGN

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Dedicated with love to my children Nathan, Emily, and Adam.

PREFACE

This Digital Electronics laboratory manual has been produced to enable the student to experience the hands-on creative design aspects of the digital electronics field. By transforming the theoretical concepts studied in the classroom into functioning digital circuits, students are able to reinforce ideas and develop the creative design flair necessary for successful engineering.

This lab manual is coordinated to follow the progression of subject matter covered in **Digital Electronics: Concepts and Applications for Digital Design**. Forty three lab experiments plus several project experiments carry the student from the fundamental ideas of digital logic to more advanced and interesting design work. While the number of labs may seem to exceed that which can be utilized in a typical digital course sequence, the organization is deliberate. Since no two classes of students are ever the same and since no two semesters ever follow exactly the same teaching pattern, a few all encompassing lab experiments would be restrictive for the instructor. Rather, the labs in this manual are simply experiments on important digital subjects that instructors can organize in any way to meet the objectives of their course and the needs of their students. For example, it is quite likely that experiments 1, 2, and 3 (AND, OR, INVERT) could all be accomplished in the same lab session. If for some reason all this material is inappropriate at the time, the instructor has the flexibility to use only what is needed.

A major objective of this manual is to provide labs to enhance the design abilities of students. For this reason, many experiments call upon students to create an appropriate circuit for the engineering problem described in the experiment. This sharply contrasts with a cookbook approach where circuits are given and merely assembled. Some may argue that the majority of lab time should be spent by students testing circuits. I counter with the argument that students who can design a digital circuit and then build it will have no problem testing nor understanding the circuit or the design concepts. Naturally, the students' laboratory experience is enhanced when guided by the instructor. The insightful instructor will verify periodically that students are on track in their design efforts throughout the lab session.

It is suggested that most of the experiments be carried out using TTL or LSTTL parts due to the ruggedness and inexpensive nature of these devices. However, it is certainly possible to build the circuits using CMOS or ECL logic if desired. Although TTL is suggested for circuit construction you will not find experiment after experiment simply testing every TTL part on the market. Rather, TTL - and simple TTL for that matter - is utilized only as the technology base for designing the circuits in this manual. Using the same philosophy as in the accompanying textbook, logic fundaments - not TTL fundamentals - are stressed. For example, rather than force fit a predesigned TTL counter into a design application, it is far more benefical for students to know and understand how to design a specific counter to fit the specific application. The reasoning is simple. Today's students will not necessarily be using TTL or other current logic families when they become tomorrow's designers. They are more likely to encounter advanced logic technologies that require them to know how to design rather than know how to look up a TTL part in a data book.

All of the experiments detailed in the manual can be assembled and tested on the digital trainers commonly available to the educational market. In fact this is an assumption upon which each experiment is based. Occassionally, an additional logic indicator or switch may be required. Indicators can be easily fashioned with an LED and a current limiting resistor or simply by using an oscilloscope, meter, or logic probe to show an output level. DIP switches and pull-up resistors easily provide additional inputs. When necessary these additional devices are shown in the experiment affected. With the exception of the projects, which may necessitate additional resources, all labs can be accomplished with a minimum amount of expense.

How The Labs Are Organized: Each lab consists of a statement of purpose to set an objective for the student. Following this is a parts list stating the components required for the experiment. As mentioned, the availability of a logic trainer is assumed.

Several key facts are then listed to focus the students' attention on critical information required for successful completion of the experiment. Then a number of process steps take the students through the entire experiment. Space is supplied for the recording of data and for answers to related questions. Since the pages of this manual can be removed, students will have all the necessary information required for lab reports with the exception of an analytical treatise of the lab theory.

Suggested Lab Groupings: Since it may be possible to run several experiments in a single lab session (subject to time and student ability) the following is a suggested list of experiments which could be used in a typical two to three hour lab session. These labs are not dependent on each other, freeing the instructor to choose any pattern of experimentation desired. But, this listing is typical for a digital course.
Labs 1, 2, and 3; Labs 4, 5, and 6; Labs 7 and 8; Labs 9 and 10; Labs 11, 12, and 13; Lab 14 may be used with 9 and 10; Labs 15 and 16; Labs 17 and 18; Labs 19 and 20; Lab 21; Lab 22; Lab 23; Labs 24, 25, and 26; Labs 27, 28 and 29; Lab 30; Lab 31; Lab 32 and 33; Lab 34; Labs 35 and 36; Labs 37 and 38; Lab 39; Lab 40 and 41; Lab 42; Lab 43.

The projects are run separately. Suggested lengths: Lab 44 - one week; Lab 45 - two weeks; Lab 46 - three weeks.

Acknowledgements

I am indebted to many people and organizations for their contributions to the creation of this laboratory manual. I am pleased to thank Texas Instruments, Inc. and Intel, Inc. for the use of their integrated circuit data sheets found in the appendix.

The following reviewers made useful suggestions that have enhanced the value of this lab manual. I thank these gentlemen for their time and effort:

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Gerald Schickman, Miami Dade Community College, North
Steve Yelton, Cincinnati Technical College

I sincerely appreciate the work and dedication shown by the Saunders College Publishing staff including Barbara Gingery, Electronics Technology Editor and Laura Shur, Editorial Assistant.

It seems appropriate to mention in this lab manual the work, creativity, and friendship shown over the years by Walter (Jake) Theurer. As the Electrical Technology laboratory technician at Fulton-Montgomery Community College, Jake's innovations, enthusiam, and limitless energy have been a wonderful asset to the college and my teaching. I am fortunate to have his assistance in the lab.

Finally and most importantly, my love and thanks go to my wife, Jan, and our children Nathan, Emily, and Adam. I am especially grateful for their understanding, love, and support.

Richard J. Prestopnik
September 1989

DIGITAL ELECTRONICS: CONCEPTS AND APPLICATIONS FOR DIGITAL DESIGN LABORATORY MANUAL

Laboratory Experiments

LABORATORY EXPERIMENT 1 —— THE AND FUNCTION

PURPOSE To investigate the logical operation of the AND function including basic gate operation, enable and disable capability, and waveform analysis.

PARTS LIST: 7408 AND gate, Oscilloscope, Clock Generator.

KEY FACTS: 1) The AND gate output is high when all inputs are high; otherwise the output is low. 2) A circuit is enabled when a controlling input allows another input to change the circuit output level. When the output level is prevented from changing, then the circuit is disabled.

PROCESS: 1) Test a 7408 AND gate for all possible input combinations using switches for inputs and a LED for the output. Use the data sheets in the appendix of this manual for the pin connections or use your own data manual. Enter the output values corresponding to each input combination in the data section. Draw the circuit below:

A	B	Y
0	0	
0	1	
1	0	
1	1	

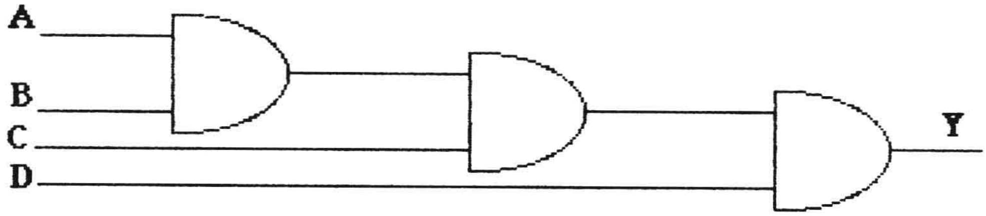
Which input combination is the unique input combination? ______________________

Why is this significant? ______________________

Why are the non-unique input combinations useful as well? ______________________

____

2) Assign pin numbers to each AND gate input and output in the following circuit:



Build the circuit and test the circuit's response to all possible input combinations. Record your data below.

A	B	C	D	Y

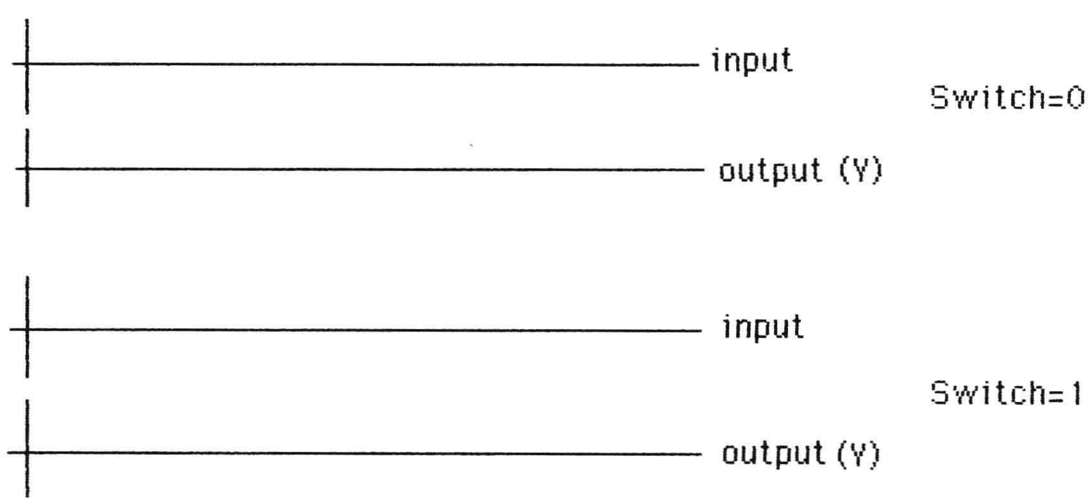
What function have you created? __________

What can you conclude about the AND function from this circuit? ____________________

____

Identify the unique input combination. ________

3) Using a single 2-input AND gate, connect one input to a switch and the other to a clock generator (1 kHz). Monitor on a dual channel oscilloscope the clock input waveform and the AND gate output signal (Y). Record the scope patterns when the switch is high and again when the switch is low. Determine when the gate is enabled and disabled. Record your waveforms below.



LABORATORY EXPERIMENT 2 —— THE OR FUNCTION

PURPOSE To investigate the logical operation of the OR function including basic gate operation, enable and disable capability, and waveform analysis.

PARTS LIST: 7432 OR gate, Clock Generator, Oscilloscope.

KEY FACTS: 1) The OR gate output is high when any input is high; the output is low only when all inputs are low. 2) A circuit is enabled when a controlling input allows another input to change the circuit output level. When the output level is prevented from changing, then the circuit is disabled.

PROCESS: 1) Test an OR gate for all possible input combinations using switches for inputs and a LED for the output. Use the data sheets in the appendix of this manual for the pin connections or use your own data manual. Enter the output values corresponding to each input combination on the truth table shown. Draw the circuit as well.

A	B	Y
0	0	
0	1	
1	0	
1	1	

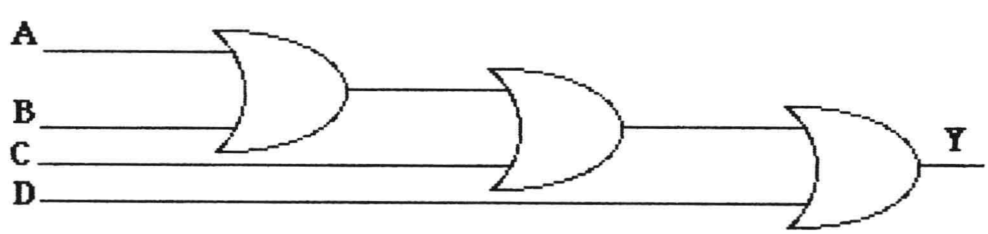
Which input combination is the unique input combination? ____________

Why is this significant? ____________

Why are the non-unique input combinations useful as well? ____________

____

2) Assign pin numbers to each OR gate input and output in the following circuit:



Build the circuit and test the circuit's response to all possible input combinations. Record your data below.

A	B	C	D	Y

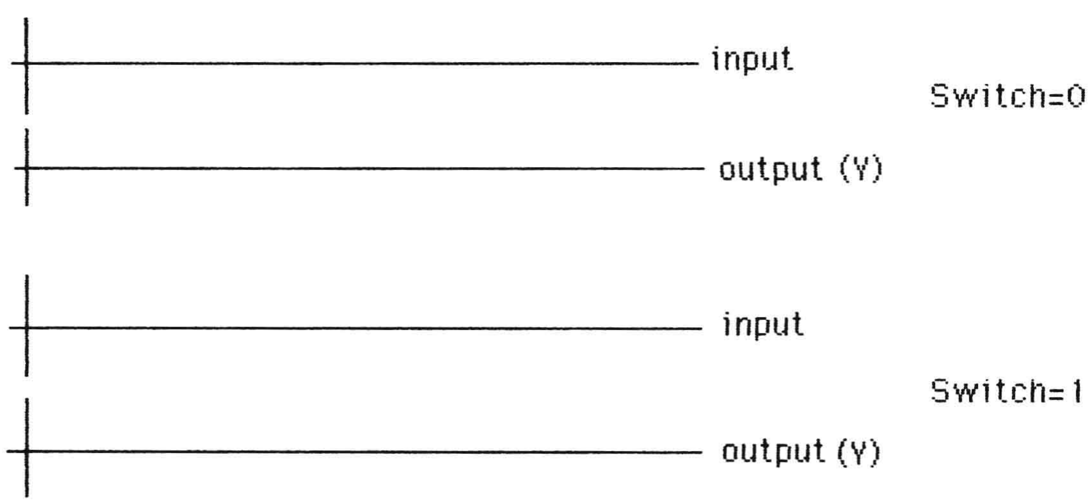
What function have you created? __________

What can you conclude about the OR function from this circuit? __________________________

____

Identify the unique input combination. _______

3) Using a single 2-input OR gate, connect one input to a switch and the other to a clock generator (1 kHz). Monitor on a dual channel oscilloscope the clock input waveform and the OR gate output signal (Y). Record the scope patterns when the switch is high and when the switch is low. Determine when the gate is enabled and disabled.



PURPOSE: To verify the complementing property of the inverter and to determine the delay time imparted to a digital signal by a logic gate.

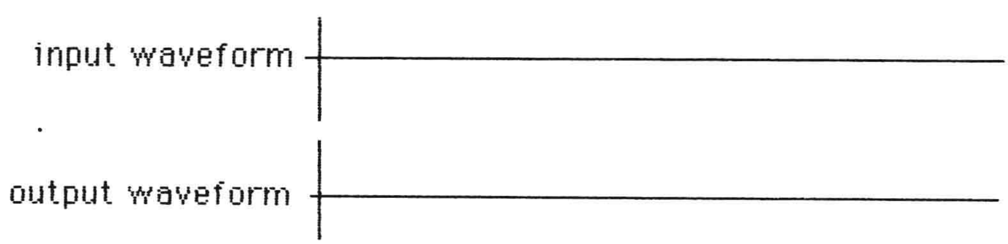
PARTS LIST: 7404 Inverter, Clock Generator, Oscilloscope.

KEY FACTS: 1) Inverters complement digital signals so that a high input appears as a low output and vise-versa. 2) Propagation delay time is the delay in the change of an output signal as compared to the input signal initiating the change in output.

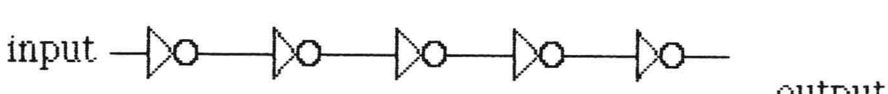
PROCESS: 1) Test the basic operation of an inverter gate by connecting the input to a switch and the output to a light. Note the output response when the input is both high and low.

input	output
0	
1	

2) Replace the switch input with an 1kHz square wave clock signal. Monitor on the oscilloscope both input and output. Record the waveforms in the data section. If possible, vary the duty cycle of the input waveform. Does inversion still take place?



3) Cascade five inverter gates together as shown:



Connect the input to a switch and test each gate output with a logic probe or test LED for a low and high input levels. Repeat the process using the oscilloscope and a 1 kHz input square wave signal.

input = low	input = high
output at:	output at:
1st inverter=	1st inverter=
2nd inverter=	2nd inverter=
3rd inverter=	3rd inverter=
4th inverter=	4th inverter=
5th inverter=	5th inverter=

How does the 1 kHz input waveform confirm the readings above?

4) Increase the input frequency to 1 MHz. Compare on the oscilloscope the positive edge of the input signal to the negative edge of the last inverter's output signal. Measure the time difference between the two. Divide this number by five to approximate the delay of one inverter stage. Does this calculation match the data book specification for the inverter's propagation delay?

Delay time from the positive edge of the input signal to the negative edge of the last inverter's output signal =

$$\frac{\text{Total delay time}}{5} = \frac{\_\_\_\_\_\_}{5} = \text{delay of one inverter}$$

sketch waveform:

input

last inverter's output

LABORATORY EXPERIMENT 4 —— THE NAND FUNCTION

PURPOSE To investigate the logical operation of the NAND function including basic gate operation, enable and disable capability, and waveform analysis.

PARTS LIST: 7400 NAND gate, Clock Generator, Oscilloscope.

KEY FACTS: 1) The NAND gate output is low when all inputs are high; otherwise the output is high. 2) A circuit is enabled when a controlling input allows another input to change the circuit output level. When the output level is prevented from changing, then the circuit is disabled.

PROCESS: 1) Test a NAND gate for all possible input combinations using switches for inputs and a light for the output. Use the data sheets in the appendix of this manual for the pin connections or use your own data manual. Enter the output values corresponding to each input combination below.

A	B	Y
0	0	
0	1	
1	0	
1	1	

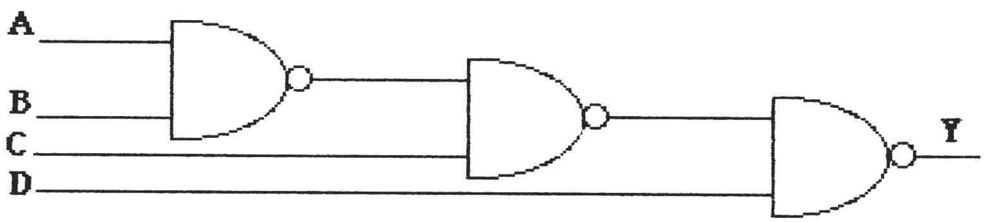
Which input combination is the unique input combination? ______________

Why is this significant? ______________

Why are the non-unique input combinations useful as well? ______________

____

2) Assign pin numbers to each NAND gate input and output in the following circuit:



Build the circuit and test its response to all possible input combinations. Record your data on the following page. Does this configuration create a larger NAND function? Write the logic equation for Y.