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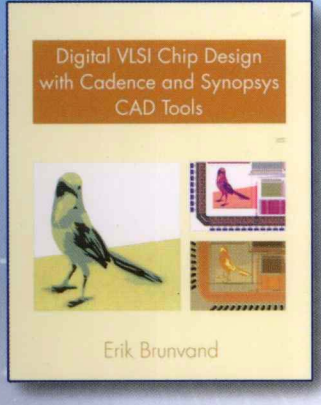
数字VLSI芯片设计

——使用Cadence和Synopsys CAD工具



Digital VLSI Chip Design

with Cadence and Synopsys CAD Tools

[美] Erik Brunvand 著

電子工業出版社
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国外电子与通信教材系列

数字 VLSI 芯片设计

——使用 Cadence 和 Synopsys CAD 工具

（英文版）

Digital VLSI Chip Design with Cadence and

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内容简介

本书介绍如何使用Cadence和Synopsys公司的CAD工具来实际设计数字VLSI芯片。读者通过本书可以循序渐进地学习这些CAD工具，并使用这些软件设计出可制造的数字集成电路芯片。本书内容按集成电路的设计流程编排，包括CAD设计平台、电路图输入、Verilog仿真、版图编辑、标准单元设计、模拟和数模混合信号仿真、单元表征和建库、Verilog综合、抽象形式生成、布局布线及芯片总成等工具；每一工具的使用都以实例说明，最后给出了一个设计简化MIPS微处理器的完整例子。本书可与有关集成电路设计理论的教科书配套使用，可作为高等院校有关集成电路设计理论类课程的配套教材和集成电路设计实践类课程的教科书，也可作为集成电路设计人员的培训教材和使用手册。

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序

2001年7月间，电子工业出版社的领导同志邀请各高校十几位通信领域方面的老师，商量引进国外教材问题。与会同志对出版社提出的计划十分赞同，大家认为，这对我国通信事业、特别是对高等院校通信学科的教学工作会很有好处。

教材建设是高校教学建设的主要内容之一。编写、出版一本好的教材，意味着开设了一门好的课程，甚至可能预示着一个崭新学科的诞生。20世纪40年代MIT林肯实验室出版的一套28本雷达丛书，对近代电子学科、特别是对雷达技术的推动作用，就是一个很好的例子。

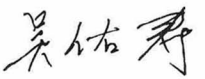
我国领导部门对教材建设一直非常重视。20世纪80年代，在原教委教材编审委员会的领导下，汇集了高等院校几百位富有教学经验的专家，编写、出版了一大批教材；很多院校还根据学校的特点和需要，陆续编写了大量的讲义和参考书。这些教材对高校的教学工作发挥了极好的作用。近年来，随着教学改革不断深入和科学技术的飞速进步，有的教材内容已比较陈旧、落后，难以适应教学的要求，特别是在电子学和通信技术发展神速、可以讲是日新月异的今天，如何适应这种情况，更是一个必须认真考虑的问题。解决这个问题，除了依靠高校的老师和专家撰写新的符合要求的教科书外，引进和出版一些国外优秀电子与通信教材，尤其是有选择地引进一批英文原版教材，是会有好处的。

一年多来，电子工业出版社为此做了很多工作。他们成立了一个“国外电子与通信教材系列”项目组，选派了富有经验的业务骨干负责有关工作，收集了230余种通信教材和参考书的详细资料，调来了100余种原版教材样书，依靠由20余位专家组成的出版委员会，从中精选了40多种，内容丰富，覆盖了电路理论与应用、信号与系统、数字信号处理、微电子、通信系统、电磁场与微波等方面，既可作为通信专业本科生和研究生的教学用书，也可作为有关专业人员的参考材料。此外，这批教材，有的翻译为中文，还有部分教材直接影印出版，以供教师用英语直接授课。希望这些教材的引进和出版对高校通信教学和教材改革能起一定作用。

在这里，我还要感谢参加工作的各位教授、专家、老师与参加翻译、编辑和出版的同志们。各位专家认真负责、严谨细致、不辞辛劳、不怕琐碎和精益求精的态度，充分体现了中国教育工作者和出版工作者的良好美德。

随着我国经济建设的发展和科学技术的不断进步，对高校教学工作会不断提出新的要求和希望。我想，无论如何，要做好引进国外教材的工作，一定要联系我国的实际。教材和学术专著不同，既要注意科学性、学术性，也要重视可读性，要深入浅出，便于读者自学；引进的教材要适应高校教学改革的需要，针对目前一些教材内容较为陈旧的问题，有目的地引进一些先进的和正在发展中的交叉学科的参考书；要与国内出版的教材相配套，安排好出版英文原版教材和翻译教材的比例。我们努力使这套教材能尽量满足上述要求，希望它们能放在学生们的课桌上，发挥一定的作用。

最后，预祝“国外电子与通信教材系列”项目取得成功，为我国电子与通信教学和通信产业的发展培土施肥。也恳切希望读者能对这些书籍的不足之处、特别是翻译中存在的问题，提出意见和建议，以便再版时更正。



中国工程院院士、清华大学教授

“国外电子与通信教材系列”出版委员会主任

出 版 说 明

进入21世纪以来，我国信息产业在生产和科研方面都大大加快了发展速度，并已成为国民经济发展的支柱产业之一。但是，与世界上其他信息产业发达的国家相比，我国在技术开发、教育培训等方面都还存在着较大的差距。特别是在加入WTO后的今天，我国信息产业面临着国外竞争对手的严峻挑战。

作为我国信息产业的专业科技出版社，我们始终关注着全球电子信息技术的发展方向，始终把引进国外优秀电子与通信信息技术教材和专业书籍放在我们工作的重要位置上。在2000年至2001年间，我社先后从世界著名出版公司引进出版了40余种教材，形成了一套“国外计算机科学教材系列”，在全国高校以及科研部门中受到了欢迎和好评，得到了计算机领域的广大教师与科研工作者的充分肯定。

引进和出版一些国外优秀电子与通信教材，尤其是有选择地引进一批英文原版教材，将有助于我国信息产业培养具有国际竞争能力的技术人才，也将有助于我国国内在电子与通信教学工作中掌握和跟踪国际发展水平。根据国内信息产业的现状、教育部《关于“十五”期间普通高等教育教材建设与改革的意见》的指示精神以及高等院校老师们反映的各种意见，我们决定引进“国外电子与通信教材系列”，并随后开展了大量准备工作。此次引进的国外电子与通信教材均来自国际著名出版商，其中影印教材约占一半。教材内容涉及的学科方向包括电路理论与应用、信号与系统、数字信号处理、微电子、通信系统、电磁场与微波等，其中既有本科专业课程教材，也有研究生课程教材，以适应不同院系、不同专业、不同层次的师生对教材的需求，广大师生可自由选择和自由组合使用。我们还将与国外出版商一起，陆续推出一些教材的教学支持资料，为授课教师提供帮助。

此外，“国外电子与通信教材系列”的引进和出版工作得到了教育部高等教育司的大力支持和帮助，其中的部分引进教材已通过“教育部高等学校电子信息科学与工程类专业教学指导委员会”的审核，并得到教育部高等教育司的批准，纳入了“教育部高等教育司推荐——国外优秀信息科学与技术系列教学用书”。

为做好该系列教材的翻译工作，我们聘请了清华大学、北京大学、北京邮电大学、南京邮电大学、东南大学、西安交通大学、天津大学、西安电子科技大学、电子科技大学、中山大学、哈尔滨工业大学、西南交通大学等著名高校的教授和骨干教师参与教材的翻译和审校工作。许多教授在国内电子与通信专业领域享有较高的声望，具有丰富的教学经验，他们的渊博学识从根本上保证了教材的翻译质量和专业学术方面的严格与准确。我们在此对他们的辛勤工作与贡献表示衷心的感谢。此外，对于编辑的选择，我们达到了专业对口；对于从英文原书中发现的错误，我们通过与作者联络、从网上下载勘误表等方式，逐一进行了修订；同时，我们对审校、排版、印制质量进行了严格把关。

今后，我们将进一步加强同各高校教师的密切关系，努力引进更多的国外优秀教材和教学参考书，为我国电子与通信教材达到世界先进水平而努力。由于我们对国内外电子与通信教育的发展仍存在一些认识上的不足，在选题、翻译、出版等方面的工作中还有许多需要改进的地方，恳请广大师生和读者提出批评及建议。

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To Sandy and Scruggs

Preface

THIS BOOK covers the practical aspects of digital VLSI chip design using commercial CAD tools from Cadence Design Systems, Inc. and Synopsys, Inc. It is intended as a supplement to a more theoretical textbook such as *CMOS VLSI Design: A Circuits and Systems Perspective* by Weste and Harris (Addison Wesley) [1] or *Digital Integrated Circuits: A design Perspective* by Rabaey, Chandrakasan, and Nikolic (Prentice Hall) [2] to give just two examples.

One thing that makes a practical chip-building component of a digital VLSI course possible is the use of powerful commercial CAD tools for integrated circuit design. The use of different tools in different parts of the design process to make a complete chip is known as a "tool flow." In a commercial design environment, the design team will very likely choose "best in class" tools for each step in the design process. That is, after careful evaluation the best available tool will be used for each step even if it means buying tools from many different vendors. In a university environment our CAD tool budget is usually more constrained, as is our ability to spend time interfacing tools from different vendors.

The VLSI CAD flow described in this book uses tools from two vendors: Cadence Design Systems, Inc. and Synopsys Inc. These tools are extremely good at keeping track of the myriad details required to make a working chip, but they have a notoriously steep learning curve. Over the years I've developed detailed tutorial examples for each of the tools in the design flow. Other instructors around the world are doing the same thing, which seems like needless duplication of effort. I thought that perhaps a book that collects these tutorials in one place, and connects them into a cohesive flow that represents the entire chip design process, would be useful to other designers, students, and instructors. This book is not meant to replace a VLSI design textbook, but to augment it.

This book can also serve as a reference for chip designers who use these tools in their own design flow. I find that I refer to it quite often myself as I get to various points in a chip project. There are indeed many details to remember.

A Digital VLSI Course

This book came about from years of teaching a Digital VLSI course at the University of Utah. I have strong feelings about the curriculum of this course. In particular, even though it is the first course related to digital integrated circuit design that many students take, I believe that they should have the experience of designing a complete chip project to the point where it can be fabricated. The semester proceeds as follows:

- First, we study transistor theory for a solid foundation.
- We then learn how to use CMOS transistors to build Boolean gates and logic functions.
- Next we study how the transistors are fabricated, and how to draw the layouts that define the fabrication layers.
- Students then form teams and develop their own small CMOS cell library consisting of 10–20 cells, ranging from inverters to D-type flip-flops.
- These cells are then characterized for functionality and timing so that they can be used with synthesis tools. They are also abstracted for use in place and route tools.
- Finally, student teams develop a project using Verilog as a front-end. They use synthesis and place and route tools with their own cells as the target library to implement a complete chip, ready for fabrication.
- As an option, teams can choose to fabricate their chips. This is generously supported by the MOSIS Educational Program [3]. Student chips are fabricated and returned for testing in the following semester.

This "soup to nuts" approach makes for an action-packed semester. I believe that all students benefit from developing their projects to the point where they could be fabricated, even if they don't choose that option in the end. The exercise of making their chip "fab ready" adds a realistic element to the project that really brings home how many details must be attended to in a successful project. I like to tell my students that VLSI design (at some level) isn't really hard, but it is very time consuming. They usually believe me by the end of the semester.

Another saying I like is: "When you've finished 90% of your chip, you only have 90% left to go!"

For the students who decide to send their designs for fabrication, there are additional educational benefits of testing their chips when they are returned. For many students the process of testing their chip is frustrating at first as they convert their simulation test vectors for use on the tester, but it is ultimately satisfying as they verify that their chip is working. Many of those students go on to build small systems around their chips to further demonstrate their function. For other students the testing process demonstrates in a very real way the challenges of designing good tests for simulation, and how assumptions that

are made during simulation can fool you into thinking that things are working. In the end, they usually figure out that the chip is doing exactly what the simulation said it would, but that the behavior is perhaps not exactly what they planned it to be.

Supplemental Information

This book describes a number of data files, scripts, and other bits of information used in various parts of the design flow. These files, other information about the tools, and color versions of all the figures in the book, are available on the book's Web site, **http://www.pearsonhighered.com/brunvand**.
In addition, the Web site has an instructor's section that includes the full **UofU_Digital** cell library used in this book. I've put that library in a separate section so that instructors can choose to either let their students use that predesigned cell library, or have them create their own without seeing the details of an existing library.

Acknowledgements

Many students at the University of Utah have used various versions of this book, and I gratefully acknowledge their patience and their helpful comments. I hope that the book was useful to them as they learned the art of digital VLSI design.

I myself have learned a great deal about chip design from some excellent instructors and colleagues. I designed my first chip in Kent Smith's VLSI class in 1981. At that time we were designing circuits in $5\mu m$ nMOS (we started using CMOS in the follow-on class in 1982) using special integrated circuit design workstations from ComputerVision, saving our designs on nine-track tape, and plotting the layouts on a CalComp ballpoint pen plotter. Our chips were fabricated through the fledgling MOSIS [4] service. Since that time, the feature size of the CMOS process we use in VLSI classes has shrunk by a factor of 10 to $0.5\mu m$, and the feature size of commercial high-performance chips has shrunk by a factor of 100 to $0.045\mu m$ ($45nm$). However, even after those amazing advances in processing technology, the fundamentals of integrated circuit design have not changed all that much, and our class chips are still fabricated through MOSIS.

Note that decreasing the feature size of devices by a factor of 100 corresponds roughly to a factor of 10,000 increase in the number of devices that can be placed in the same area.

I have benefited from associations with such inspirational designers as Randy Bryant, Al Davis, Carl Ebling, Ran Ginosar, David Harris, Reid Harrison, Alan Hayes, Ian Jones, Dick Lyon, Charles Molnar, Mike Parker, Bob Reese, Bob Sproull, Marshall Soares, Ken Stevens, James Stine, Ivan Sutherland, and Allen Tanner. I have also learned a huge amount from my former graduate students whose research involved VLSI design: Gaurav Gulati, John Hurdle, Luli Josephson, Vamshi Kadaru, Ajay Koche, Niti Madan, Sudheesh Madayi, Joe Novak, Bill Richardson, Himanshu Singh, Tom Wolf, and Jung-Lin Yang.

PREFACE

The initial work on putting my class notes into book form was done during a sabbatical leave I spent at Columbia University, and was supported in part by a John R. Park Teaching Fellowship from the University of Utah.

I appreciate the willingness of both Cadence Design Systems, Inc. and Synopsys Inc. to grant me the right to reproduce screenshots from their fine CAD packages. If you are using a different version of the tools than I am in the examples, you might see slightly different windows or sets of menu commands than are shown in this book. However, it should still be a great help to see what the windows look like in general at each step in the process.

The folks at Addison-Wesley/Pearson have been wonderful in this process. I would particularly like to thank my editors Matt Goldstein, Sarah Milmore, and Jeff Holcomb, copyeditor Genevieve d'Entremont, and cover designer Elena Sidorova.

E.B.

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