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David E. Malach
Editor

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PREFACE

Mechanical engineering is an engineering discipline that applies the principles of physics and materials science for analysis, design, manufacturing, and maintenance of mechanical systems. This book covers leading-edge research in a cross-section of fields centering on mechanical engineering including current research data on phonon modeling in semiconductor low dimension structures; reverse engineering techniques; multivariable constrained process control problems; and heterogeneous circuit insights through substrate coupling.

Chapter 1 - This work investigates substrate coupling effects in mixed IC's, especially the perturbations on RF blocks (VCOs, ...).

The design and analysis of fully integrated radiofrequency Voltage Controlled Oscillators (VCOs) are performed. The authors have focused on oscillation frequency, tuning range, phase noise, output power optimization and buffer stage specifications. SiGe(C) heterojunction bipolar transistors have been used for such circuits and produced via monolithic BiCMOS technologies.

First of all, the oscillation frequency sensitivity functions of tuning voltage and bias current and spurious side-bands due to injected noise are extracted to find out some relation between substrate noise and spectrum purity.

In the core of the paper, the authors try to develop quantitative predictions about the phase noise of such oscillators, and to give some new tracks in this field.

Mixed mode simulations are involved by applying a microscopic Drift Diffusion Model to the device, while the rest of the circuit used is governed by the Kirchhoff's laws; these numerical experiments are in very good accordance with the authors' analytical models of the oscillator phase fluctuations.

Moreover, if we consider high voltage devices, compatible with some (Bi)CMOS standard technology, we ought to consider tri-dimensional phenomena, induced by deep trench or transversal silicon via.

One of the key points of this work is also the prediction of substrate cross-talks in mixedsignal circuits. Phenomena that involve substrate parasitic voltage and substrate propagation are discussed.

Another problem field for the designers of complex heterogeneous circuits is to predict the perturbations coming from commutating logical gates, flowing through the substrate to reach some sensitive analog blocks. The authors present an application of a stochastic process model; the digital switching activity is handled as functions defined as Markov Chains. The final goal is to grasp the noise power density of such perturbations.

The necessity of including the actual electrically active defects (GR, deep traps, RTS,...) in microwave devices is demonstrated. Nevertheless, their localization, as well as their effective density or their capture sections, have a strong influence over the electric characteristics of the HBTs. Indeed, the authors' final aim will be to grasp a versatile complete parameterized compact model of such complex circuits.

Chapter 2 - The mathematical model of a steam boiler has been developed, showing the influence of water-wall slagging and superheater fouling on the boiler performance. With traditional methods, operators often are not able to detect the critical build-up of deposits on the specific heating surfaces of the boiler. The mathematical model can be used as a boiler slagging and fouling simulator to monitor the boiler operation when the boiler heating surfaces become covered with ash deposits. In addition, the computer-based boiler performance system, presented in reference [1], has been implemented to provide a quantitative assessment of cleanliness of the surfaces in the furnace and the convective pass. Measurements of temperatures, pressures, flows, and gas composition are used to perform heat transfer analysis in the boiler furnace and evaporator. The on-line measurements of ash deposit loadings can be used to guide sootblower operations for the combustion chamber and steam superheaters. This contributes to the lowering of the medium usage in the sootblowers and an increase of the water-wall lifetime.

Chapter 3 - In this chapter, the authors present the latest research results on phonon modeling in semiconductor low dimensional structures (LDS) and their interactions with electrons. LDS have been used several times in quantum optoelectronic devices like e.g. semiconductor laser and quantum computing devices. In these heterostructures, the electron-phonon interactions, among other interactions, have a crucial rule in relaxation, decoherence and dephasing effects. In order to determine their suitability for device performance, the authors have estimated the electron scattering rates via the emission/absorption of phonons including the one and two-phonon processes and the pure dephasing processes.

Chapter 4 - Advancements in nanotechnology have created the need for efficient means of communication of electrical signals to nanostructures, which can be addressed using low resistance contacts. In order to study and estimate the resistance of such contacts or the resistance posed by the interface(s) in such contacts, standardised test structures and accurate evaluation techniques need to be used. The resistance posed by an interface is quantified using its specific contact resistivity (SCR), and while multiple techniques have been utilised, inaccuracies of such techniques in measuring values of SCR lesser than $10^{-8}~\Omega cm^2$ have been reported. This chapter presents the experimental validation for a new technique for accurate evaluation of low values of SCR, with the ohmic contacts using relevant silicide thin films (titanium silicide TiSi₂ and nickel silicide NiSi). Experimental data for aluminium (Al) to TiSi₂ ohmic contacts and Al/NiSi/doped silicon ohmic contacts are presented.

Chapter 5 - With recent sophisticated developments in modern material fabrication technology, it is now become possible to produce low-dimensional systems that confine carriers in two (quantum wires) or all three (quantum dots) spatial directions. Devices based on quantum wires and quantum dots have shown excellent features. Consequently, and to study the functioning of devices based on nano particles, digital simulation tools are becoming increasingly necessary for design and characterization of integrated circuit

Preface

component to reduce the number of tests in clean room and optimize them. The simulation of devices offers a fast and inexpensive way to check device designs and processes and can provide good guidance for the selection of wire and dot parameters to experimental studies.

Chapter 6 - The wide spread of Information and Communication Technologies (ICTs) characterising the recent competitive scenario is giving rise to the great interest of researchers and practitioners. Many studies are addressed to give answers to different questions concerning, for example, the impact of ICTs on organisations, the role of ICTs in economic development, the opportunities given by ICT adoption in Small- and Medium-sized Enterprises (SMEs) and its performance measurement. This paper contributes to enrich the current literature on the analysis of diffusion of ICTs within as well as across countries. In particular, by using two datasets derived from independent country-specific surveys, it undertakes an international comparison of diffusion of ICT use in Italy and India. Furthermore, the paper focus on a specific kind of firms, namely the small and medium sized firms, which are more delay in adopting ICTs and are also those less studied in the literature.

Chapter 7 - In this paper, a reverse engineering technique oriented to determine the Paris law constants from the analysis of fracture surfaces of round bars is presented. Experimental work is required in order to obtain two experimental crack front shapes, at least, and the number of cycles between them. Then, a three-dimensional automatic crack growth technique based on the finite element method (FEM) is employed to obtain the Paris law constants by comparing experimental and numerical crack shapes. A careful optimisation procedure was previously carried out in order to obtain feasible numerical results.

Chapter 8 - As the concept of sustainability is gradually incorporated into development models, companies are changing the way they view reverse logistics. It is starting to be seen as a potential source of competitive advantage rather than merely a financial burden imposed by legal requirements. This study shows how the application of reverse logistics to the manufacture of television screens and funnels has simultaneously brought about positive environmental, social and economic outcomes. The financial returns obtained were measured by the net present value and the internal rate of return.

Chapter 9 - In every real control loop exist physical limits, security bounds or system dynamic behaviors that constrain the reachable closed-loop performance. In particular, physical and/or technological limitations of actuators give rise to plant input constraints, whilst safety operation regions or non-minimum phase characteristics generally affect the evolution of the controlled variables or system outputs. In a multivariable or MIMO (Multiple-Input Multiple-Output) process, the effects of these constraints are worsened because of the presence of directions associated to input/output vectors and, even more important, the crossed coupling or interactions between the system variables.

This chapter deals with some relevant practical problems of multivariable process control, which are consequence of crossed *interactions*, control *directionality* and input or output *constraints*.

To this end, recently proposed control strategies are unified in a generalized framework to deal with both input and output constraints. The resulting control strategy, which is herein called *sliding mode reference conditioning* (SMRC) technique, makes use of variable structure control (VSC) and sliding modes (SM) related concepts in order to prevent the process from violating its restrictions while minimizing their undesired effects. Sliding regimes are just transiently employed by SMRC over bounding surfaces corresponding to the unavoidable process constraints, and they are confined to an auxiliary reference conditioning

loop in the low-power side of the system. This way of operation permits accomplishing distinctive properties and design methodologies with respect to the conventional applications of VSC and SM.

The chapter is outlined as follows. Firstly, the basic ideas behind SMRC are introduced for systems involving biproper transfer function descriptions, such as proportional or proportional-integral industrial controllers. Then, the methodology analysis and design is extended to deal with strictly-proper systems. This general analysis is performed independently of the type of constraint. From then on, some applications or case studies of practical interest in multivariable control are discussed and results are presented: (i) the preservation of control directionality and full dynamic decoupling even in the presence of actuator saturation, (ii) the limitation of remaining coupling in partial decoupled non-minimum phase processes, and (iii) a way of delimiting the crossed interactions in industrial decentralized or multi-loop control of multivariable processes.

CONTENTS

Preface		vii
Chapter 1	Heterogeneous Circuits Insights through Substrate Coupling: Noises and Parasites Christian Gontrand, Olivier Valorge, Francis Calmon, Jacques Verdier, Mohamed Abouelatta-Ebrahim, Cristian Andrei, José Cruz Nunez –Perez, Maya Lakhdara, Saïda Latreche and Pierre Dautriche	Ĩ
Chapter 2	Monitoring of Ash Fouling and Internal Scale Deposits in Pulverized Coal Fired Boilers Jan Taler, Marcin Trojan and Dawid Taler	91
Chapter 3	Phonons in Low Dimensional Structures V. N. Stavrou and G. P. Veropoulos	133
Chapter 4	Accurate Evaluation of Specific Contact Resistivity of Multi-layered Silicon Based Ohmic Contacts Madhu Bhaskaran, Sharath Sriram and Anthony S. Holland	163
Chapter 5	Modelling and Simulation of Semiconductor Nano Particles Based Devices S. Abdi-Ben Nasrallah and A. Bouazra	185
Chapter 6	Practice of Information and Communication Technology: A Comparison between Indian and Italian SMEs Nunzia Carbonara and Milind K. Sharma	213
Chapter 7	Determination of the Paris Law Constants from Crack Shapes on Fracture Surfaces in Round Bars R. Branco, F. V. Antunes, J. D. Costa, FengPeng Yang and ZhenBang Kuang	231

vi Contents

Chapter 8	The Benefits of a Reverse Logistics Policy: The Case of a Television Manufacturer Fabricio Mendonça, Eduardo Miguez, Rogerio Valle and Kátia Nunes	245
Chapter 9	A Unified Approach to Deal with Multivariable Constrained Process Control Problems Fabricio Garelli, Ricardo J. Mantz and Hernan De Battista	255
Index		275

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Chapter 1

HETEROGENEOUS CIRCUITS INSIGHTS THROUGH SUBSTRATE COUPLING: NOISES AND PARASITES

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ABSTRACT

This work investigates substrate coupling effects in mixed IC's, especially the perturbations on RF blocks (VCOs, ...).

The design and analysis of fully integrated radiofrequency Voltage Controlled Oscillators (VCOs) are performed. We have focused on oscillation frequency, tuning range, phase noise, output power optimization and buffer stage specifications. SiGe(C)

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hetero-junction bipolar transistors have been used for such circuits and produced via monolithic BiCMOS technologies.

First of all, the oscillation frequency sensitivity functions of tuning voltage and bias current and spurious side-bands due to injected noise are extracted to find out some relation between substrate noise and spectrum purity.

In the core of the paper, we try to develop quantitative predictions about the phase noise of such oscillators, and to give some new tracks in this field.

Mixed mode simulations are involved by applying a microscopic Drift Diffusion Model to the device, while the rest of the circuit used is governed by the Kirchhoff's laws; these numerical experiments are in very good accordance with our analytical models of the oscillator phase fluctuations.

Moreover, if we consider high voltage devices, compatible with some (Bi)CMOS standard technology, we ought to consider tri-dimensional phenomena, induced by deep trench or transversal silicon via.

One of the key points of this work is also the prediction of substrate cross-talks in mixed-signal circuits. Phenomena that involve substrate parasitic voltage and substrate propagation are discussed.

Another problem field for the designers of complex heterogeneous circuits is to predict the perturbations coming from commutating logical gates, flowing through the substrate to reach some sensitive analog blocks. We present an application of a stochastic process model; the digital switching activity is handled as functions defined as Markov Chains. The final goal is to grasp the noise power density of such perturbations.

The necessity of including the actual electrically active defects (GR, deep traps, RTS,...) in microwave devices is demonstrated. Nevertheless, their localization, as well as their effective density or their capture sections, have a strong influence over the electric characteristics of the HBTs. Indeed, on our final aim will be to grasp a versatile complete parameterized compact model of such complex circuits.

I. Introduction

First of all, this paper addresses SiGe(C) base bipolar transistor compatible with some industrial silicon-based processes (BiCMOS, essentially 0.35 or 0.25 μm: STMicroelectronics-like) [1,2]. These devices are part of sophistical analog circuits. Mixed Signal IC's design has become a key point for VLSI systems-on-chip. Functional analog blocks like LNAs, VCOs, filters, AD/DA converters are often placed on a die with high speed digital processing elements, composed of a few millions of logic gates. Crosstalk occurs between the noisy digital and the sensitive analog parts of the circuit. Due to various parasitic coupling mechanisms, there is a very possibility that the transient regimes in the digital circuitry of such systems will corrupt the low-level analog signals and seriously compromise the achievable performance.

VCO phase fluctuations have been a sound subject of numerous studies [3,4]. Theoretical insights have been developed in this framework. Simulations have been performed as a check of the prediction of such analytic developments.

Then, we present simply the problem of substrate coupling [5,9] and propose some basic rules associated with a methodology and some tools to quantify and reduce substrate noise in future designs.

Associated tools are presented to quantify the voltage supply ringing, the substrate equivalent resistance, and the analog ground fluctuations.

To go further for handling efficiently the digital noise of (very) large circuits, the more convenient way seems to be statistical; Monte-Carlo procedures are the predilection tool, but it is very time consuming for large ASICs. Another way, simpler, is to introduce the Markov chain theory[10].

Parasitic signals, induced by the digital part can propagate through various ways: power supply grid, signal wires, package pins, bondings, and obviously the silicon substrate.

II. ABOUT DEVICE MODELLING AND CHARACTERIZATION

In the recent years, band gap engineering of Si based materials, e.g., SiGe or SiGeC has raised considerable attention for various device applications [11-13]. Strained SiGe (C) layers are interesting for applications in ultra-fast heterojunction bipolar transistors (HBTs). The principal challenge is to develop silicon based bipolar transistors having cut-off frequencies competing with III-V devices. For SiGeC [14-16], the carbon doping in the base region suppresses undesirable boron diffusion (cf. Figure 1); therefore, high cut off frequency (f_T) and high maximum oscillation frequency (f_{max}) simultaneously required for the digital and analogue integrated circuitry of high speed communication systems could be achieved.

Brief Recalls on the Heterojunction Bipolar Transistor (HBT)

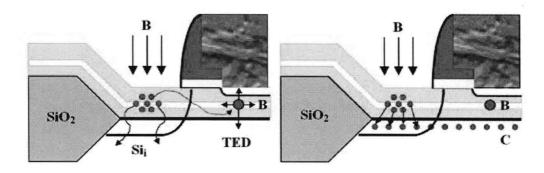
The compressive strain lifts the conduction and valence band degeneracy at band extremes, effectively reducing states and improving the carrier mobility (due to reduction in carrier scattering) with respect to pure Si [17-20].

The base current (holes for the NPN HBT studied below) is known to show a little or no dependence on collector-base bias. It is not affected by the presence of SiGe and it is determined by the injection of holes into the emitter.

Introduction of Germanium in the base offers a new degree of freedom. The presence of the SiGe base material increases collector current, which induces high current gain with low base resistance (because of a higher base doping and a narrow base - cf. high frequency performances, i.e. f_t and f_{max} , corresponding to a reduced base transit -).

The HBT Modelling

We have developed numerical methods for analyzing SiGe heterostructure semiconductor devices, with macroscopic semiconductor equations using the Drift Diffusion Model (DDM) [22,23]. The continuity and transport equations along with Poisson's equation have been employed to describe the electrical characteristics of semiconductor devices. We base our analysis on a macroscopic description of semiconductors with no uniform composition.



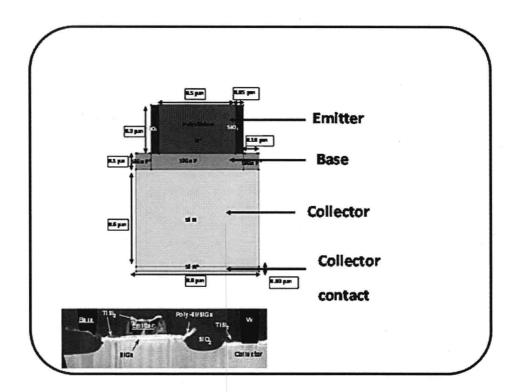


Figure 1.a Schematic cross section of the investigated SiGe (C) Heterojunction Bipolar Transistor integrated in a BiCMOS technology, with a single polysilicon emitter quasi self- Aligned architecture (left: without carbon – TED: Transient Enhanced Diffusion -; right: with carbon). (b). an HBT geometry

Various semiconductors differ in their fundamental properties such as band gap, carrier mobility, effective electron and hole masses. In addition, interfaces between different materials must be properly described. The equations and physical models involved in the simulation of Si BJT and $Si_{1-x}Ge_x$ HBT are implemented in our program.

"SIBIDIF"; (Simulation Bidimensional by Finite Difference) is our 2-D simulator for silicon germanium bipolar device optimization, in finite-difference, developed in previous paper specifically for investigating the SiGe HBTs [23].

As a DDM solver, SIBIDIF solves these partial differential equations for electrostatic potential Φ , and for electron and hole concentration n and p, respectively.

(a) Poisson's equation

$$\nabla^2 \phi = \frac{-q}{\varepsilon_{S/C}} \left[p - n + N_D^+ - N_A^- \right] \tag{1}$$

(b) Continuity equations for electrons and holes

$$\frac{\partial n}{\partial t} = GR_n + \frac{1}{q} \frac{dJ_n}{dx} \tag{2}$$

$$\frac{\partial P}{\partial t} = GR_p - \frac{1}{q} \frac{dJ_p}{dx}.$$
 (3)

(c) Current equations for electrons and holes

$$J_n = -q n \mu_n \frac{d\phi_n}{dx} \tag{4}$$

$$J_p = q p \mu_p \frac{d\phi_p}{dr} \tag{5}$$

 N_D^+ and N_A^- are the ionized impurity concentration. ϵ is the permittivity of the material and q is the magnitude of the charge associated with an electron or hole. The electron and hole current densities are function of carrier concentration, carrier mobilities μ_n and μ_p and quasi Fermi potential for electron and holes, Φ_n and Φ_p .

GR_n and GR_p are respectively the net recombination rates for holes and electrons. The recombination and generation models for the SiGe heterojunction are the same models previously described by the homojunction: the so-called Shockley-Read-Hall model.

$$GR_n = GR_p = \frac{n \cdot p - n_i^2}{\tau_n \left(p + p_i \right) + \tau_p \left(n + n_i \right)}$$
 (6)

For numerical implantation, (1) - (5) are discredited on a 2D – finite difference mesh. E_{FN} and E_{FP} are quasi –Fermi potentials.

$$\phi_n = -\frac{1}{q} E_{FN} \ \phi_p = -\frac{1}{q} E_{FP} \tag{7}$$

$$E_{FN} = E_c + KT \ln \left(\frac{n}{N_c}\right) + KT \ln \gamma_n \tag{8}$$

$$E_{FP} = E_V - KT \ln \left(\frac{p}{N_V}\right) + KT \ln \gamma_p \tag{9}$$

$$\gamma_n = \gamma_p = 1$$
 for Boltzmann statistics (10)

$$E_C = -q\phi + \frac{Eg}{2} \tag{11}$$

$$E_V = -q\phi - \frac{Eg}{2} + \Delta E_V \tag{12}$$

$$\Delta E_{v} = 0.74x \tag{13}$$

This allows heterostructure device simulation capabilities to be easily implemented, and hence permits simulation of graded – base SiGe HBT's.

$$E_{g(SiGe)} = E_{g(Si)} - \Delta E_g \tag{14}$$

$$n_{i(SiGe)} = (N_C N_V)_{SiGe} \exp\left(-\frac{E_{g(Si)}}{KT}\right) \exp\left(\frac{\Delta E_g}{KT}\right)$$
(15)

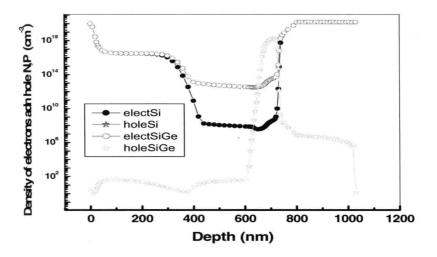
Concerning SiGeC

The available SiGeC Heterojonction Bipolar Transistors (HBTs) exhibit graded Ge and C profiles within the base in order to reduce the base transit time. We use, for instance, a low voltage version dedicated to the RF applications (break-down voltage: BV_{CEO} = 3.3V –, transition frequency: $f_T = 52$ GHz) with a low noise figure of merit (FOM). These transistors have typical performances, for a surface of emitter $A_E = 0.4x12.8~\mu m^2$, a current gain β of around 200, an Early voltage of about 200 V. For this type of HBT, the emitter width, W_E , and the emitter length, L_E , may vary from 0.4 μ m to 1.6 μ m and from 0.8 μ m to 30 μ m respectively, always with $L_E \ge W_E$. Finally, we can use up to 6 base fingers (5 for the emitter and the collector). Therefore, it is important to realize an analysis to keep the best candidate for some oscillator application, where low phase noise and optimal output power are important criterions. High frequency simulations in small signal and low frequency noise study must be done to verify the expected evolutions. These simulations have to be associated to the performance analysis of the oscillator [24]. In our work, the principal HBT used is the

NN232A128 (from STMocroelectronics). It consists of 2 fingers of emitter, 3 of base and 2 of collector. Its emitter width is W_E =A=0.4 μm and its emitter length is L_E =12.8 μm .

According to the passive elements, the technology features 5 metal levels, which makes possible the realization of MIM capacitors and spiral inductors. Inductors are realized with patterned ground shield topography, featuring reasonable quality factor at the frequency of 20 GHz if an optimal value and an appropriate geometry are chosen.

We present on the figure 1.b a cross section of a typical simulated HBT. These electrical simulations have been completed either by ISE [22], or by our own simulator [23], or both.



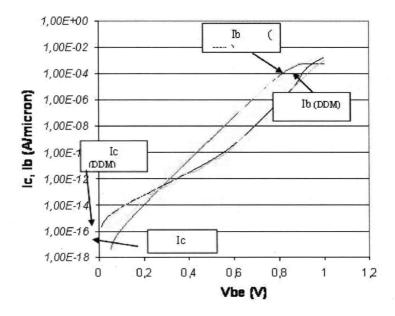


Figure 2.a HBT carrier profiles: Si and SiGe base (same geometry, same doping profiles). (b). Gummel plots (Drift Diffusion Model versus measurements)

To model SiGeC heterostructure, we need appropriate material physical parameters. Depending on Germanium and carbon concentration, the Si_{1-x-y}Ge_xC_y has its material properties different from those of Si, Ge, and C. What is more, these material parameters are to a certain extent affected by strains in SiGeC epitaxial layer. The interfaces between different materials must be properly described.

The band gap energy is dependent not only on Ge mole fraction x in the base and fraction y of carbon, but also on the amount of strain in the base layer, which in turn depends on the type of substrate used. We will assume Si substrate for which band gap varies as eq. 16 [25]: In our simulation, we used 20% of Ge and 0.75% of carbon concentration.

The band gap is modified as follows:

$$Eg_{SiGec}(x) = Eg_{Si} - 0.96x + 0.43x^2 - 0.17x^3 + 3.4y$$
 (16)

It is still beginning discussed how band gap narrowing (BGN) is allocated in SiGeC [26] band, but result suggests that the total band gap reduction for SiGeC materials mainly occurs in valence band as in SiGe as well. So we think that band gap widening effect due to carbon is allocated also, mainly in valence band. Our simulations were done assuming that band gap widening due to carbon is completely allocated in valence band equal to the bandgap reduction (band gap narrowing) ΔEg≅ΔEv [27]. In the Si/Si_{1-x-y}Ge_xC_y/Si n-p-n HBTs, the addition of carbon causes a shift in band gap of +26meV.

The electron and hole densities are presented on figure 2.a along the structure.

Typical Gummel characteristics of a SiGe-base transistor are presented en Figure 2.b. Comparisons between experiments and DDM simulations are in very good accordance.

The influences of Fermi Dirac statistics, needed at low temperatures, on band gap narrowing, are depicted as:

$$\gamma_{n,p} = F^{1/2} \frac{\eta_{n,p}}{\exp(\eta_{n,p})} \quad n_i^2 = \left(N_C \cdot N_V\right) \exp\left(-\frac{E_g}{KT}\right)$$

$$\eta_n = \frac{E_{FN} - E_C}{KT} = F_{1/2}^{-1} \left(\frac{n}{N_C}\right) \quad \eta_p = \frac{E_V - E_{FP}}{KT} = F_{1/2}^{-1} \left(\frac{p}{N_V}\right)$$
(17)

Although an essential aim is to analyze the impact of low temperatures on electrical characteristics of the actual working devices, it is also a good tool for device reliability studies. We report respectively on the Figure 3.a the Gummel plots (base current and collector current) for a SiGeC HBT simulated by SIBIDIF simulator compared for the measurements transistors for an emitter area 0.17x 5.9µm² at the room temperature (T=300K) and at T=150K [14,15]. We note that there is a very good agreement between simulation and measurement results (as well as Early Plots: Figure 3b). We see the reduction of the base current according to the temperature increase; besides, we can note non-idealities on the base current. The thermal current is negligible. The no ideal currents corresponding to mechanisms as recombination or tunnel current are visible at the cryogenic temperatures, but they do not appear at room temperature. Moreover, the augmentation of transductance appears for more significant polarisation (Vbe).