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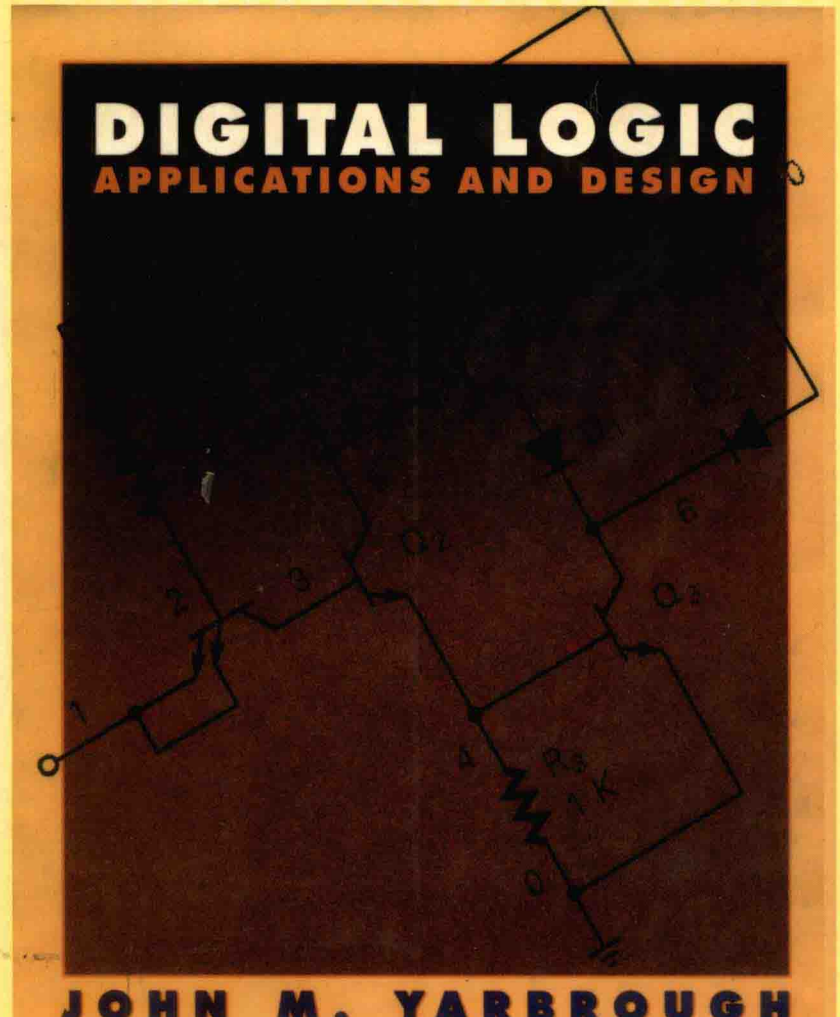
数字逻辑 应用与设计

（英文版）



（美）John M. Yarbrough 著

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数字逻辑 应用与设计 （英文版）

Digital Logic Applications and Design

本书概括了经典的组合与时序逻辑，介绍了PAL、PLA、GAL和EPLD逻辑电路的实现及TTL、ECL和CMOS的电路分析。全书共10章，包括基本原理、数字系统、组合逻辑、时序电路分析与设计、异步时序电路及数字开关电路。

读者对象：

电气、电子计算机和工程技术专业的学生及工程技术人员。

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PREFACE

The purpose of *Digital Logic: Applications and Design* is to provide electrical, electronic, and computer engineering students, and engineering technology students with material fundamental to the design and analysis of digital circuits. It can also be used by practicing engineers, technologists, and technicians or anyone else, for that matter, with a basic science background, for self-study or as a review.

The typical audience might consist of college sophomores taking the first or second of a series of quarter or semester course(s) in digital logic and circuits. The material is comprehensive; that is, it covers classical combinational and sequential logic. It also covers material on PAL, PLA, GAL, and EPLD realization of logic circuits and has a chapter on circuit analysis of TTL, ECL, and CMOS logic families.

There are 10 chapters in the book, starting with basic principles and number systems, continuing on through combinational logic topics, sequential circuit analysis and design, asynchronous sequential circuit material, and ending with coverage of digital switching circuits. The organization of the book is as follows:

Chapter 1 introduces digital concepts, number systems, binary codes, and arithmetic.

Chapter 2 develops logic symbols and Boolean algebra.

Chapter 3 defines combinational logic and the generation of switching equations from truth tables. It continues in the simplification of switching equations using Karnaugh maps, Quine-McClusky, and map-entered variable algorithms.

Chapter 4 continues the treatment of combinational logic with design problems, multiplexers, decoders, adders, subtractors, and arithmetic logic units.

Chapter 5 treats flip-flops, including timing specifications. The chapter continues with simple counters, MSI integrated circuit counters, and registers.

Chapter 6 introduces synchronous sequential circuit design. Included are Mealy and Moore sequential circuit models, state diagram notation, development of transition and excitation tables, and derivation of excitation and output equations. Analysis of synchronous circuits and the design of counters is included.

Chapter 7 continues with such sequential circuit design topics as state equivalence and reduction, state assignment, algorithm state machines, and linked sequential machines.

Chapter 8 develops asynchronous sequential circuit analysis and design. Fundamental and pulse mode circuits are discussed, analysis of asynchronous circuits, derivation of flow tables, state assignment problems, and design examples are included. Some discussion of data synchronizers and mixed-operating mode logic is given.

Chapter 9 introduces memory chips as a means of realizing combinational and sequential circuits. PLD design is discussed and examples given. The chapter also introduces two field programmable gate array (FPGA) architectures; the Xilinx and Actel FPGA devices.

Chapter 10 concludes the text by presenting a fairly comprehensive treatment of digital integrated circuit logic families. Included are discussions of TTL, ECL, and CMOS circuits. In addition, tristate, open collector, and mixed logic subfamily interfacing is presented.

The electronics aspect of digital design and analysis is absent from many texts on digital logic. Combinational and sequential logic design from a strictly logic perspective is, in my view, incomplete. Digital integrated circuits are electronic devices. Factors such as fan-out considerations, power supply current, propagation delay, and timing analysis, all affect the design of working systems. To address the electronics as well as the logic aspects of digital design, the entire book uses actual IC devices. Becoming familiar with the wide array of ICs available to the logic designer is as important as knowing Boolean algebra and state diagram notation. I have attempted to show the internal logic as well as the logic symbols for many of the SSI and MSI devices commonly used.

Even though PLDs, FPGAs, and ASIC devices are the choices of industry logic designers, an understanding of fundamental principles imparted by using standard ICs prepares the student for dealing with ASIC libraries. Once the logic design principles are learned, any FPGA or ASIC design system can be mastered and used. It would be difficult to move directly from Boolean algebra, combinational, and sequential logic design principles into designing circuits using FPGAs and ASIC devices. FPGA and ASIC design platforms and software are still too expensive to find their way into undergraduate curricula. Writing a text using a given hardware platform and design software would necessarily exclude those not using that particular hardware and software combination.

I know that *almost* anyone can connect a series of digital integrated circuits to provide some useful result under ideal conditions. But what about nonideal conditions? The answer is found in Chapter 10 on "Digital Integrated Circuits," whose purpose is to develop the connection between the "logic" and the electronics that implement that logic. For those who have a good transistor circuits background, much of the early part of Chapter 10 can be eliminated by going straight to the specifications and characteristics of the IC themselves. For students more concerned with digital logic as a prelude to computer architecture courses and software, Chapter 10 can be skipped altogether.

COURSE PARTITIONING

Several partitions are possible with the material presented in the book, depending on relative emphasis, length of lecture and laboratory course (quarter or semester), and the amount of credit given. Some examples are shown here.

1. Quarter calendar, three-course sequence with emphasis on circuits as logic. Three lectures and three laboratory courses.
   a. First quarter: 3 credit lecture, 2 credit laboratory.
      Chapter 1. "Digital Concepts and Number Systems"
      Chapter 2. "Boolean Switching Algebra"
      Chapter 3. "Principles of Combinational Logic"
      Chapter 10. "Digital Integrated Circuits" (portions of Chapter 10 may be treated lightly or omitted depending on the emphasis of IC families and transistor circuits)
   b. Second quarter: 3–4 credit lecture, 1–2 credit laboratory.
      Chapter 4. "Analysis and Design of Combinational Logic"
      Chapter 5. "Flip-Flops, Simple Counters, and Registers"
      Chapter 6. "Introduction to Sequential Circuits"
   c. Third quarter: 3–4 credit lecture, 1–2 credit laboratory.
      Chapter 7. "Sequential Circuit Design"
      Chapter 8. "Asynchronous Sequential Circuits"
      Chapter 9. "Programmable Logic and Memory"
2. Semester calendar with the same coverage as given in the three-term course sequence.
   a. First semester.
      Chapter 1. "Digital Concepts and Number Systems"
      Chapter 2. "Boolean Switching Algebra"
      Chapter 10. "Digital Integrated Circuits"
      Chapter 3. "Principles of Combinational Logic"
      Chapter 4. "Analysis and Design of Combinational Logic"
   b. Second semester.
      Chapter 5. "Flip-Flops, Simple Counters, and Registers"
      Chapter 6. "Introduction to Sequential Circuits"
      Chapter 7. "Sequential Circuit Design"
      Chapter 8. "Asynchronous Sequential Circuits"
      Chapter 9. "Programmable Logic and Memory"

Laboratory assignments can be made from selected problems given at the end of each chapter. For example, Chapter 5, "Flip-Flops, Simple Counters, and Registers," might yield the following laboratory assignments:

1. Latches and flip-flops (problems 3, 4, 5, 6, 7, 8, 9)
   a. Construct an S′R′ latch from NAND gates. Verify the characteristic table and derive the characteristic equation.
   b. Add additional NAND gates to convert the S′R′ latch to a level triggered J–K flip-flop. Verify the operation by constructing a characteristic table. Identify the operation when $J = K = 1$. Suggest a solution for the problem encountered (convert the level trigger to a pulse trigger).
   c. Convert the pulse triggered J–K flip-flop to a D flip-flop and a T flip-flop. Verify the operation of each by creating characteristic tables. Derive the characteristic equations.
   d. Predict and measure power consumption and propagation delay.
2. Counters (problem 25)
   a. Design a modulo-8 counter using standard IC flip-flops.
      1. Construct the state diagram.

2. Determine the number of flip-flops needed.
3. Make a binary state assignment (000, 001, 010, 111).
4. Create a state table and a transition table.
5. Using *D* flip-flops create an excitation table (compare the transition and excitation tables).
6. Generate the simplified excitation equations.
7. Construct the circuit using TTL integrated circuit packages (*D* flip-flops, AND, NAND, etc. gates).

b. Predict the timing diagram for the modulo-8 counter.

c. Test the circuit operation.

1. Single step through each state and verify state transitions.
2. Connect a function generator to the clock inputs. Set the function generator to produce a square wave between 0 and 5 V at a frequency of 10 KHz. Measure the *Q* outputs of the flip-flops using an oscilloscope and produce a timing diagram.

3. Johnson counter (problem 26)

4. Special purpose pulse generator (problem 33)

5. Register system (problem 43)

SUPPLEMENTAL PACKAGE

- A solutions manual to all text problems (only odd answers are given in the text)
- For selected text illustrations, a set of transparency masters to use as overheads
- A lab manual is being developed, which is unique because other texts at this level do not have one (ask your West sales representative when it will be available)

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