

国外电子信息精品著作(影印版)

# 集成电路中的电源 完整性分析与管理

**Power Integrity Analysis and  
Management for Integrated Circuits**

**Raj Nair  
Donald Bennett**



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## 内 容 简 介

随着对集成电路工作速度和集成度的要求越来越高,集成电路电源完整性的问题已成为集成电路设计中亟待解决的重要问题及研究热点。本书分四部分对集成电路电源完整性的分析与管理进行研究,全书注意基础、内容详实,由浅入深地对电源完整性的基本理论、建模、设计与分析进行了介绍,使读者能够学会先进的电源完整性管理实现。

本书既可作为学生学习集成电路设计的教科书,也适合研究集成系统开发的工程师使用。

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## 《国外电子信息精品著作》序

20世纪90年代以来，信息科学技术成为世界经济的中坚力量。随着经济全球化的进一步发展，以微电子、计算机、通信和网络技术为代表的信息技术，成为人类社会进步过程中发展最快、渗透性最强、应用面最广的关键技术。信息技术的发展带动了微电子、计算机、通信、网络、超导等产业的发展，促进了生命科学、新材料、能源、航空航天等高新技术产业的成长。信息产业的发展水平不仅是社会物质生产、文化进步的基本要素和必备条件，也是衡量一个国家的综合国力、国际竞争力和发展水平的重要标志。在中国，信息产业在国民经济发展中占有举足轻重的地位，成为国民经济重要支柱产业。然而，中国的信息科学支持技术发展的力度不够，信息技术还处于比较落后的水平，因此，快速发展信息科学技术成为我国迫在眉睫的大事。

要使我国的信息技术更好地发展起来，需要科学工作者和工程技术人员付出艰辛的努力。此外，我们要从客观上为科学工作者和工程技术人员创造更有利于发展的环境，加强对信息技术的支持与投资力度，其中也包括与信息技术相关的图书出版工作。

从出版的角度考虑，除了较好较快地出版具有自主知识产权的成果外，引进国外的优秀出版物是大有裨益的。洋为中用，将国外的优秀著作引进到国内，促进最新的科技成就迅速转化为我们自己的智力成果，无疑是值得高度重视的。科学出版社引进一批国外知名出版社的优秀著作，使我国从事信息技术的广大科学工作者和工程技术人员能以较低的价格购买，对于推动我国信息技术领域的科研与教学是十分有益的事。

此次科学出版社在广泛征求专家意见的基础上，经过反复论证、仔细遴选，共引进了接近30本外版书，大体上可以分为两类，第一类是基础理论著作，第二类是工程应用方面的著作。所有的著作都涉及信息领域的最新成果，大多数是2005年后出版的，力求“层次高、

内容新、参考性强”。在内容和形式上都体现了科学出版社一贯奉行的严谨作风。

当然，这批书只能涵盖信息科学技术的一部分，所以这项工作还应该继续下去。对于一些读者面较广、观点新颖、国内缺乏的好书还应该翻译成中文出版，这有利于知识更好更快地传播。同时，我也希望广大读者提出好的建议，以改进和完善丛书的出版工作。

总之，我对科学出版社引进外版书这一举措表示热烈的支持，并盼望这一工作取得更大的成绩。

A large, bold, black handwritten signature in cursive script, reading '王越' (Wang Yue).

中国科学院院士

中国工程院院士

2006年12月

*To my mother, Urath Shanthakumari, whose devotion to  
her children made me an engineer, and to my children,  
Prathik Rajendran, Rohan Alexander Nair, and  
Hannah Jyothi Nair, whose love and faith in me  
keep me going.*

—Raj Nair

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# P R E F A C E

This book is our earnest and first effort at demystifying power integrity, its detailed analysis, and its management for integrated circuits in the nanometer scale era.

The focus of the book is squarely on integrated circuits and power integrity as it pertains to such components. It is intended both for the student engineer gaining an introduction to the field of integrated circuit design, and for those skilled in the art, developing systems based on integrated components. Hence, every attempt has been made to emphasize basic concepts, principles, and intuitive understanding, while also discussing state-of-the-art and advanced concepts and technologies. This book differs from prior, related efforts at least in that it emphasizes comprehensive, *true-physical* modeling of integrated circuits and systems behavior. Beginning with an intuitive understanding of power integrity in a fundamental, physical sense, through analogies with mechanical systems and their underlying laws, we explore root causes for a rise to predominance of power integrity as a performance differentiator for integrated circuits.

A simple example is helpful in establishing the importance of power integrity to integrated circuits and systems. Today, as integrated systems become increasingly powerful and portable, system and device power and energy consumption is a critical design constraint. But less noticed is power integrity, despite its principal role in determining power consumption. Most of us notice that if we dim the lights in our entertainment rooms too much, sharp changes in brightness of our television screens hurt our eyes. Our attempt to reduce lighting energy

consumption therefore depends directly on the level of light noise we encounter. The very same is true for integrated circuits: minimization of power and energy consumption through supply voltage reduction, a fundamental approach, depends directly on knowing the level of power supply noise, or, in other words, power integrity.

We must nevertheless confess that motivation for this work comes in large part from power integrity studies into high-performance microprocessors rather than from a need to save energy in low-power, system-on-chip components. While engaged in the investigation of technologies for future generations of processor packages, we observed a lack of tools enabling the determination of the spatio-temporal coincidence of power supply noise with critical path activation within circuits. Optimization of the placement of power integrity management components such as package capacitors remains an afterthought in package design. Non-physical approximations such as simplified resistance-capacitance models are commonly employed in the analysis of a chip power distribution network. It is well known that the extraction of key electromagnetic aspects of on-chip interconnect, or resistance, capacitance, and inductance, and simulation of such extracted models with circuit blocks and system-level components, are tasks of high and increasing computational complexity. Hence, optimization of on-chip power grids, circuit block placement, and decoupling capacitance allocation also suffers in quality. More importantly, we see an absence of early, front-end tools for allocation of chip resources such as metal, decoupling capacitance, and external connectivity such as power supply pads with respect to power integrity performance. This constrains quality and degrees of freedom in physical design, often leading to overallocation of chip resources, or excessive iterations of design. With many additional challenges in nanometer-scale fabrication processes, we see this absence of comprehensive, true-physical investigation, and of front-end analysis capability for power integrity, to be significant challenges to continued scaling of integrated devices.

We have therefore endeavored to put into book form our learning and investigations over the past decade into this important aspect of integrated circuit design. Our work in this field has taught us that high levels of abstraction and physics-based modeling and analysis addresses many of the challenges of power integrity. This learning is captured in the book, along with traditional and advanced methods and techniques for power integrity analysis.

While we discuss many necessary aspects of power, power integrity, power supply, and distribution network design, as well as power integrity management,



this book is, quite simply, only an introduction to this complex topic. Discussions within may at times appear to be too brief, or, occasionally, overly laden with details and exemplary illustrations, and at times even appear to be repetitive. While many readers will grasp the principles and theory discussed readily, we believe lay readers will find additional explanations, examples, and reiteration within helpful. Readers of all levels will appreciate some of our exercises designed to invoke thought beyond the teachings of chapter material. The book is meant to provide a fuller understanding of power integrity as it relates to integrated circuits, and strives to focus on derivations from first principles as well as intuitive understanding. Empirical understanding is also provided in places within along with our considered inferences where appropriate.

We humbly opine that as researchers ourselves, we are fallible; we've ventured to discuss concepts in this book that are not yet in common use, which must therefore be applied by our readers after diligent and thorough validation in their work. Skilled practitioners nevertheless will, we believe, find the advanced concepts discussed in this book resonating well with their own efforts, and, on occasion, to be surprising discoveries advancing their learning. For instance, we discuss *differential power distribution* as a "broadband" power supply distribution method. Signal integrity engineers may readily appreciate the similarities that this concept shares with differential signal transmission, which has all but replaced single-ended signaling. We also discuss *active noise regulation*, a technique that dynamically changes network impedance at a power grid junction, enhancing power integrity. These and other concepts and techniques, as for example, *holistic integration*, and the constructive employment of supply undulations to benefit circuit performance through *dynamic timing analysis*, are proposed with confidence but not necessarily with sufficient prior implementation and empirical evidence. We hope readers and researchers will find these concepts as intriguing and enlightening as they have been to us.

## Book Organization

At a high level, the book is organized into four distinct parts. The first part, comprising Chapters 1 to 3, provides a foundational understanding of power integrity, the challenges posed for power and power integrity by relentless scaling, practical aspects of power delivery, and the beneficial application of *total power integrity* to chip physical design optimization. Chapters 4 through 7 form the second part, which focuses on various aspects of power distribution network modeling, design, and analysis. These chapters highlight abstraction and physics-based analysis while

also providing copious discussion of traditional circuit- and field-solver-based techniques. The third part concentrates on floorplanning and implementation of various techniques for power integrity management. Chapters 8 and 9 comprise this part of the book, and discuss advanced power integrity management concepts and implementations. Chapter 10 closes the book with a discussion on integration trends and the consequent challenges for power integrity. Brief descriptions of the individual chapters and recommended reading strategies follow.

Chapter 1, “Power, Delivering Power, and Power Integrity,” employs physical analogies to develop an intuitive understanding of power and aspects of power integrity. For instance, the *force-voltage analogy* is used to relate work done, power, and energy in electrical form to the same quantities in the physical world. Beginning readers in the field will find this chapter helpful in developing an appreciation for power integrity, whereas skilled practitioners may wish to skip the chapter, or skim through it to review and refresh some salient points.

Chapters 2 and 3 are essential segments of the first part of the book, recommended for both beginning experimenters and skilled practitioners of the field. Chapter 2, “Ultra-Large-Scale Integration and Power Challenges,” delves deeply into fundamental aspects of CMOS scaling and *energy-delay*, illustrating through simple derivations differences between *nanoscale* and prior integrated circuit fabrication regimes. This chapter sets a foundation for discussions on *total power integrity* including inductive aspects of chip power grids by demonstrating potential follies ensuing from the exclusion of inductance in signal propagation analysis as it relates to energy and circuit performance. The chapter also derives scaling-driven relationships for power integrity and system aspects that influence it directly. Chapter 3, “IC Power Integrity and Optimal Power Delivery,” discusses power delivery and IC power distribution, and in particular, details *distributed voltage regulation* as well as a connection between switched, efficient power conversion and scaling. These chapters firmly establish the significance of on-chip inductance to chip power grid design, and provide methods for its incorporation into power integrity analysis.

Chapters 4 through 7, recommended for readers of all skill levels in the field, discuss various techniques for power distribution network modeling and analysis in much detail. Chapter 4, “Early Power Integrity Analysis and Abstraction,” details *front-end analysis* and abstraction based chip and power distribution network modeling. Chapter 5, “Power Integrity Analysis and EMI/EMC,” begins with a detailed description of traditional power distribution network modeling and impedance management, discusses modeling methods and numerical analysis, and

establishes the importance of, and accuracy in, 3D field-solver-based methodologies. The chapter then illustrates the application of such analysis methods to exploring the close relationship between power integrity and electromagnetic radiation in chip packages. It again highlights the need for comprehensive, system-level, and early analysis of power integrity as well as EMI. Chapter 6, “Power Distribution Modeling and Integrity Analysis,” presents a modeling technique that employs distributed *RLC* elements for accurate and efficient on-chip power distribution analysis, and applies the technique to a case study demonstrating the effects of different power supply noise reduction techniques. Chapter 7, “Effective Current Density and Continuum Models,” describes a novel modeling method that permits the abstraction of a power distribution grid into a continuum model of greatly reduced computational complexity. The chapter includes numerous illustrative examples demonstrating benefits of abstraction-based modeling in chip floorplanning, and compares a continuum model-based simulator with SPICE.

Chapters 8 and 9 combine state-of-the-art and advanced methodologies and concepts developed in the industry for power and power integrity management, as well as power-integrity-aware floorplanning. Chapter 8 in particular focuses on chip floorplanning and design with power integrity awareness, and discusses the impact of power management techniques on power integrity. Chapter 9 details chip- and package-level power integrity management techniques, exploring advanced techniques such as decoupling capacitance *channel length design*, triple-well fabrication processes, *voltage-dependent capacitance*, and *active packaging*. These chapters are recommended reading for practicing and experienced engineers.

Chapter 10 forms a brief, closing segment of the book, discussing advanced technologies and trends for continued device scaling and electronics integration. Readers will find ample evidence for integration moving into the third dimension through silicon and packaging technologies in this chapter. Integration driven by miniaturization and cost-reduction requirements is described in detail, with implications to power, heat, and power integrity challenges highlighted.

## Supporting Material

Appendices included in the book assist by providing further detail for derivations or theory in the more mathematical chapters of the book. Appendix A is the complete derivation of the *Effective Current Density* based continuum modeling approach to conducting grids. Appendix B provides a derivation of the Helmholtz equation for planar circuits.

Internet links dispersed throughout the book are intended to provide readers with ready access to advanced simulation results visualization as well as online reference documents. In like manner, footnotes throughout all chapters provide readers with ready clarification of uncommon terms or concepts.

The continuum model based power grid simulator employing abstraction for chip power grid, circuit blocks, and capacitance, RLCSim.exe, is freely available from Anasim at the web link: <http://www.anasim.com/category/software/>. This Microsoft Windows compatible software comes with a manual and a set of examples including some experiments of Chapter 4.

### **Further Learning**

Other texts in this area, listed early among the references in Chapter 9, provide excellent treatment of printed circuit boards, planes, passive components, transmission lines, and related circuit behavior. We hope that our unwavering focus on integrated circuits and power integrity in this book will complement these other works well, while paving the way for further investigations into advanced analysis methods and power integrity management. Advancement in power integrity modeling and analysis capability as discussed within will be key to facilitating sustainable, 3D, and holistic integration in the nanoscale regime. It is with this belief that we offer our work and learning to you as stepping stones to further learning and accomplishment.

*Raj Nair*  
*Donald Bennett*  
Anasim Corporation

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# A C K N O W L E D G M E N T S

This book effort came to life after much contemplation of a request from Bernard Goodwin, Publishing Partner at Pearson Education. We thank him for initiating the effort, and for his able support and guidance. Many leading experts reviewed our book proposal and helped improve the book's quality. We thank Eric Bogatin of Bogatin Enterprises, Steve Weir of Teraspeed Consulting, Michael Kozicki of the Arizona State University, Vijay Nair of Intel Corporation, Seth Wolpert of Penn State University, and Dave Cuthbert for their critical reviews of the book proposal. We wish to gratefully acknowledge diligent and constructive chapter reviews from Michael Kozicki and Paul Aiken of the University of the West Indies/UTech, and comments from an unnamed reviewer that helped shape book chapters into their current form.

Contributions in the form of chapters or sections of chapters from a number of area experts in the industry and academia have greatly enhanced the book's content. Masanori Hashimoto of Osaka University, Japan, and Navin Srivastava of Mentor Graphics contributed key sections of Chapter 3. Swagato Chakraborty, Dipanjan Gope, and Vikram Jandhyala of Physware Inc., Mosin Mondal at the University of Washington, and Souvik Mukherjee, Woopoung Kim, and Rajen Murugan of Texas Instruments contributed Chapter 5. Li-Rong Zheng of the Swedish Royal Institute of Technology (KTH), and Sampo Tuuna at the University of Turku, Finland, contributed Chapter 6. Shane Stelmach and Snehamay Sinha of Texas Instruments contributed Chapter 7. Masanori Hashimoto additionally contributed a key section of Chapter 9. Leo Mathew of the University of

Texas at Austin, and Mario A. Bolaños of Texas Instruments contributed the multi-gate transistor and packaging sections of Chapter 10, respectively. These contributions are most gratefully acknowledged. It is Rajen Murugan's initiative and leadership that brought about many of the contributions to Chapters 5, 8, and 10. We thank him and Texas Instruments for the keen interest, valuable time, and result-oriented efforts put into our book. It has been a distinct honor for us to have worked with such a distinguished team of contributors.

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Our near and dear ones have, without complaint, shared the burden of this effort, and have our heartfelt gratitude for their patience and unquestioning support.

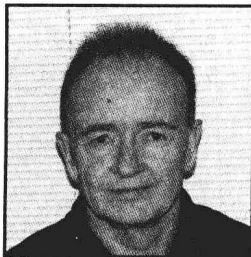
*Raj Nair*  
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## A B O U T   T H E   A U T H O R S



**Raj Nair** has more than twenty-two years of engineering and research experience in the industry and academia and holds over forty patents in VLSI Design and general electronics. He has conducted extensive investigations into power delivery and integrity management at the electronic system, circuits, and device levels, of which the most notable is his work at Intel Corporation, where he researched and conceived of integrated CMOS voltage regulation for microprocessor power integrity management. Raj founded ComLSI, Inc., and Anasim Corp., where he worked on developing advanced, patented techniques and tools for ULSI power integrity analysis and management, and consults in the areas of power integrity and IC design.



**Dr. Donald Bennett**, a device physicist and veteran of the semiconductor industry, co-founded Anasim Corp. with Raj Nair. Donald is the inventor of the patent-pending Effective Current Density method facilitating high levels of abstraction and physics based simulations for integrated circuit and system power integrity analysis. Prior to Anasim, he founded QuantumDA, Inc., developing and deploying RLCSim, a grid simulation software employing the ECD method.

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## C O N T R I B U T O R S

**Mario A. Bolaños:** Mario Bolaños has more than thirty years' experience in semiconductor packaging and is the strategic packaging research and university collaborations manager at Texas Instruments' packaging organization. This organization is responsible for researching new, pathfinding packaging technology for TI. Mario is the author of ten patents, numerous technical papers, and keynote speeches around the world. He received his B.S. in electrical engineering at Jesuit University (UCA) in El Salvador in 1976, and a Master's degree from the University of Texas at Dallas in 1995.

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**Leo Mathew:** Leo has a Bachelor's degree from the Government College of Technology, Coimbatore, India, and a Master's degree from Arizona State University in 1992. From 1992 to 2007, he designed and developed various device technologies at Motorola and Freescale. He is the co-founder and CTO of Astrowatt, and co-founder of Applied Novel Devices. He has forty issued patents, and was the EE Times *Innovator of the Year* in 2006.

**Mosin Mondal:** Mosin Mondal received his Ph.D. in electrical engineering from the University of Washington, Seattle. He received his M.S. and B.E. from Rice University and Jadavpur University, India, respectively. He was a member of technical staff with Cadence Design Systems, India, from 2001 to 2004. His research interests include power and signal integrity, circuit-EM simulation, interconnect modeling, and CAD for VLSI systems. He has published more than twenty papers in journals and conferences.

**Souvik Mukherjee:** Dr. Souvik Mukherjee obtained his Bachelor of Technology in electrical engineering from the Indian Institute of Technology (IIT), Kharagpur, India, in 2002, and his M.S. and Ph.D. from the Georgia Institute of Technology in