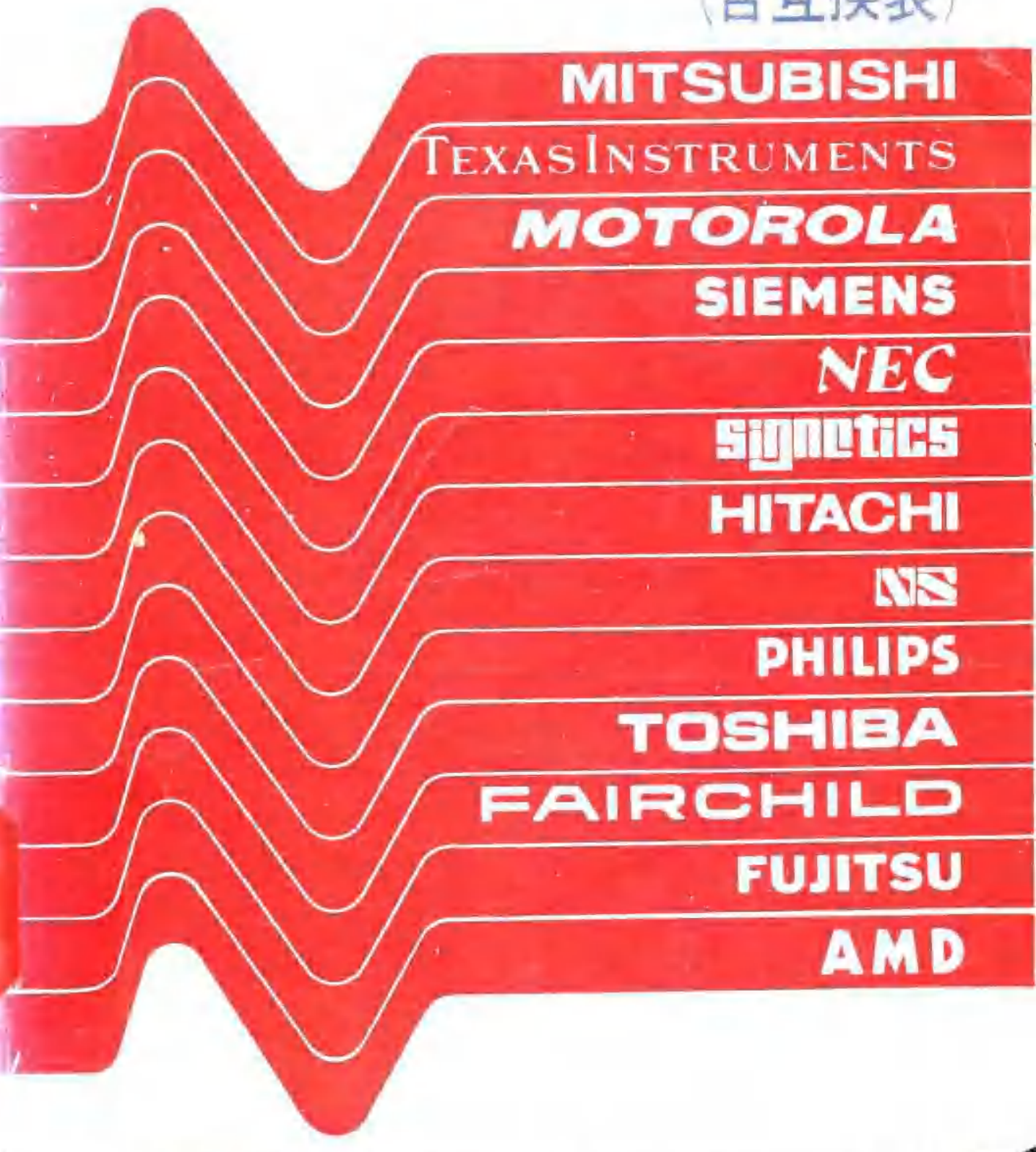
全世界TTL IC特性手册

THE WORLD TTL, IC DATA & CROSS-REFERENCE GUIDE

（含互换表）



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全世界TTL IC特性手册

（含互換表）

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序　言

自從半導體被發明以後，電子技術有着驚人的進步，特別是以縮小空間，增加集積度爲背景而誕生的積體電路 (Integrated circuit, IC) 使得電子工業界朝着經濟化、小型化及功能化而邁進，如此發展的結果，目前半導體已繼續發展到第 3 代。

積體電路中，數位的TTL(Transistor-Transistor-Logic) 積體電路具有種類繁多，信賴性高，性能佳，經濟性優良等特性，因此不僅電子工業，連其他相關工業的機器均樂於大量採用。

各製造公司販賣中的數位 TTL 積體電路之型名、規格等，雖儘量力求統一，但是尚有一段距離，因此在維護、修理各種數位儀器或設計各種電子電路時，均須具備各廠家的資料手冊，非常麻煩。在此，我特地把世界上主要的TTL積體電路之規格，綜合起來，編成TTL積體電路互換表，以德州儀器公司主要的TTL積體電路之規格爲主，作爲從事電子技術者的參考。

本書記載以外的數位 TTL 積體電路尚有很多，因篇幅關係，不得不割愛，此外 TTL 以外的積體電路也非常多，我想下次有機會再另外編書整理。

本書給予從事電子儀器之維護修理者及欲知各廠家之 TTL 積體電路規格之互換者提供很大的幫助，希望讀者能具備一冊，置於案頭加以利用。

最後，謹對於提供許多寶貴資料給我的德州儀器公司亞洲總代理的山城進及秋山洋一兩位先生致最深的謝意，同時感謝德州儀器公司及各廠家提供許多資料讓我引用。

芝浦工業大學　加藤剛正

感謝您

感謝您選購全華圖書！

希望本書能滿足您求知的慾望！

圖書之可貴在其量也在其質

量指圖書內容充實、質指資料新穎够水準，我們就是本著這個原則，竭心盡力地爲國家科學中文化努力貢獻給您這一本全是精華的全華圖書。

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PRACTICAL GUIDE

(使用指導)

PRACTICAL GUIDE (使用指導)

本資料手冊主要的部份爲互換表及資料單，互換表係以德州儀器公司(T.I.) 之數位TTL積體電路爲主體，與世界上代表的12家廠商製造的數位積體電路列爲一互換表。

而資料單係以 T.I. 公司的數位TTL積體電路爲代表，記載其電氣上的特性及接腳分配圖、功能表、電路圖、功能方塊圖等

這13家廠商之IC，其互換性係以電路功能、接腳分配、主要電氣特性、溫度範圍爲主，其他電氣上的特性、溫度範圍及電路圖之細節並不一定完全相同，使用時，只要針對其使用用途，確定兩者之規格完全相同，即可互換使用。

最後，如互換後，若有產生不良之後果，敬請原諒。

各廠家記載之規格如需要更詳細的資料，請與下列公司連絡。

TEXAS INSTRUMENTS	03 (498) 2111	德州儀器公司
FAIRCHILD	03 (400) 8351	日本快捷半導體公司
MOTOROLA	03 (440) 3311	日本摩托羅拉公司
N.S.C.	03 (358) 0781	日本ジャパン
PHILIPS	03 (435) 5339	日本菲立普公司
SIGNETICS	03 (230) 1521	日本SIGNETICS公司
SIEMENS	03 (490) 2181	日本西門子公司
FUJITSU	03 (216) 3211	日本富士通公司
HITACHI	03 (270) 2111	日立公司 (日本)
MITSUBISHI	03 (218) 3367	三菱電機公司 (日本)
NEC	03 (453) 5511	日本電氣公司 (日本)
TOSHIBA	03 (501) 5411	東芝電氣公司 (日本)
A.M.D.	03 (329) 2751	Advanced Micro Devices公司 (美國)

PRACTICAL GUIDE（使用指導）

○Cross-Reference Table Guide（交叉參考表指引）

Example：

	Schottky TTL					High-Speed TTL					Low-Power Schottky TTL					Standard TTL					Low-Power TTL				
	Device Type	Package				Device Type	Package				Device Type	Package				Device Type	Package				Device Type	Package			
		C	P	M	CF		C	P	M	CF		C	P	M	CF		C	P	M	CF		C	P	M	CF
T.I.	SN54S00	J①	N①		W①	SN54H00	J①			W①	SN54LS00	J①			W①	SN5400	J①			W②	SN54L00	J①	N①	T②	
	SN74S00	J①	N①			SN74H00	J①	N①			SN74LS00	J①	N①			SN7400	J①	N①			SN74L00	J①	N①	T②	
	3	4				3	4				3	4				3	4				3	4			

1

1 Manufacturer（製造商）

T.I.	Texas Instruments Incorporated 德州儀器公司（美國）
FAIRCHILD	Fairchild Semiconductor 快捷半導體公司（美國）
MOTOROLA	Motorola Semiconductor Products Inc. 摩托羅拉公司（美國）
N.S.C.	National Semiconductor 國際半導體公司（美國）
PHILIPS	Philips Gloelampenfabrieken, Eindoven 菲立普公司（荷蘭）
SIGNETICS	Signetics Corporation SIGNETICS公司（美國）
SIEMENS	Siemens Aktiengesellschaft 西門子公司（西德）
FUJITSU	富士通公司（日本）
HITACHI	日立公司（日本）
MITSUBISHI	三菱電機公司（日本）
NEC	日本電氣公司（日本）
TOSHIBA	東芝電氣公司（日本）
A.M.D.	Advanced Micro Devices公司（美國）

2 Classification of TTL（TTL的種類）

Schottky TTL（蕭特基TTL）
High-Speed TTL（高速TTL）
Low-Power Schottky TTL（低功率蕭特基TTL）
Standard TTL（標準TTL）
Low-Power TTL（低功率TTL）

3 Device Type（型號）

Upper Side 上段：Military Use（上段：軍用
Lower Side 下段：Commercial／Industry Use（下段：民生／工業用

4 Package Type（包裝型式）

C：Ceramic Dual In-Line Package（陶質，並行接腳包裝）
P：Plastic Dual In-Line Package（塑膠，並行接腳包裝）
M：Metal Flat Package（金屬，平面接腳包裝）
CF：Ceramic Flat Package（陶質，平面接腳包裝）

The digit number in package sections refer to the figured number in the Pin Assignments.
（包裝部份之數字號碼是表示其接腳安排之圖形號碼。）

○Data Sheet Guide（資料表指引）

In this book, the each technical data used on the individual data sheet is that of Texas Instruments Digital TTL Integrated Circuits and the each device type for the individual data sheet represents as follows:

（本書中，各個資料表中所使用的每一個技術資料都是以德州儀器的數位TTL積體電路爲主，且各個資料表的每一裝置之型式表示如下：）

Example：Electrical Characteristics SN5400／SN7400

LETTER SYMBOLS, TERMS, AND DEFINITIONS

(文字記號、術語、定義)

LETTER SYMBOLS, TERMS, AND DEFINITIONS

(文字記號，術語，定義)

VOLTAGES

V_{IH} High-level input voltage 輸入高電位

An input voltage level within the more positive (less negative) of the two ranges of values used to represent the binary variables. A minimum value is specified which is the least-positive (most-negative) value of high-level input voltage for which operation of the logic element within specification limits is guaranteed

V_{IL} Low-level input voltage 輸入低電位

An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables. A maximum value is specified which is the most-positive (least-negative) value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{T+} Positive-going threshold voltage 輸入端由低電位升爲高電位之工作點

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, V_T .

V_{T-} Negative-going threshold voltage 輸入端由高電位降爲低電位之工作點

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V_{T+}.

V_{OH} High-level output voltage 輸出高電位

The voltage at an output terminal for a specified output current I_{OH} with input conditions applied that according to the product specification will establish a high level at the output.

V_{OL} Low-level output voltage 輸出低電位

The voltage at an output terminal for a specified output current I_{OL} with input conditions applied that according to the product specification will establish a low level at the output

V_O(on) On-state output voltage 狀態之輸出電壓

The voltage at an output terminal for a specified output current with input conditions applied that according to the product specification will cause the output switching element to be in the on state

Note: This characteristic is usually specified only for outputs not having internal pull-up elements.

V_O(off) Off-state output voltage 狀態之輸出電壓

The voltage at an output terminal for a specified output current with input conditions applied that according to the product specification will cause the output switching element to be in the off state.

Note: This characteristic is usually specified only for outputs not having internal pull-up elements.

CURRENT

I_{IH} High-level input current 高電位輸入電流

The current flowing into* an input when a specified high-level voltage is applied to that input.

I_{IL} Low-level input current 低電位輸入電流

The current flowing into* an input when a specified low-level voltage is applied to that input

I_{OH} High-level output current 高電位輸出電流

The current flowing into* the output with a specified high-level output voltage V_{OH} applied

Note. This parameter is usually specified for open-collector outputs intended to drive other logic circuits.

I_O(off) Off-state output current 狀態之輸出電流

The current flowing into* an output with a specified output voltage applied and input conditions applied that according to the product specification will cause the output switching element to be in the off state.

Note: This parameter is usually specified for open-collector outputs intended to drive devices other than logic circuits or for three-state outputs.

I_{OS} Short-circuit output current 輸出短路電流

The current flowing into* an output when that output is short circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential)

I_{CCH} Supply current, output(s) high 輸出高電位時之電源供給電流

The current flowing into* the V_{CC} supply terminal of a circuit when the reference output(s) is (are) at a high-level voltage.

I_{CCL} Supply current, output(s) low 輸出低電位時之電源供給電流

The current flowing into* the V_{CC} supply terminal of a circuit when the reference output(s) is (are) at a low-level voltage.

* Current flowing out of a terminal is a negative value

LETTER SYMBOLS, TERMS, AND DEFINITIONS

(文字記號，術語，定義)

DYNAMIC CHARACTERISTICS

f_{max} Maximum clock frequency 最高工作頻率
The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause a change of output state with each clock pulse

t_{HZ} Output disable time (of a three-state output) from high level 三態輸出由高電位到不動作所需時間
The time between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined high level to a high-impedance (off) state.

t_{LZ} Output disable time (of a three-state output) from low level 三態輸出由低電位到不動作所需時間
The time between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined low level to a high-impedance (off) state

t_{PLH} Propagation delay time, low-to-high-level output 輸出由低電位至高電位之傳輸延遲時間
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

t_{PHL} Propagation delay time, high-to-low-level output 輸出由高電位至低電位之傳輸延遲時間
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

t_{TLH} Transition time, low-to-high-level output 輸出由低電位至高電位之轉換時間
The time between a specified low-level voltage and a specified high-level voltage on a waveform that is changing from the defined low level to the defined high level

t_{THL} Transition time, high-to-low-level output 輸出由高電位至低電位之轉換時間
The time between a specified high-level voltage and a specified low-level voltage on a waveform that is changing from the defined high level to the defined low level

t_w Average pulse width 平均脈衝寬
The time between 50-percent-amplitude points (or other specified reference points) on the leading and trailing edges of a pulse.

t_{hold} Hold time 持續時間
The time interval for which a signal or pulse is retained at a specified input terminal after an active transition occurs at another specified input treminal.

$t_{release}$ Release time 釋放時間
The time interval between the release from a specified input terminal of data intended to be recognized and the occurrence of an active transition at another specified input terminal.

Note When specified, the interval designated "release time" falls within the setup interval and constitutes, in effect, a negative hold time

t_{setup} Setup time 設置時間
The time interval for which a signal is applied and maintained at a specified input treminal before an active transition occurs at another specified input terminal

t_{ZH} Output enable time (of a three-state output) to high level 三態輸出由不動作至高電位所需時間
The time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined high level.

t_{ZL} Output enable time (of a three-state output) to low level 三態輸出由不動作至低電位所需時間
The time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined low level.

CLASSIFICATION OF CIRCUIT COMPLEXITY 依電路複雜性而分類

Gate equivalent circuit 閘等值電路
A basic unit-of-measure of relative digital-circuit complexity. The number of gate equivalent circuits is that number of individual logic gates that would have to be interconnected to perform the same function.

LSI Large-scale integration 大型積體電路
A concept whereby a complete major subsystem or system function is fabricated as a single microcircuit. In this context a major subsystem, or system whether logical or linear, is considered to be one that contains 100 or more equivalent gates or circuitry of similar complexity.

MSI Medium-scale integration 中型積體電路
A concept whereby a complete subsystem or system function is fabricated as a single microcircuit. The subsystem or system is smaller than for LSI, but whether digital or linear, is considered to be one that contains 12 or more equivalent gates or circuitry of similar complexity.

SSI Small-scale integration 小型積體電路
Integrated circuits of less complexity than medium-scale integration (MSI).

NOMENCLATURE OF TTL INTEGRATED CIRCUITS

（數位TTL積體電路之命名法）

NOMENCLATURE OF TTL INTEGRATED CIRCUITS
(數位TTL積體電路之命名法)

TEXAS INSTRUMENS

Examples : SN 74 LS 195 A J
(1) (2) (3) (4) (5) (6)

SN 2 9000 N
(1) (2) (4) (6)

(1) SN : Standard Prefix of TEXAS INSTRUMENTS
(德州儀器公司標準字首)

(2) Operating Temperature Range (動作溫度範圍)
54 : −55°C 至 +125°C 2 : 0°C 至 +75°C
74 : 0°C 至 +70°C 3 : −55°C 至 +125°C

(3) Classification of TTL (TTL之分類)
54S 74S : Schottky TTL 蕭特基TTL
54H 74H : High Speed TTL 高速TTL
54LS 74LS : Low Power Schottky TTL 低功率蕭特基TTL
54 74 : Standard TTL 標準TTL
54L 74L : Low Power TTL 低功率TTL

(4) Consecutive Numbers to Indicate the Each Type
(表示各種類之一連續數字編號)

(5) Alphabet : Series Improved
(表示改良型之一連續文字符號)

(6) Package Type (包裝型式)
J : Ceramic Dual In Line Package
陶瓷並行接腳包裝型式
N : Plastic Dual In Line Package
塑膠並行接腳包裝型式
F : Metal Flat Package
金屬平面接腳包裝型式
W : Ceramic Flat Package
陶瓷平面接腳包裝型式

MOTOROLA

Example : MC 74 91 A P
(1) (2) (3) (4) (5)

(1) MC : Prefix of MOTOROLA MC Number Series
(摩托羅拉公司 MC編號序列字首)

(2) Operating Temperature Range (動作溫度範圍)
MC54XX : −55°C 至 +125°C MC9XXX : −55°C 至 +125°C
MC74XX : 0°C 至 +70°C MC8XXX : 0°C 至 +75°C
MC31XX : −55°C 至 +125°C
MC30XX : 0°C 至 +75°C

(3) Consecutive Numbers to Indicate the Each Type
(表示各別種類之一連續數字編號)

(4) Alphabet : Series Improved
(表示改良型之一連續文字編號)

(5) Package Type (包裝型式)
L : Ceramic Dual In Line Package
(陶瓷並行接腳包裝型式)
P : Plastic Dual In Line Package
(塑膠並行接腳包裝型式)
F : Ceramic Flat Package
(陶瓷平面接腳包裝型式)

FAIRCHILD

Example : F 9310 D C
(1) (2) (3) (4)

Note : In this book type description for FAIRCHILD TTL Integrated Circuits is as follows

注意 : (本書所記載之FAIRCHILD 公司TTL積體電路係以下列方式表示)

Example : F C 9310 D
(1) (4) (2) (3)

(1) F : Prefix of FAIRCHILD (快捷公司字首)

(2) Classification of TTL (TTL之分類)
54S 74S 系列 : Schottky TTL 蕭特基TTL
54H 74H 系列 : High Speed TTL 高速TTL
54 74 系列 : Standard TTL 標準TTL
9000 系列 : Medium Speed SSI 中速SSI 93S00 系列 : Schottky MSI 蕭特基MSI
9S00 系列 : Schottky SSI 蕭特基SSI 9300 系列 : Standard MSI 標準MSI
9H00 系列 : High Speed SSI 高速SSI 93L00 系列 : Low Power MSI 低功率MSI
9N00 系列 : Standard SSI 標準SSI 9600 Series : Monostable SSI 單穩態SSI
9L00 系列 : Low Power SSI 低功率SSI 93400 Series : Memory Elements 記憶元件

(3) Package Type パッケージの型
D : Ceramic Dual In Line Package
(陶瓷並行接腳時包裝型式)
P : Plastic Dual In Line Package
(塑膠並行接腳包裝型式)
F : Flat Package
(平面接腳包裝型式)

(4) Operating Temperature Range (動作溫度範圍)
C : Commercial Industrial 0°C to +70°C (or 75°C)
M : Military −55°C to +125°C

NATIONAL SEMICONDUCTOR

Example : DM 74 L 165 A N
(1) (2) (3) (4) (5) (6)

(1) DM : "Digital" Monolithic TTL of NATIONAL SEMICONDUCTOR
(NS公司單晶數位TTL積體電路字首)

(2) Operating Temperature Range (動作溫度範圍)
DM 54XX : −55°C 至 +125°C
DM 74XX : 0°C 至 + 70°C
DM 9XXX : −55°C 至 +125°C
DM 8XXX : 0°C 至 − 70°C (or 75°C)

(3) Classification of TTL (TTL之分類)
S : Schottky TTL 蕭特基TTL
H : High Speed TTL 高速TTL
(空白) : Standard TTL 標準TTL
L : Low Power TTL 低功率TTL

(4) Consecutive Numbers to Indicate the Each Type
(表示各別種類之一連續數字編號)

(5) Alphabet : Series Improved
(表示改良型之一連續文字編號)

(6) Package Type (包裝型式)
D : Glass Metal Dual In Line Package
(玻璃 / 金屬並行接腳包裝型式)
F : Flat Package (0.25" wide)
平行接腳包裝型式(0.25"寬)
J : Glass Glass Dual In Line Package
平行接腳包裝型式(0.275"寬)
N : Molded Dual In Line Package
(玻璃 / 玻璃並行接腳包裝型式)
W : Flat Package (0.275" wide)
(塑膠包裝型式)

NOMENCLATURE OF TTL INTEGRATED CIRCUITS
(數位TTL積體電路之命名法)

PHILIPS

Example : FJ H 13 1
(1) (2) (3) (4)

(1) Digital Family Types of PHILIPS
FJ : FJ族
GJ : GJ族

(2) Circuit Function (電路功能)
H : Combinational Circuit 組合邏輯電路
J : Bistable or Multistable Sequential Circuit 双穩或多穩順序電路
K : Monostable Sequential Circuit 單穩順序電路
L : Level Converter 位準轉換電路
Y : Miscellaneous 其他種類電路

(3) Consecutive Numbers to Indicate the Each Type
(表示各種類之一連續數字編號)

(4) Operating Temperature Range (動作溫度範圍)
1 0°C to +70°C or Wider

(5) Classification of Package (包裝分類)
14 Lead Plastic Dual In-Line Package (Type A)
14脚塑膠並行接脚包裝型式 (A類)
16 Lead Plastic Dual In-Line Package (Type B)
16脚塑膠並行接脚包裝型式 (B類)
24 Lead Ceramic Dual In-Line Package
24脚陶瓷並行接脚包裝型式

SIGNETICS

Example : N74 S 00 F
(1) (2) (3) (4)

(1) Operating Temperature Range (動作溫度範圍)
S84 : −55°C to +125°C (軍用)
N74 0°C to +70°C (工業用)

(2) Classification of TTL (TTL之分類)
S : Schottky TTL 蕭特基TTL
H : High-Speed TTL 高速TTL
(空白) : Standard TTL 標準TTL

(3) Consecutive Numbers to Indicate the Each Type
(表示各種類之一連續數字編號)

(4) Package Type (包裝型式)
F 14-16 Pin Ceramic Dual In-Line Package
(14—16脚並行接脚陶瓷包裝型式)
F 24-Pin Ceramic Dual In-Line Package
(24脚陶瓷包裝型式)
A 14-Pin Dual In-Line Silicon Package
(14脚並行接脚矽質包裝型式)
B : 16 Pin Dual In-Line Silicon Package
(16脚並行接脚矽質包裝型式)
N : 24-Lead Dual In-Line Silicon Package
(24脚並行接脚矽質包裝型式)
Q : 24-Pin Ceramic Flat Package
(24脚陶瓷平面接脚包裝型式)
W 14-16 Pin Flat Ceramic Package
(14—16脚陶瓷平面包裝型式)

SIEMENS

Example : FL H 29 1 U
(1) (2) (3) (4) (5)

(1) FL : TTL Digital Family of SIEMENS
(西門子公司TTL數位積體電路字首)

(2) Circuit Function (電路功能)
H : Combinatorial Circuit 組合近輯電路
J : Bistable or Multistable Sequential Circuit 双穩或多穩順序電路
K : Monostable Sequential Circuit 單穩順序電路
L : Level Converter 位準轉換電路
O : Read/Write Memory Circuit 讀/寫記憶電路
Y : Miscellaneous Circuit 其他種類電路

(3) Consecutive Numbers to Indicate the Each Type
(表示各種類之一連續數字編號)

(4) Operating Temperature Range (動作溫度範圍)
1 0°C to +70°C or Wider

(5) Modification (變形)

Package : Plastic Dual In-Line Package
包裝去 : 塑膠並行接脚包裝型式

FUJITSU

Example MB 400 M
(1) (2) (3)

(1) MB Abbreviation of FUJITSU Semiconductor
Integrated Circuit "Micro Block"
(富士通公司之半導體縮寫字首)

(2) Classification of TTL and Type Number
(TTL分類及型號)
MB8××× 系列 : High-Speed TTL 高速TTL
MB4××× 系列 : Standard TTL 標準TTL

(3) Package Type and Operating Temperature Range
(包裝型式與動作溫度範圍)
M Plastic Dual In-Line Package −15°C to +80°C
(塑膠並行接脚包裝型式)
(BLANK) Ceramic Dual In-Line Package −25°C to +125°C
(陶瓷並行接脚包裝型式)