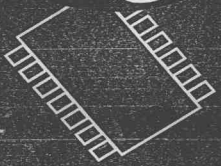
Logic IC Master Reference



David L. Heiserman

Preface

This reference work summarizes the identification codes, functions, pinouts, and package styles for a broad range of digital IC devices. The primary purpose is to help digital design engineers make the most prudent selection of IC devices for the projects at hand. The information can also help engineers and technicians determine the function and pinouts for digital IC devices found in circuits produced elsewhere.

It was necessary to apply some selection criteria in order to strike a balance between the size of the book and its usefulness in everyday engineering situations. Regarding functions, the selections are generally limited to small- and medium-scale devices—logic functions, buffers, decoders, multiplexers, counters, and shift registers for example. A few large-scale digital devices are included as well, but the selection is limited to the most common and necessary. There are no references for microprocessors and memory devices.

A second criterion for including a device in this book is its relative popularity. Devices provided by two or more major IC manufacturers are included here. Some devices offered by a single major manufacturer are also included, but only in those instances where they are part of a highly successful series of components.

The content of this book does not do away with the need for the depth of engineering detail found in IC manufacturer's data books. Rather, the primary function of this book is to offer a breadth of choice that cannot be found in the data books from a single manufacturer.

The main body of the book is divided into three sections:

Section I—54/7400 TTL and CMOS devices
Section II—4000-series CMOS devices
Section III—ECL devices

And there are two indexes. One of these is organized by device identification code and the other by device function.

Contents

Logic IC Master Reference

David L. Heiserman

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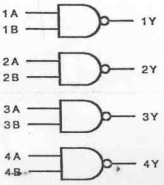
54/7400-Series Devices

(54/74)00 NAND Gate

- Quad 2-input

Pin Description
*n*A, *n*B — Data inputs
*n*Y — Data outputs

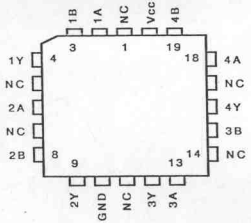


Logic diagram.

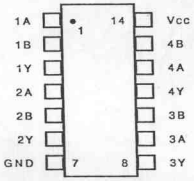
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

$Y = \overline{AB}$

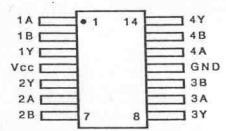
Logic table.



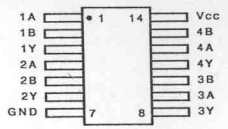
Pinout (top view) for all DIP and SO packages.



Pinout (top view) for all PLCC and LCC packages.



Pinout (top view) for the following FP packages: 5400, 54H00, and 54L00.



Pinout (top view) for the following FP packages: 54F00, 54LS00, and 54S00.

COMMERCIAL GRADE VERSIONS

DEVICE IDENTIFICATION	PACKAGE STYLE				
	DIP	SO	PLCC	LCC	FP
TTL TECHNOLOGY					
7400	14	14	20		
74ALS00	14	14	20		
74AS00	14	14	20		
74F00	14	14	20	20	
74H00	14				
74L00	14				
74LS00	14	14	20		
74S00	14	14	20		
CMOS TECHNOLOGY					
74AC00	14	14			
74ACT00	14	14			
74C00	14				
74HC00	14	14	20		
74HCT00	14	14			

INDUSTRIAL GRADE VERSIONS

DEVICE IDENTIFICATION	PACKAGE STYLE				
	DIP	SO	PLCC	LCC	FP
TTL TECHNOLOGY					
5400	14				14
54ALS00	14			20	
54AS00	14			20	
54F00	14			20	14
54H00	14				14
54L00	14				14
54LS00	14			20	14
54S00	14			20	14
CMOS TECHNOLOGY					
54AC00	14	14			
54ACT00	14	14			
54C00	14				
54HC00	14				
54HCT00	14				

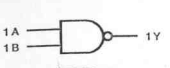
Available types and packages.

- Quad 2-input
- Open collector/drain

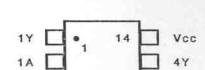
Pin Description

*n*A, *n*B — Data inputs

*n*Y — Data outputs



Logic diagram.

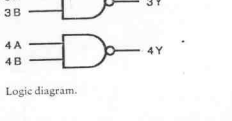


Pinout (top view) for all DIP and SO packages except 54/74H01.

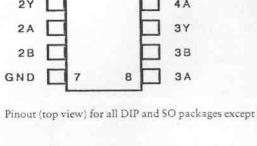
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

$Y = \overline{A B}$

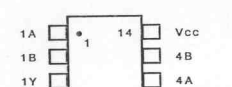
Logic table.



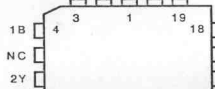
Pinout (top view) for DIP packages 54/74H01.



Pinout (top view) for all PLCC and LCC packages.



Pinout (top view) for 54LS01 FP package.



Pinout (top view) for the following FP packages: 5401, 54H01, and 54L01.

COMMERCIAL GRADE VERSIONS

DEVICE IDENTIFICATION	PACKAGE STYLE				
	DIP	SO	PLCC	LCC	FP
TTL TECHNOLOGY					
7401	14				
74ALS01	14	14	20		
74H01	14				
74L01	14				
74LS01	14	14	20		
CMOS TECHNOLOGY					
74HC01	14	14			

INDUSTRIAL GRADE VERSIONS

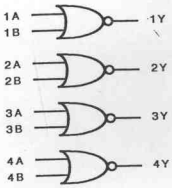
DEVICE IDENTIFICATION	PACKAGE STYLE				
	DIP	SO	PLCC	LCC	FP
TTL TECHNOLOGY					
5401	14				14
54ALS01	14			20	
54H01	14				14
54L01	14				14
54LS01	14			20	14
CMOS TECHNOLOGY					
54HCT01	14				

Available types and packages.

- Quad 2-input

Pin Description

*n*A, *n*B — Data inputs
*n*Y — Data outputs

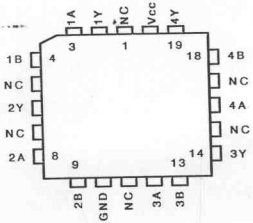


Logic diagram.

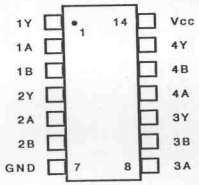
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

$Y = \overline{A + B}$

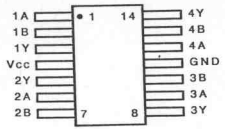
Logic table.



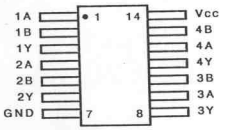
Pinout (top view) for all DIP and SO packages.



Pinout (top view) for PLCC and LCC packages.



Pinout (top view) for the following FP packages: 5402 and 54L02.



Pinout (top view) for the following FP packages: 54F02, 54LS02, and 54S02.

COMMERCIAL GRADE VERSIONS

DEVICE IDENTIFICATION	PACKAGE STYLE				
	DIP	SO	PLCC	LCC	FP
TTL TECHNOLOGY					
7402	14				
74ALS02	14	14	20		
74F02	14	14	20	20	
74L02	14				
74LS02	14	14	20		
74S02	14	14	20		
CMOS TECHNOLOGY					
74AC02	14	14	20		
74C02	14				
74HC02	14	14	20		
74HCT02	14	14			

INDUSTRIAL GRADE VERSIONS

DEVICE IDENTIFICATION	PACKAGE STYLE				
	DIP	SO	PLCC	LCC	FP
TTL TECHNOLOGY					
5402	14				14
54ALS02	14			20	
54AS02	14			20	
54F02	14			20	14
54L02	14				14
54LS02	14			20	14
54S02	14			20	14
CMOS TECHNOLOGY					
54AC02	14			20	14
54C02	14				
54HC02	14				
54HCT02	14				

Available types and packages.

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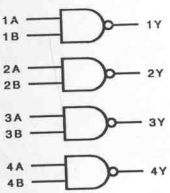
- Quad 2-input
- Open collector/drain

Pin Description

*n*A, *n*B — Data inputs
*n*Y — Data outputs

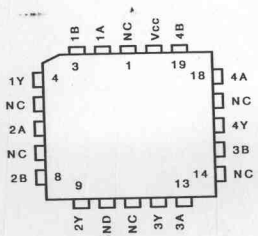


Logic diagram.

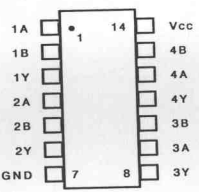
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

$Y = \overline{AB}$

Logic table.



Pinout (top view) for DIP, SO, and FP packages.



Pinout (top view) for PLCC and LCC packages.

COMMERCIAL GRADE VERSIONS

DEVICE IDENTIFICATION	PACKAGE STYLE				
	DIP	SO	PLCC	LCC	FP
TTL TECHNOLOGY					
7403	14				
74ALS03	14	14	20		
74L03	14				
74LS03	14	14	20		
74S03	14	14	20		
CMOS TECHNOLOGY					
74HC03	14	14	20		
74HCT03	14	14			

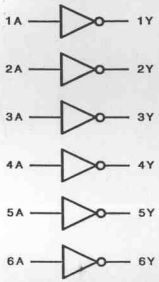
INDUSTRIAL GRADE VERSIONS

DEVICE IDENTIFICATION	PACKAGE STYLE				
	DIP	SO	PLCC	LCC	FP
TTL TECHNOLOGY					
5403	14				14
54ALS03	14		20		
54L03	14				
54LS03	14			20	14
CMOS TECHNOLOGY					
54HC03	14				
54HCT03	14				

Available types and packages.

- Hex

Pin Description
nA – Data input
nY – Data output

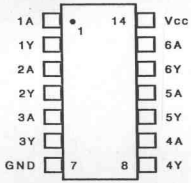


Function diagram.

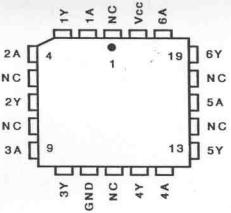
A	Y
0	1
1	0

$Y = \overline{A}$

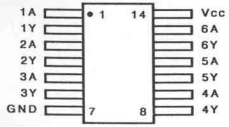
Function table.



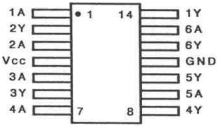
Pinout (top view) for DIP and SO packages.



Pinout (top view) for PLCC and LCC packages.



Pinout (top view) for the following FP packages: 7404, 54LS04, 54S04, 54AC04, 54ACT04, and 54C04.



Pinout (top view) for the 5404 and 54H04 FP packages.

COMMERCIAL GRADE VERSIONS

DEVICE IDENTIFICATION	PACKAGE STYLE				
	DIP	SO	PLCC	LCC	FP
TTL TECHNOLOGY					
7404	14				14
74ALS04	14	14	20		
74AS04	14	14	20		
74F04	14	14			
74H04	14				
74LS04	14	14	20		
74S04	14	14	20		
CMOS TECHNOLOGY					
74AC04	14	14	20		
74ACT04	14	14	20		
74C04	14				
74HC04	14	14	20		
74HCT04	14	14	20		

INDUSTRIAL GRADE VERSIONS

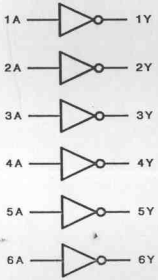
DEVICE IDENTIFICATION	PACKAGE STYLE				
	DIP	SO	PLCC	LCC	FP
TTL TECHNOLOGY					
5404	14				14
54ALS04		14			
54AS04		14			
54F04	14				
54H04	14				14
54L04	14				
54LS04	14	14		20	14
54S04	14	14		20	14
CMOS TECHNOLOGY					
54AC04	14			20	14
54ACT04	14			20	14
54C04	14				14
54HC04	14				
54HCT04	14				

Available types and packages.

- Hex
- Open-collector/drain outputs

Pin Description

*n*A – Data input
*n*Y – Data output

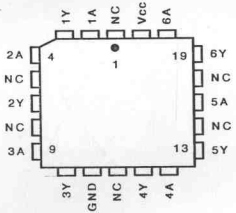


Function diagram.

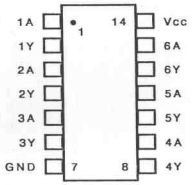
A	Y
0	1
1	0

$Y = \overline{A}$

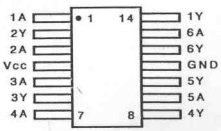
Function table.



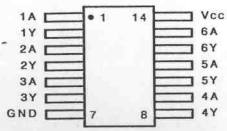
Pinout (top view) for DIP and SO packages.



Pinout (top view) for PLCC and LCC packages.



Pinout (top view) for the 5405 and 54H05 FP packages.



Pinout (top view) for the following FP packages: 7405, 54LS05, and 54S05.

COMMERCIAL GRADE VERSIONS

DEVICE IDENTIFICATION	PACKAGE STYLE				
	DIP	SO	PLCC	LCC	FP
TTL TECHNOLOGY					
7405	14				14
74ALS05	14	14			
74AS05	14	14	20		
74H05	14				
74LS05	14	14	20		
74S05	14	14	20		
CMOS TECHNOLOGY					
74AC05	14	14			
74ACT05	14	14			
74HC05	14	14			
74HCT05	14	14			

INDUSTRIAL GRADE VERSIONS

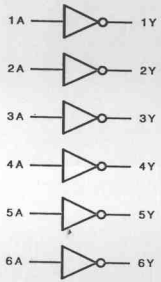
DEVICE IDENTIFICATION	PACKAGE STYLE				
	DIP	SO	PLCC	LCC	FP
TTL TECHNOLOGY					
5405	14				14
54ALS05	14	14		20	
54H05	14				14
54LS05	14			20	14
54S05	14			20	14
CMOS TECHNOLOGY					
54AC05	14				
54ACT05	14				
54HC05	14				
54HCT05	14				

Available types and packages.

- Hex
- Open-collector outputs
- Outputs rated at 30 V

Pin Description

*n*A — Data input
*n*Y — Data output

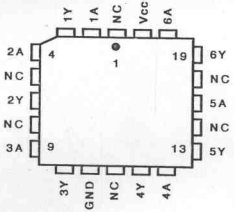


Function diagram.

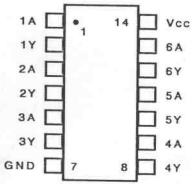
A	Y
0	1
1	0

$Y = \overline{A}$

Function table.



Pinout (top view) for DIP, SO, and FP packages.



Pinout (top view) for the PLCC package.

COMMERCIAL GRADE VERSIONS

DEVICE IDENTIFICATION	PACKAGE STYLE				
	DIP	SO	PLCC	LCC	FP
TTL TECHNOLOGY					
7406 74LS06	14 14	14	20		

INDUSTRIAL GRADE VERSIONS

DEVICE IDENTIFICATION	PACKAGE STYLE				
	DIP	SO	PLCC	LCC	FP
TTL TECHNOLOGY					
5406 54LS06	14 14				14

Available types and packages.

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