

IBM $\frac{PC}{PC}/XT$

逻辑原理图

苏州电子计算机厂

一九八四年十月

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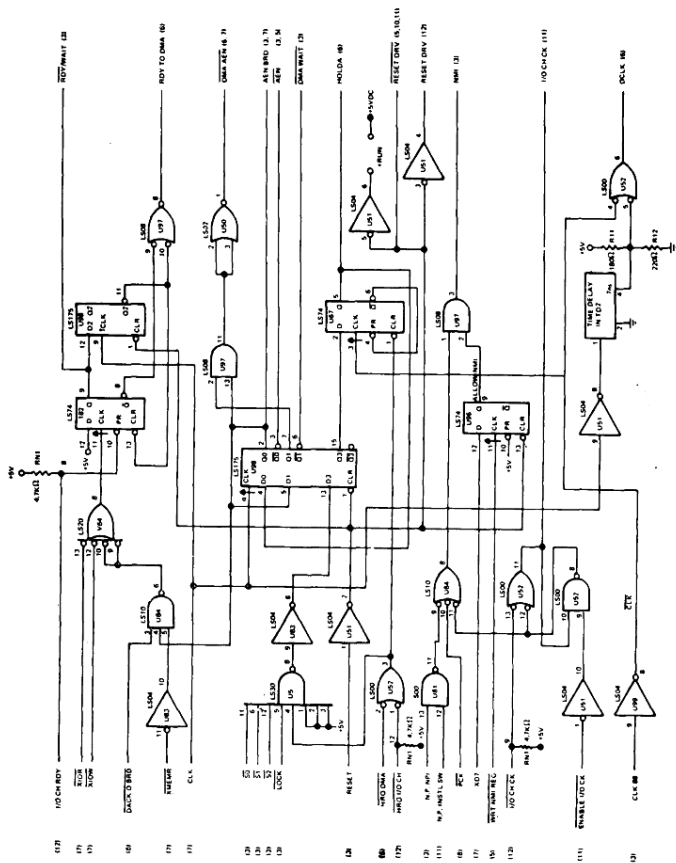
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Appendix D



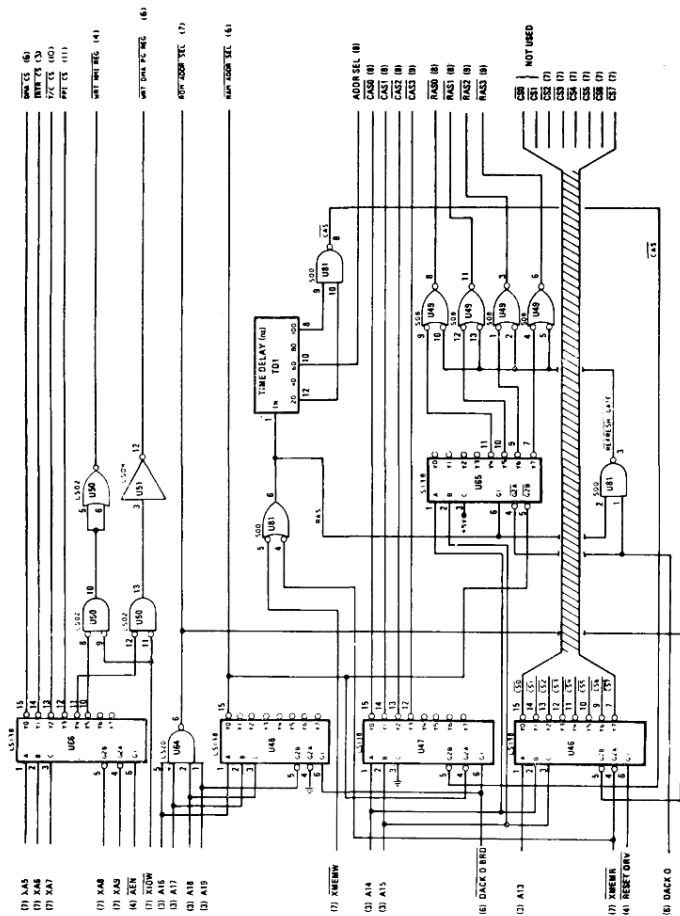
Logic Diagrams D-1

SYSTEM BOARD (WAIT STATE GENERATOR)

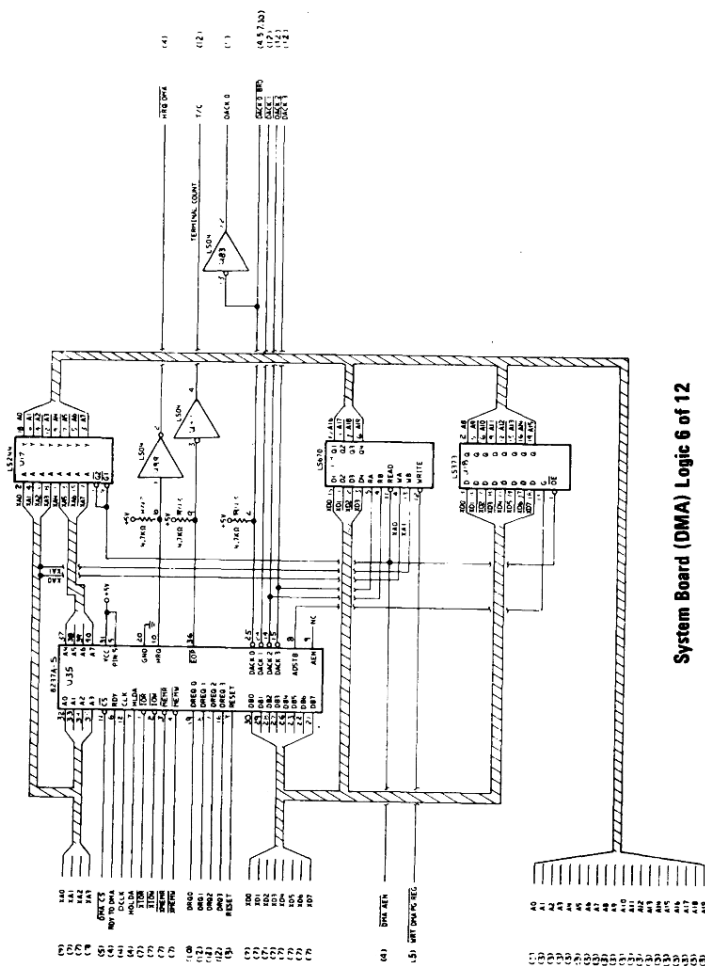


System Board (Wait State Generator) Logic 4 of 12

System Board (Device Decodes) Logic 5 of 12

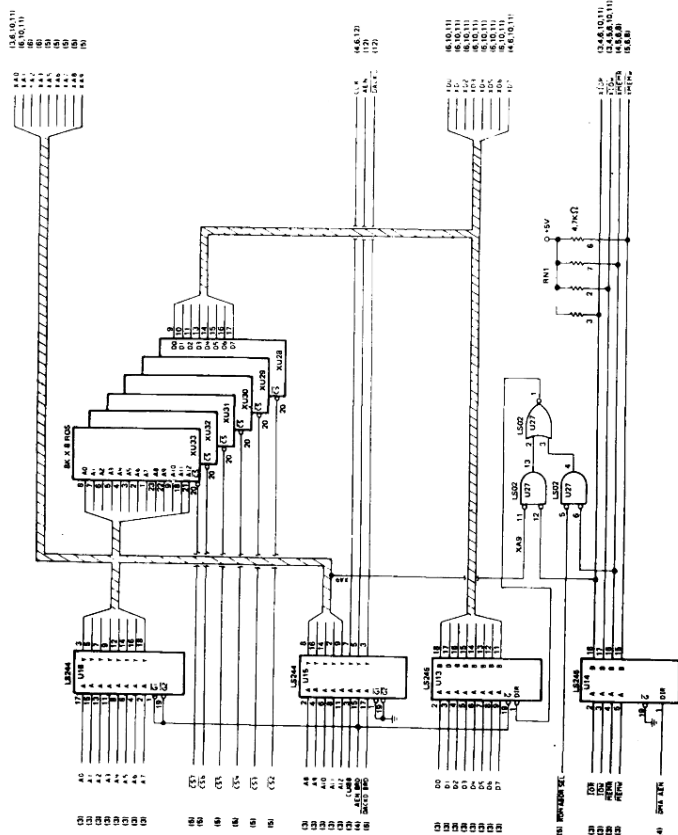


SYSTEM BOARD (DMA)



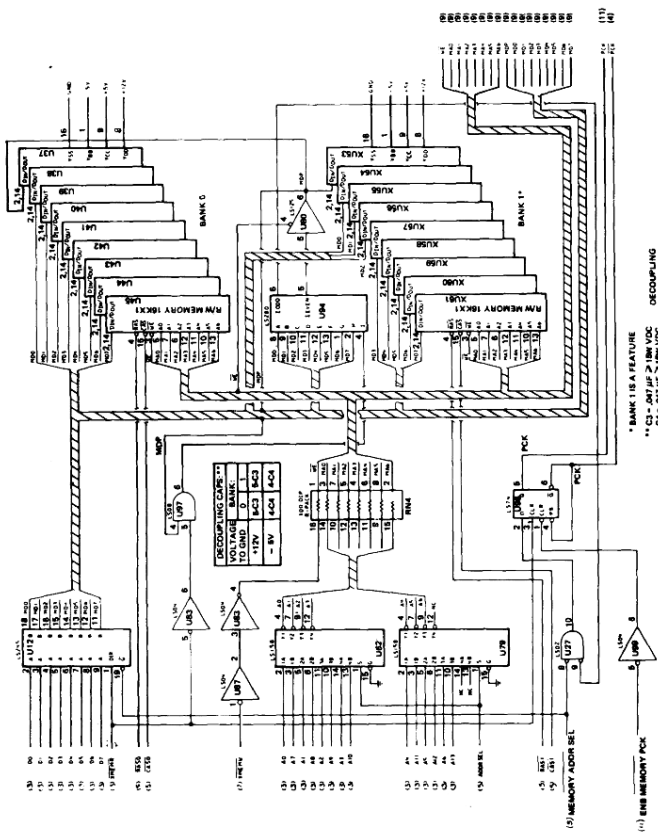
System Board (DMA) Logic 6 of 12

SYSTEM BOARD (ROS AND BUS DRIVER)



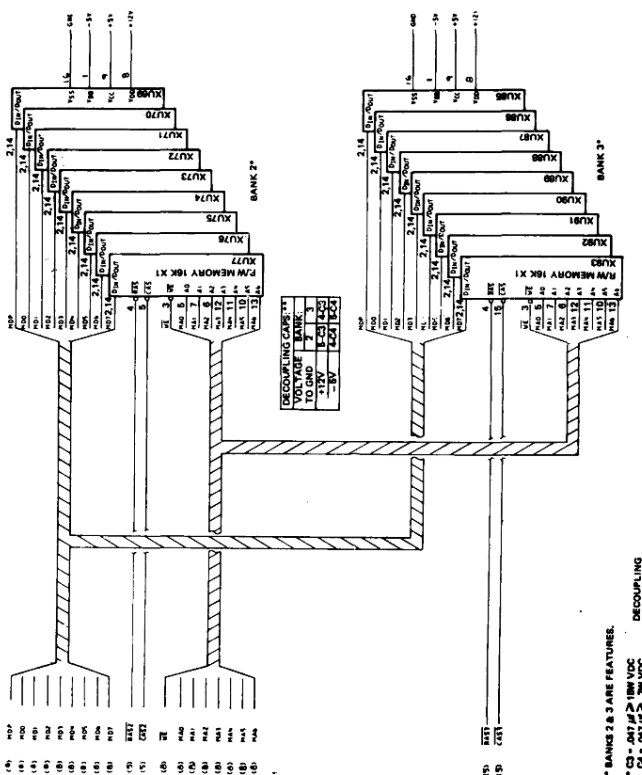
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SYSTEM BOARD (DYNAMIC MEMORY)



System Board (Dynamic Memory) Logic 8 of 12

SYSTEM BOARD (DYNAMIC MEMORY EXTENDED)

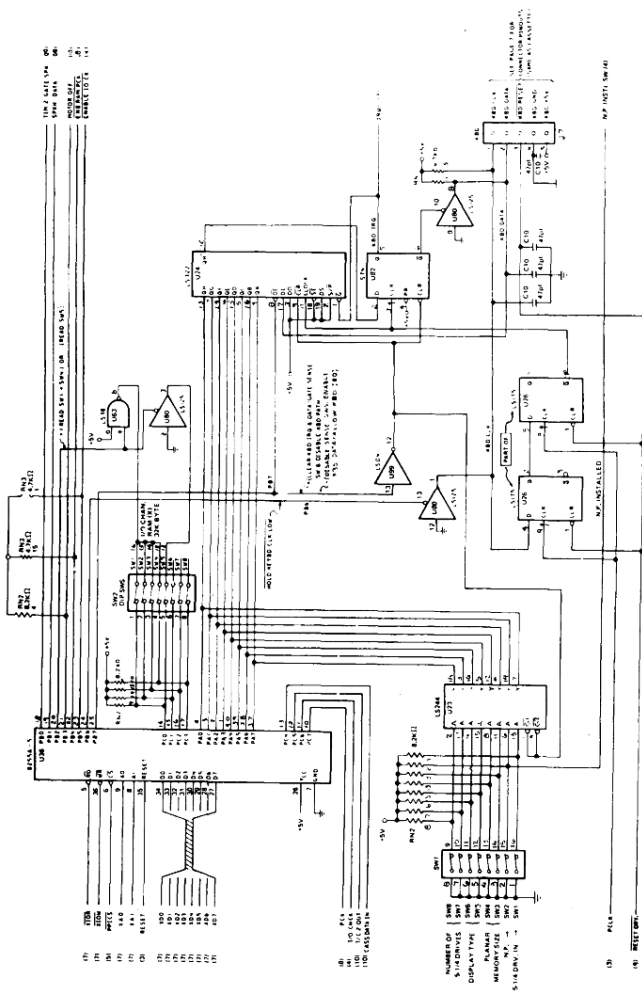


System Board (Dynamic Memory Extended) Logic 9 of 12

D-8 Logic Diagrams



SYSTEM BOARD (KEYBOARD/SENSE/CONTROL)



System Board (Keyboard/Sense/Control) Logic 11 of 12

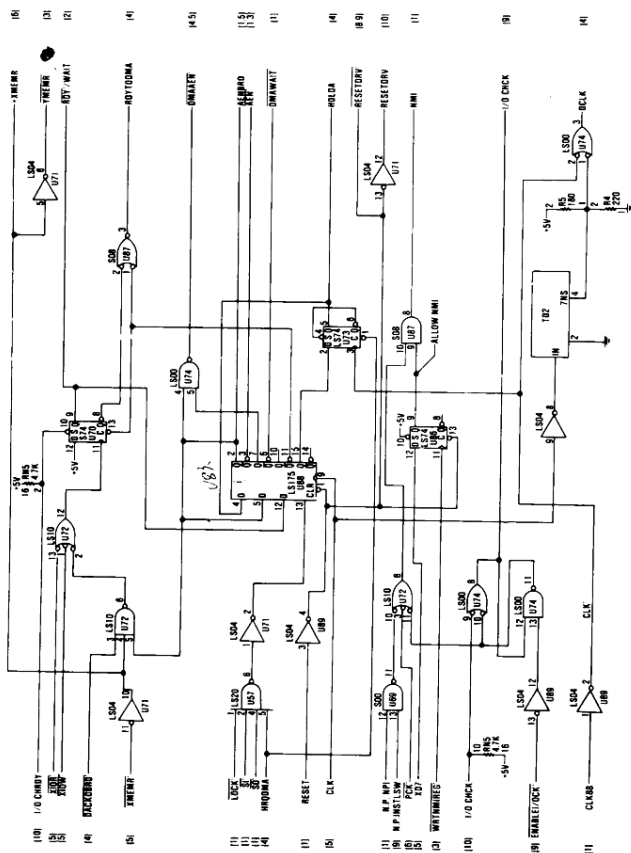
MODE	REG.	IN. CAP.	IN. W.
P (A)	REG.	IN. CAP.	IN.
P (B)	REG.	IN. CAP.	OUT
P (C)	REG.	IN. CAP.	IN.

9-10 Logic Diagrams

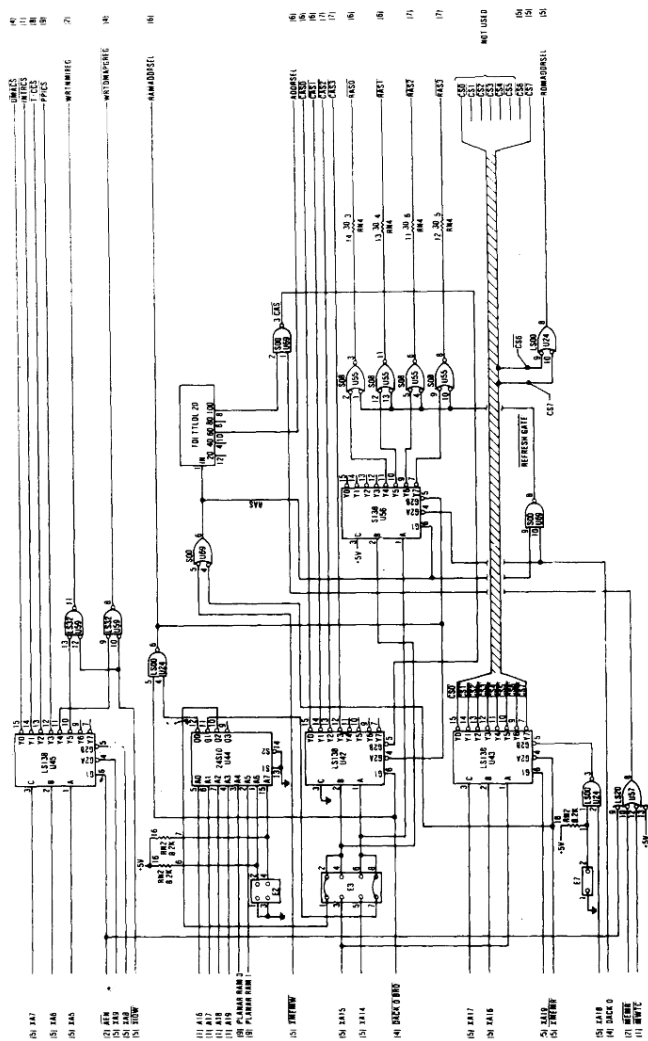


System Board (I/O Channel) Logic 12 of 12





System Board (Sheet 2 of 10)



System Board (Sheet 3 of 10)

