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TECHNICAL DIGEST

international
**ELECTRON
DEVICES**
meeting

1981

WASHINGTON, D.C.

December 7-8-9

Late News!
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1981 International Electron Devices Meeting TECHNICAL DIGEST

International Electron Devices Meeting.

International Electron Devices Meeting; (Technical program,
New York, Institute of Electrical and Electronics Engineers.

v. illus. 23 cm. annual.

Meetings for sponsored by the IEEE Electron Devices Group.
Includes supplements.

1. Electronic apparatus and appliances—Congresses. I. Institute of Electrical and Electronics Engineers. II. Institute of Electrical and Electronics Engineers. Electron Devices Group.

TK7801.I 53

621.881'028

78-20188

Library of Congress

rev
71 (r72c2)

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WELCOMING STATEMENT FROM THE GENERAL CHAIRMAN

Welcome to the 1981 International Electron Devices Meeting. This international forum on electron devices has been held every year, starting in 1955, in Washington, D.C. Attendance over the last five years has been increasing at the rate of approximately 12% per year, and attendance in 1981 is expected to exceed 2,000. The number of paper submissions has also approximately matched this pace. Abstracts submitted for consideration totaled 405. The program this year is composed of 26 contributed sessions composed of 170 accepted papers. These sessions cover the six main activity areas of the IEDM: Solid State Devices; Device Technology; Integrated Circuits; Quantum Electronics and Energy Conversion Devices; Detectors, Sensors and Displays; and Electron Tubes. In addition to the contributed sessions, which generally include an appropriate invited paper, are the Plenary Session and the Evening Panel Sessions. The three invited papers given Monday morning in the Plenary Session cover emerging potential technologies. These are a New Approach to a Self-Contained Solar Energy System; the Emerging Technology of Molecular Beam Epitaxy as Applied to Silicon; and Nonvolatile Semiconductor Memories.

This year will be the third year the IEDM has scheduled a panel session for Tuesday evening. In continuing to explore the desires of its attendees, the program committee this year has organized two panels which run simultaneously. One follows up on the Plenary Session topic of solar energy and is entitled Prospects for Photovoltaics, while the second addresses processing issues in leading-edge silicon integrated circuits technology. The issue of innovation, current industrial productivity, and perhaps changes needed in the structure of our society in the 1980's will be addressed by our Tuesday luncheon speaker, Dr. Tom Vanderslice, President and Chief Operating Officer of General Telephone and Electronics in his presentation entitled "Challenges of Technological Leadership."

The growth of R&D activities reported on at the IEDM, even in periods of economic slowdown, attests to the increasing importance attached to these activities by both the private and public sectors of the industrialized world. In recognition of this growing and more geographically dispersed base from which the IEDM attracts attendees, beginning next year the IEDM will be held in San Francisco in even years and return on odd years to its present location, the Washington Hilton. In 1982 the site for the IEDM is the San Francisco Hilton.

I want to congratulate the Conference Committee for the excellent job they have done in planning and organizing the 1981 IEDM, and thank them in behalf of the members of the IEEE Electron Devices Society, which sponsors the IEDM, for their hard work and dedication to excellence. Finally, and most importantly, I want to thank the authors of the papers for their commitment to technical excellence and welcome them and all attendees to the 1981 International Electron Devices Meeting.



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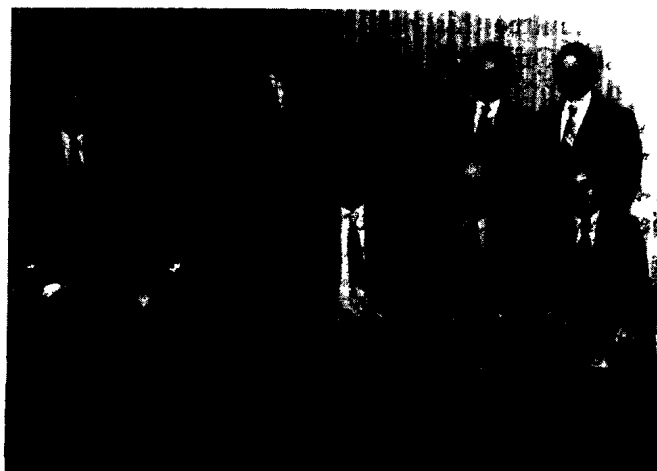
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IBM Thomas J. Watson
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Yorktown Heights, NY, USA

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9.4 **AN ANALYTIC MOSFET MODEL INCLUDING INTER-NODAL CAPACITANCES: RESULTS ON DEVICE SCALING AND PARASITIC LIMITATIONS**, G.W. Taylor and W. Fichtner, *Bell Laboratories, Murray Hill, NJ* 215

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9.5 **A RE-EXAMINATION OF PRACTICAL SCALABILITY LIMITS OF N-CHANNEL AND P-CHANNEL MOS DEVICES FOR VLSI**, H. Shichijo, *Texas Instruments Incorporated, Dallas, TX* 219

11:10 a.m.

9.6 **A TWO-DIMENSIONAL COMPUTER SIMULATION OF HOT CARRIER EFFECTS IN MOSFETS**, S. M. Wada, T. Shibata, M. Konaka, H. Izuka, and R.L.M. Dang, *Toshiba Corporation, Kawasaki, Japan* 223

SESSION 10: Device Technology—New Developments in Material Technology

Tuesday, December 8, 9:00 a.m.

International Ballroom Center

Co-Chairmen: H.J. Geipel
L.C. Parrillo

9:00 a.m.

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10.1 **OXYGEN PRECIPITATION IN SILICON** (Invited Paper), R.A. Craven, *Monsanto Industrial Chemicals Co., St. Louis, MO* 228

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10.2 **STRESS-ENHANCED MOBILITY IN MOSFETS FABRICATED IN ZONE-MELTING-RECRYSTALLIZED POLY-SI FILMS**, B.-Y. Tsaur, J.C.C. Fan, M.W. Geis, D.J. Silversmith, and R.W. Mountain, *Lincoln Laboratory, Massachusetts Institute of Technology, Lexington, MA* 232

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10.3 **A DETAILED CHARACTERIZATION OF MOS TRANSISTORS FABRICATED ON LASER-CRYSTALLIZED POLYSILICON**, R.D. Dwivedi and R.E. Thomas, *Carleton University, Ottawa, Canada* 190

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10.4 **THE USE OF THIN EPITAXIAL SILICON LAYERS FOR MOS VLSI** (Invited Paper), D.S. Yaney, *Bell Laboratories, Allentown, PA*, and C.W. Pearce, *Western Electric Co., Allentown, PA* 236

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10.5 **LOW TEMPERATURE PHOTO-CVD OXIDE PROCESSING FOR SEMICONDUCTOR DEVICE APPLICATIONS**, J.W. Peters, *Hughes Aircraft Co., Culver City, CA* 240

11:10 a.m.

10.6 **INFLUENCE OF ENCAPSULATION FILMS ON THE PROPERTIES OF Si/SiO₂ INTERFACE OF MOS-STRUCTURES WHEN EXPOSED TO RADIATION**, A.G. Sabnis, J.T. Nelson, and J.N. Billig, *Bell Laboratories, Allentown, PA* 244

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Jefferson Room

Co-Chairmen: A.R. Hartman
J.E. Berthold

9:00 a.m.

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11.1 **530V INTEGRATED GATED DIODE SWITCH FOR TELECOMMUNICATIONS**, A.R. Hartman, J.E. Berthold, T.J. Riley, J.E. Kohl, Y.H. Wong, H.T. Weston, and R.S. Scott, *Bell Laboratories, Murray Hill, NJ, and Reading, PA* 250

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11.2 **HIGH VOLTAGE INTEGRATED CIRCUITS FOR TELECOMMUNICATIONS** (Invited Paper), T. Kamei, *Hitachi Research Laboratory, Itachi-shi, Japan* 254

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11.3 **PROCESS AND DEVICE DESIGN OF A 1000V MOS-IC**, T. Yamaguchi and S. Morimoto, *Tektronix, Inc., Beaverton, OR* 255

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11.4 INTEGRATED HIGH-VOLTAGE/LOW-VOLTAGE MOS DEVICES, S.A. Buhler, D.L. Heald, R.R. Ronen, T. Gannon, and P. Elkins, *Xerox Microelectronics Center, El Segundo, CA* 259
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11.5 THE MONOLITHIC HV BIPMOS, N. Zommer, *Intersil, Inc., Cupertino, CA* 263
- 11:10 a.m.
11.6 A DEPLETION STOP DOUBLE BASE PHOTOTRANSISTOR: A DEMONSTRATION OF A NEW TRANSISTOR STRUCTURE, C.Y. Chen, A.Y. Cho, P.A. Garbinski, and C.G. Bethea, *Bell Laboratories, Murray Hill, NJ* 267

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M.A. Pollack

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12.2 AN INTEGRATED p/n/J-FET PHOTORECEIVER FOR LONG WAVELENGTH OPTICAL SYSTEMS, R.F. Leheny, R.E. Nahory, J.C. DeWinter, R.J. Martin, and E.D. Beebe, *Bell Laboratories, Holmdel, NJ* 276
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12.3 MONOLITHIC INTEGRATION OF OPTIC DETECTORS WITH WAVELENGTH MULTIPLEXING AMPLIFIERS FOR CABLE AND WIDEBAND SATELLITE COMMUNICATIONS, A. von Lehmen, and J.M. Ballantyne, *Cornell University, Ithaca, NY*
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12.4 THE RELIABILITY OF 1.3 μm EMITTERS AND DETECTORS FOR FIBER OPTICS, M. Eittenberg and G.H. Olsen, *RCA Laboratories, Princeton, NJ* 280
- 10:45 a.m.
12.5 THE SUPERLATTICE PHOTODETECTOR: A NEW AVALANCHE PHOTODIODE WITH A LARGE IONIZATION RATES RATIO, F. Capasso, W.T. Tsang, A. Hutchinson, and G.F. Williams, *Bell Laboratories, Murray Hill, NJ* 284
- 11:10 a.m.
12.6 DETERMINATION OF IMPACT IONIZATION COEFFICIENTS IN InP BY ANALYSIS OF PHOTOMULTIPLICATION AND NOISE MEASUREMENTS, G.E. Bulman, L.W. Cook, M.M. Tashima, and G.E. Stillman, *University of Illinois, Urbana, IL* 288
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12.7 TRAP-ASSISTED TUNNELING IN THE REVERSE DARK CURRENT OF GaAlAsSb AVALANCHE PHOTODIODES, R. Chin, *Rockwell International, Thousand Oaks, CA*, and N. Tabatabaie and G. E. Stillman, *University of Illinois, Urbana, IL* 292

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P. Pleshko

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13.2 THE CHARACTERISTICS AND PERFORMANCE OF AN EXPERIMENTAL AC PLASMA 960 × 768 LINE PANEL AND ELECTRONICS ASSEMBLY, P. Pleshko, G.W. Smith, D.R. Thompson, and N. Vecchiarelli, *IBM Corporation, Kingston, NY* 299
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13.3 AN IMPROVED POSITIVE CONTRAST GUEST-HOST TYPE DISPLAY USING NEMATIC-CHOLESTERIC PHASE-CHANGE, H. Kawarada, T. Tatsumichi, and T. Otsuka, *Matsushita Electric Industrial Co., Ltd., Osaka, Japan* 301
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13.4 EVAPORATED POLYCRYSTALLINE-SILICON THIN-FILM TRANSISTORS ON GLASS, A. Misumi, K. Sunahara, H. Tanabe, and M. Kumada, *Hitachi, Ltd., Chiba Prefecture, Japan* 305
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13.5 A 2048-ELEMENT CONTACT-TYPE LINEAR IMAGE SENSOR FOR FACSIMILE, K. Komiya and M. Kanzaki, *Nippon Telephone and Telegraph, Kanagawa, Japan*, and T. Yamashita, *Matsushita Electric Industrial Co., Ltd., Osaka, Japan* 309
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13.6 A CONTACT-TYPE LINEAR SENSOR WITH AN A GD A-Si:H PHOTODETECTOR ARRAY, Y. Kanoh, S. Usui, A. Sawada, and M. Kikuchi, *Sony Corporation Research Center, Yokohama, Japan* 313

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R.W. Grow

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14.2 THEORY OF EIGENMODE AMPLIFICATION, G. Dohler, D. Gallagher, and R. Moats, *Northrop Defense Systems Division, Rolling Meadows, IL* 321
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14.3 "COMB-QUAD" MILLIMETER-WAVE COUPLED CAVITY TWT INTERACTION STRUCTURE, A. Karp, *Varian Associates, Palo Alto, CA* 325
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14.4 PENIOTRON OSCILLATOR OPERATING PERFORMANCE, G. Dohler, D. Gallagher, R. Moats, R. Scafuri, *Northrop Defense Systems Division, Rolling Meadows, IL* 328
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14.5 A TRIPLE-POLE-PIECE MAGNETIC FIELD REVERSAL ELEMENT FOR GENERATION OF HIGH ROTATIONAL ENERGY BEAMS, G.P. Scheitrum and R. True, *Litton Industries, San Carlos, CA* 332
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14.6 MAGNETICALLY SHIELDED ELECTRON GUNS WITH A CENTER MAGNETIC POST, N.R. Vanderplaats, H.E. Brown, S. Ahn, *Naval Research Laboratory, Washington, D.C.* 336
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14.7 MULTIPACTOR ELECTRON GUN FOR MILLIMETER WAVE TUBES, C. Bates, G. DeLhery, J. Hartley, P. Fischer, *ERADCOM, Fort Monmouth, NJ* 339

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Technology and Structures**

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International Ballroom East

Co-Chairmen: W.T. Lynch
C.A.T. Salama

2:15 p.m.

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2:20 p.m.

15.1 **SCALEABLE RETROGRADE P-WELL CMOS TECHNOLOGY**, S.R. Combs, *Intersil, Cupertino, CA*

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15.2 **350°C CMOS LOGIC PROCESS**, J.D. Beasom, R.D. Moore, and G. Mohammed, *Harris Semiconductor, Melbourne, FL*, and B.L. Draper, *Sandia National Laboratories, Albuquerque, NM*

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15.3 **DESIGN MODEL FOR BULK CMOS SCALING ENABLING ACCURATE LATCH-UP PREDICTION**, A.W. Wieder, C. Werner, and J. Harter, *Siemens AG, Munich, F.R. Germany*

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15.4 **FLOATING SUBSTRATE EFFECTS IN SOS VLSIs**, H. Hatano, Y. Uchida, M. Isobe, K. Maeguchi, and H. Tango, *Toshiba Corp., Kawasaki, Japan*

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15.5 **A NOVEL BURIED-DRAIN DMOSFET STRUCTURE**, W. Fichtner, J.A. Cooper, A.R. Tretola, and D. Kahng, *Bell Laboratories, Murray Hill, NJ*

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15.6 **SCHOTTKY MOSFET FOR VLSI**, C.I. Koeneke, S.M. Sze, R.F. Levin, and E. Kinsbron, *Bell Laboratories, Murray Hill, NJ*

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Technology**

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Co-Chairmen: K.W. Yeh
Y. Nishi

2:15 p.m.

INTRODUCTION

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16.1 **DIRECT MOAT ISOLATION FOR VLSI**, K. Wang, S. Saller, W. Hunter, P. Chatterjee, and P. Yang, *Texas Instruments Incorporated, Dallas, TX*

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16.2 **FULL ISOLATION TECHNOLOGY BY POROUS OXIDIZED SILICON AND ITS APPLICATION TO LSIs** (Invited Paper), K. Imai and S. Nakajima, *Nippon Telegraph and Telephone Public Corporation, Tokyo, Japan*

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16.3 **DOUBLE THRESHOLD MOSFETs IN BIRD'S-BEAK FREE STRUCTURES**, T. Iizuka, K. Chiu, and J. Moll, *Hewlett-Packard Laboratories, Palo Alto, CA*

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3:35 p.m.

16.4 **A NEW BIRD'S-BEAK FREE FIELD ISOLATION TECHNOLOGY FOR VLSI DEVICES**, K. Kurosawa, T. Shibata, and H. Iizuka, *Toshiba Research and Development Center, Kawasaki, Japan*

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16.5 **HIGH-FIELD GENERATION OF ELECTRON TRAPS AND CHARGE TRAPPING IN ULTRA-THIN SiO₂**, C. Jeng, T. Ranganath, C. Huang, H. Jones, and T. Chang, *Intel Corp., Santa Clara, CA*

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16.6 **NEW INSTABILITY IN THIN GATE OXIDE MOST's**, Y. Kojima, M. Kamiya, K. Tanaka, *Daini Seikosha Co., Ltd., Matsudo*, and K. Nagai and Y. Hayashi, *Electrotechnical Lab., Niihorigawa, Japan*

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16.7 **ELECTRON TRAPPING IN VERY THIN THERMAL SILICON DIOXIDES**, M. Liang and C. Hu, *University of California, Berkeley, CA*

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16.8 **THERMAL NITRIDE CAPACITORS FOR HIGH DENSITY RAMs**, M. Taguchi, T. Ito, T. Fukano, T. Nakamura, and H. Ishikawa, *Fujitsu Laboratory, Kawasaki, Japan*

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Jefferson Room

Co-Chairmen: H.N. Yu
V.A.K. Temple

2:15 p.m.

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17.1 **CONTROLLED THYRISTOR TURN-ON FOR HIGH DI/DT CAPABILITY** (Invited Paper), V.A.K. Temple, *General Electric Company, Corporate R&D Center, Schenectady, NY*

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17.2 **THYRISTORS WITH OVERVOLTAGE SELF-PROTECTION**, J.X. Przybysz and E.S. Schlegel, *Westinghouse Research Center, Pittsburgh, PA*

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17.3 **A STUDY ON GTO THYRISTOR TURN-OFF FAILURE MECHANISM**, H. Ohashi and A. Nakagawa, *Toshiba Research and Development Center, Kawasaki, Japan*

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17.4 **A LARGE AREA POWER MOSFET DESIGNED FOR LOW CONDUCTION LOSSES**, P.V. Gray, R.P. Love, and M.S. Adler, *General Electric Company, Corporate R&D Center, Schenectady, NY*

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17.5 **POWER MOS TRANSISTOR FOR 1000 V BLOCKING VOLTAGE**, J.P. Stengl, H. Strack, and J. Tihanyi, *Siemens AG, Munich, Germany*

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17.6 **LOW-SPECIFIC-ON-RESISTANCE-400 V LDMOST**, E.H. Stupp, S. Colak, and J. Ni, *Philips Laboratories, Briarcliff Manor, NY*

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17.7 **ON-RESISTANCE CHARACTERIZATION OF VDMOS POWER TRANSISTORS**, M.L. Tarng, *RCA Laboratories, David Sarnoff Research Center, Princeton, NJ*

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G.H. Olsen

2:15 p.m.

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18.1 **QUANTUM WELL LASER STRUCTURE** (Invited Paper), P.D. Dapkus and J.J. Coleman, *Rockwell International Microelectronics Research and Development Center, Thousand Oaks, CA*, and N. Holonyak, Jr., *University of Illinois, Urbana, IL*

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18.2 **SHALLOW PROTON STRIPE GaAlAs DH LASERS GROWN BY MO-CVD**, R.D. Burnham, D.R. Scifres, and W. Streifer, *Xerox Palo Alto Research Centers, Palo Alto, CA*

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18.3 HIGHLY RELIABLE AND MODE-STABILIZED (GaAl) As DOUBLE-HETEROSTRUCTURE VISIBLE LASERS ON p-GaAs SUBSTRATE, T. Hayakawa, S. Yamamoto, H. Hayashi, N. Ohtsuka, K. Murata, J. Takagi, T. Sakurai, and T. Hijikata, *Central Research Laboratories, Sharp Corporation, Nara, 632, Japan* 443

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18.4 HIGH-POWER SINGLE-MODE SEMICONDUCTOR DIODE LASERS (Invited Paper), D. Botez, *RCA Laboratories, Princeton, NJ* 447

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18.5 HIGH POWER OPTICAL FIBER DATA TRANSMISSION USING CDH-LOC AlGaAs LASER DIODES, D.J. Chanin, D. Botez, J.C. Connolly, J.O. Schroeder, J.P. Bednarz, and M. Ettenberg, *RCA Laboratories, Princeton, NJ* 452

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18.6 AUGER RECOMBINATION IN $In_{1-x}Ga_xAsP_{1-y}$, N.K. Dutta and R.J. Nelson, *Bell Laboratories, Murray Hill, NJ* 456

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18.7 LASER GENERATED (Al, Ga) As MICROSTRUCTURES WITH HIGH LUMINESCENCE EFFICIENCY, H.H. Gilgen, R.P. Salathe, Y. Rytz-Froidevaux, *University of Bern, Bern, Switzerland* 457

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18.8 THREE TERMINALS AlGaAs/GaAs HETEROSTRUCTURE LED, M. Sakuta, H. Takano, M. Kobayashi, and Y. Arai, *OKI Electric Industry Co., Ltd., Tokyo, 193, Japan* 461

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Co-Chairmen: K.D. Wise
 J.W. Knutti

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19.3 ACCURATE SIMULATION OF HIGH-PERFORMANCE SILICON PRESSURE SENSORS, K.W. Lee and K.D. Wise, *Electron Physics Laboratory, Department of Electrical and Computer Engineering, University of Michigan, Ann Arbor, MI* 471

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19.4 A NOVEL SOLID-STATE IMAGE SENSOR FOR IMAGE RECORDING AT 2000 FRAMES PER SECOND, T.H. Lee, T.J. Tredwell, B.C. Burkey, J.S. Hayward, T.M. Kelly, R.P. Khosla, and D.L. Losee, *Research Laboratories, Eastman Kodak Company, Rochester, NY* 475

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19.5 SOLID-STATE COLOR IMAGER USING AN α -Si:H PHOTOCONDUCTIVE FILM, T. Tsukada, T. Baji, Y. Shimomoto, A. Sasano, Y. Tanaka, H. Matsumaru, Y. Takasaki, N. Koike, and T. Akiyama, *Central Research Laboratory, Hitachi, Ltd., Kokubunji, Tokyo, 185, Japan* 479

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19.6 A POLYSILICON-ISOLATED PHOTODIODE ARRAY IMAGER, N. Kadekodi, S. Law, C. Chang, M. Lo, and A. Ibrahim, *Xerox Microelectronics Center, Xerox Corporation, El Segundo, CA* 483

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19.7 A CCD IMAGING DEVICE HAVING A PLOSS STRUCTURE, Y. Terui, M. Yoshino, M. Ogura, M. Nakayama, K. Kugimiya, S. Akiyama, T. Chikamura, Y. Miyata, S. Horiuchi, Y. Ota, M. Yoneda, M. Fujimoto, and H. Tanaka, *Central Research Laboratory, Matsushita Electric Co., Ltd., Osaka, 570, Japan* 487

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Monroe Room

Co-Chairmen: L.A. Wood
 J.J. Tancredi

2:15 p.m.
INTRODUCTION

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20.2 SYNTHESIS OF A HOLLOW-BEAM GUN BASED ON THE PIERCE DESIGN, J.R.M. Vaughan, *Litton Industries, San Carlos, CA* 496

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20.3 SOLITONS AND MICROWAVE CROSSED FIELD AMPLIFIER CHARACTERISTICS, G.E. Thomas and A.S. Wilczek, *Varian Associates, Beverly, MA* 500

3:35 p.m.
20.4 A COUPLED-CAVITY TWT OPERATING IN THE INVERTED SLOT MODE, J.R. Frey and I. Tammaru, *Hughes Aircraft Co., Torrance, CA* 504

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Tuesday, December 8, 8:00-10:00 p.m.
International Ballroom East

Panel Organizer: D.G. Schueler
 Sandia National Laboratories
 Albuquerque, NM

PANEL DISCUSSION MEMBERS

Panel Moderator: Donald G. Schueler
 Sandia National Laboratories
 Albuquerque, NM

Edgar A. DeMeo
 Electric Power Research
 Institute
 Palo Alto, CA

Henry Ehrenreich
 Harvard University
 Cambridge, MA

Donald L. Feucht
 Solar Energy Research
 Institute
 Golden, CO

John V. Goldsmith
 Solarex Corporation
 Rockville, MD

Robert N. Hall
 General Electric Company
 Schenectady, NY

Mathew S. Imamura
 Martin Marietta Corporation
 Denver, CO

European Panel Member
 (to be announced)

SESSION 22: Evening Panel Discussion

Tuesday, December 8, 8:00-10:00 p.m.
International Ballroom Center

Panel Organizer: Michael S. Adler
General Electric Co.
Corporate Research and Development
Center
Schenectady, NY

PANEL DISCUSSION MEMBERS

Panel Moderator: Michael S. Adler
General Electric
Schenectady, NY

Dana Secombe
Hewlett Packard
Ft. Collins, CO

Billy Crowder
IBM
Yorktown Heights, NY

Roderick Davies
Texas Instruments
Dallas, TX

Yasutaka Ban
Fujitsu Ltd.
Kawasaki, Japan

U. Buerker
Siemens AG
Munich, Germany

William Oldham
University of California
Berkeley, CA

Hyman J. Levinstein
Bell Telephone
Laboratories
Murray Hill, NJ

Youssef A. El-Mansy
Intel Corp.
Aloha, OR

SESSION 23: Integrated Circuits—Bipolar IC Technology

Wednesday, December 9, 9:00 a.m.
International Ballroom East

Co-Chairmen: J.E. Smith
W.M. Shedd

9:00 a.m.

INTRODUCTION

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23.1 PERSPECTIVE OF SCALED BIPOLAR DEVICES, N. Hanaoka and A. Anzai, *Hitachi, Tokyo, Japan*

9:30 a.m.

23.2 MODELING OF BIPOLAR DEVICE STRUCTURES-PHYSICAL SIMULATION, J.L. D'Arcy, E.J. Prendergast, and P. Lloyd, *Bell Telephone Laboratories, Allentown, PA*

9:55 a.m.

23.3 LIMITATIONS TO THE SCALING OF SCHOTTKY BARRIER DIODES, A.K. Kapoor and M. Vora, *Fairchild Advanced Research and Development Laboratory, Palo Alto, Ca*

10:20 a.m.

23.4 1.25 MICRON INJECTION LOGIC TECHNOLOGY, M. Vora, W. Rust, S. Radigan, and K. Radigan, *Fairchild Advanced Research and Development Laboratory, Palo Alto, CA*

10:45 a.m.

23.5 E-BEAM FABRICATION OF BIPOLAR VLSI LOGIC, INCLUDING A ~ 5K GATE 16-BIT I²L MICROPROCESSOR, R.H. Havemann, L.A. Arledge, Jr., R.L. Smith, and S.A. Evans, *Texas Instruments, Dallas, TX*

SESSION 24: Device Technology—Advanced CMOS Technology

Wednesday, December 9, 9:00 a.m.
International Ballroom Center

Co-Chairmen: L.C. Parrillo
H.J. Geipel

9:00 a.m.

INTRODUCTION

9:05 a.m.

24.1 ADVANCED HI-CMOS DEVICE TECHNOLOGY, Y. Sakai, T. Hayashida, N. Hashimoto, O. Mimato, and T. Masuhara, *Hitachi Central Research Laboratory, Tokyo, Japan*, and K. Nagasawa, T. Yasui and N. Tanimura, *Hitachi Musashi Works, Tokyo, Japan*

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9:30 a.m.

24.2 CONSIDERATIONS FOR SCALED CMOS SOURCE/DRAINS, D.B. Scott, Y.C. See, C.K. Lau, and R.D. Davies, *Texas Instruments Incorporated, Dallas, TX*

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9:55 a.m.

24.3 LATERAL EFFECT OF OXIDATION ENHANCED DIFFUSION IN SILICON, M. Hamasaki, J. Suzuki, and T.F. Shimada, *Sony Corporation, Kanagawa, Japan*

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24.4 EXPERIMENTAL AND THEORETICAL RESULTS ON FINE-LINE P-CHANNEL MOSFETS, W. Fichtner, R.M. Levin, K.K. Ng, and G.W. Taylor, *Bell Laboratories, Murray Hill, NJ*

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24.5 HOT CARRIER INSTABILITY IN SUBMICRON MoSi₂ GATE MOS/SOS DEVICES, Y. Mizutani, S. Taguchi, M. Nakahara, and H. Tango, *Toshiba Corporation, Kanagawa, Japan*

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11:10 a.m.

24.6 VERTICAL SINGLE-GATE CMOS INVERTERS ON LASER-PROCESSED MULTILAYER SUBSTRATES, G.T. Goeloe, E.W. Maby, D.J. Silversmith, R.W. Mountain, and D.A. Antoniadis, *Lincoln Laboratory, Massachusetts Institute of Technology, Lexington, MA*

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11:35 a.m.

24.7 ST-CMOS (STACKED TRANSISTORS CMOS): A DOUBLE-POLY-NMOS-COMPATIBLE CMOS TECHNOLOGY, J.P. Colinge and E. Demoulin, *CNET-CNS, Meylan, France*

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SESSION 25: Device Technology—Process Technology

Wednesday, December 9, 9:00 a.m.
International Ballroom West

Co-Chairmen: D.A. Antoniadis
D.F. Barbe

9:00 a.m.

INTRODUCTION

9:05 a.m.

25.1 AN OPERATIONAL TWO LEVEL PHOTORESIST TECHNOLOGY, (Invited Paper), B.F. Griffing, *General Electric Corporate Research and Development Center, Schenectady, NY*

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9:30 a.m.

25.2 PRECISION REGISTRATION METHOD FOR 0.5 μm ELECTRON BEAM LITHOGRAPHY, M. Fujinami, N. Shimazu, and K. Takamoto, *Musashino Electrical Communication Laboratory, N.T.T., Tokyo, Japan*, and N. Saitou, *Central Research Laboratory, Hitachi Ltd., Tokyo, Japan*

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9:55 a.m.

25.3 FEATURE SIZE LIMIT ANALYSIS OF LIFT-OFF METALLIZATION TECHNOLOGY, Y. Homma, A. Yajima, and S. Harada, *Central Research Laboratory, Hitachi, Ltd., Tokyo, Japan*

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10:20 a.m.

25.4 USE OF PROCESS AND 2-D MOS SIMULATION IN THE STUDY OF DOPING PROFILE INFLUENCE ON S/D RESISTANCE IN SHORT CHANNEL MOSFETS, P. Antognetti, C. Lombardi, and D.A. Antoniadis, *Massachusetts Institute of Technology, Cambridge, MA*

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10:45 a.m.

25.5 HIGH RATE ANISOTROPIC ETCHING, R.H. Bruce, G.P. Malafsky, W.W. Yao, and A.R. Reinberg, *The Perkin-Elmer Corporation, Norwalk, CT*

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11:10 a.m.

25.6 A NEW Al PLASMA ETCHING TECHNOLOGY FOR FINE METALLIZATION OF HIGHLY PACKED LSLs, T. Mizutani, H. Komatsu, and S. Harada, *Central Research Laboratory, Hitachi, Ltd., Tokyo, Japan*

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11:35 a.m.
25.7 NOVEL BIPOLAR PROCESS UTILIZING MeV ENERGY ION IMPLANTATION, M. Doken, K. Sakuma, and K. Kajiyama, *Musashino Electrical Communication Laboratory, N.T.T., Musashino-shi, Japan*, and T. Unagami, *Ibaraki, Electrical Communication Laboratory, N.T.T. Ibaraki-ken, Japan*

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SESSION 26: Solid State Devices—Modeling and MOS Devices

Wednesday, December 9, 9:00 a.m.
Jefferson Room

Co-Chairmen: R.S. Muller
 K. Hess

9:00 a.m.
INTRODUCTION

9:05 a.m.
26.1 THREE DIMENSIONAL SIMULATION OF VLSI MOSFETS: THE THREE DIMENSIONAL SIMULATION PROGRAM WATMOS, S. Chamberlain and A. Husain, *Electrical Engineering Department, University of Waterloo, Canada*

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9:30 a.m.
26.2 PHYSICAL MECHANISMS RESPONSIBLE FOR SHORT CHANNEL EFFECTS IN MOS DEVICES, T. Nguyen and J.D. Plummer, *Stanford University, Stanford, CA*

596

9:55 a.m.
26.3 A UNIFIED MODEL FOR HOT-ELECTRON CURRENT IN MOSFETS, P.K. Ko, R.S. Muller, and C. Hu, *University of California, Berkeley*

600

10:20 a.m.
26.4 ELECTRON TRAPPING IN SiO₂—AN INJECTION MODE DEPENDENT PHENOMENON, B. Eitan, D. Frohman-Bentchkowsky, and J. Shappir, *Hebrew University, Jerusalem, Israel*

604

10:45 a.m.
26.5 MODELING OF HIGH-SPEED, LARGE-SIGNAL TRANSISTOR SWITCHING TRANSIENTS FROM S-PARAMETER MEASUREMENTS, Y. Ikawa, W.R. Eisenstadt, and R.W. Dutton, *Stanford University, Stanford, CA*

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11:10 a.m.
26.6 EVALUATION OF THE PERMEABLE BASE TRANSISTOR FOR APPLICATION IN SILICON INTEGRATED LOGIC CIRCUITS, D.E. Snyder and R.L. Kubena, *Hughes Research Laboratory, Malibu, CA*

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11:35 a.m.
26.7 RADIATION-HARD 16K CMOS/SOS CLOCKED STATIC RAM, A. Gupta, M.F. Li, S.C. Su, K.K. Yu, P. Pandya and H.B. Yang, *Hughes Aircraft, Newport Beach, CA*

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SESSION 27: Solid State Devices—III-V Devices

Wednesday, December 9, 9:00 a.m.
Lincoln Room

Co-Chairmen: M.C. Driver
 D.E. Ackley

9:00 a.m.
INTRODUCTION

9:05 a.m.
27.1 GaAs CHARGE COUPLED DEVICES FOR HIGH SPEED SIGNAL PROCESSING APPLICATIONS (Invited Paper), M. Cohen, *Rockwell International Microelectronics Research and Development Center, Thousand Oaks, CA*

622

9:30 a.m.
27.2 OBSERVATION OF TWO-DIMENSIONAL CHARGE TRANSFER IN GaAs, R. Milano, R. Anderson, Y. Liu, E. Sovero, and M. Cohen, *Rockwell International Microelectronics Research and Development Center, Thousand Oaks, CA*

626

9:55 a.m.
27.3 (Ga,Al)As/GaAs BIPOLAR TRANSISTORS FOR DIGITAL INTEGRATED CIRCUITS, D.M. Asbeck, D.L. Miller, R.A. Milano, J.S. Harris, Jr., G.R. Kaelin, and R. Zucca, *Rockwell International Defense Electronics Operations, Thousand Oaks, CA*

629

10:20 a.m.
27.4 SPATIAL AND TEMPORAL CONSTRAINTS ON TRANSPORT IN SUBMICRON GALLIUM ARSENIDE DEVICES, H.L. Grubin, *Scientific Research Associates, Inc., Glastonbury, CT*; G.J. Iafrate, *U.S. Army Electronics Technology and Devices Laboratory, Fort Monmouth, NJ*, and D.K. Ferry, *Colorado State University, Fort Collins, CO*

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10:45 a.m.
27.5 In_{0.53}Ga_{0.47}As/Si₃N₄ N-CHANNEL AND P-CHANNEL INVERSION MODE MISFET'S, A.S.H. Liao, R.F. Leheny, R.E. Nahory, J.C. DeWinter, and R.J. Martin, *Bell Laboratories, Holmdel, NJ*

637

11:10 a.m.
27.6 ELECTRON DRIFT VELOCITIES IN In_{0.53}Ga_{0.47}As AT VERY HIGH ELECTRIC FIELDS, T.H. Windhorn, L.W. Cook, and G.E. Stillman, *Electrical Engineering Research Laboratory, University of Illinois, Urbana, IL*

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SESSION 28: Device Technology—VLSI MOS Technology

Wednesday, December 9, 1:30 p.m.
International Ballroom Center

Co-Chairmen: Y.A. El-Mansy
 D.M. Brown

1:30 p.m.
INTRODUCTION

1:35 p.m.
28.1 VLSI TECHNOLOGIES—A FUTURE PERSPECTIVE (Invited Paper), B.L. Crowder, *IBM Thomas J. Watson Research Center, Yorktown Heights, NY*

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2:00 p.m.
28.2 AN OPTIMALLY DESIGNED PROCESS FOR SUBMICRON MOSFETS, T. Shibata, K. Hieda, M. Sato, M. Konaka, R. Dang, and H. Iizuka, *Toshiba R&D Center, Kawasaki, Japan*

647

2:25 p.m.
28.3 ELIMINATION OF HOT ELECTRON GATE CURRENT BY THE LIGHTLY DOPED DRAIN-SOURCE STRUCTURE, S. Ogura, P. Tsang, W. Walker, J. Shepard, and D. Critchlow, *IBM, Hopewell Junction, NY*

651

2:50 p.m.
28.4 AN MO GATE 4K STATIC RAM FABRICATED USING A NOVEL DIRECT CONTACT TECHNOLOGY, M. Morimoto, E. Nagasawa, H. Okabayashi, and M. Kondo, *Basic Technology Research Lab, NEC, Tokyo, Japan*

655

3:15 p.m.
28.5 CHARACTERIZATION OF MOSi₂-GATE BURIED CHANNEL MOSFETS FOR A 256K-BIT DYNAMIC RAM, T. Tanaka, H. Ishiuchi, Y. Takeuchi, M. Ishikawa, T. Mochizuki and O. Ozawa, *Toshiba Corp., Kanagawa, Japan*

659

3:40 p.m.
28.6 1 μm 256K RAM PROCESS TECHNOLOGY USING MOLYBDENUM-POLYSILICON GATE, S. Nakajima, K. Kiuchi, K. Minegishi, T. Araki, K. Ikuta, and M. Oda, *Musashino Electrical Communications Lab, NTT, Tokyo, Japan*

663

4:05 p.m.
28.7 LEAKAGE CURRENT IN HIGH DENSITY CCD MEMORY STRUCTURES, J. Slotboom, H. Harwig, and M. Pelgrom, *Philips Research Lab, Eindhoven, The Netherlands*

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**SESSION 29: Solid State Devices—GaAs
Transistors and Diodes**

Wednesday, December 9, 1:30 p.m.
Jefferson Room

Co-Chairmen: N.A. Masnari
R.L. Kuvas

1:30 p.m.

INTRODUCTION

1:35 p.m.

29.1 HIGH EFFICIENCY, HIGH POWER X-BAND GaAs FETs, D. Zemack, L. Rosenheck, J. Thompson, and I. Drukier, *Microwave Semiconductor Corporation, Somerset, NJ*

671

2:00 p.m.

29.2 A NOVEL VIA HOLE PHS STRUCTURE IN K-BAND POWER GaAs FET, Y. Hirachi, Y. Takeuchi, T. Matsu-
mura, and K. Ohta, *Fujitsu Ltd., Kawasaki, Japan*

672

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2:25 p.m.

29.3 Q-BAND (26-40 GHz) GaAs FETs, C.H. Oxley, A.H. Peake, R.H. Bennett, J. Arnold, and R.S. Butlin, *Plessey Research Ltd., Caswell, United Kingdom*

680

2:50 p.m.

29.4 MICROWAVE STRUCTURING OF MESFET ELECTRODES FOR INCREASED POWER AND EFFICIENCY, Y. Ren, G. Ruan, and H.L. Hartnagel, *Technische Hochschule, Darmstadt, Germany*

684

3:15 p.m.

29.5 GaAs BEAM LEAD ANTIPARALLEL DIODES FOR mm WAVE SUBHARMONIC MIXERS, G.F. Anderson, C.C. Chang, D.G. Lynch, R.J. Matrecci, F.K. David, and G.I. Roberts, *Hewlett-Packard Co., Santa Rosa, CA*

688

3:40 p.m.

29.6 HIGH PERFORMANCE GaAs BEAM-LEAD MIXER DIODES FOR MILLIMETER AND SUBMILLIMETER APPLICATIONS, J.A. Calviello, S. Nussbaum, and P.R. Bie, *Eaton Corp., AIL Div., Melville, NY*

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