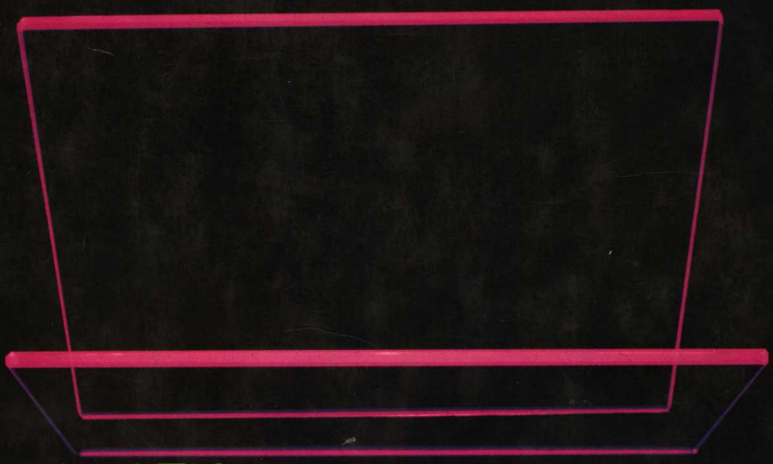

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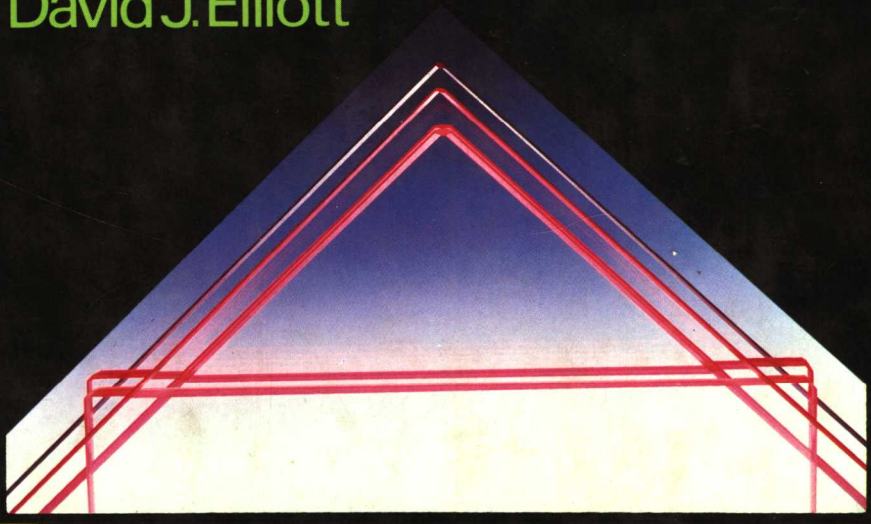

INTEGRATED CIRCUIT MASK TECHNOLOGY

Integrated Circuit Mask Technology

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Preface

This book details the major fabrication steps and many process techniques used to produce high-resolution masks for integrated-circuit fabrication. Processing parameters for the equipment and chemicals used are presented, giving emphasis to practical details and techniques. Many of the physical parameters, the principles and laws governing the behavior of light and electrons, and the other mask process reactions are explained so as to provide a reference framework for mask makers. The aim of this book is to provide a useful source of practical information on mask-making to facilitate better communication of this subject and to improve the quality of the mask-manufacturing processes.

The forces that drive mask technology are reviewed in this book, especially the lithography factors. The charts below summarize both the pattern resolution trends and the lithography technologies used to produce various levels of resolution and wafer throughput.

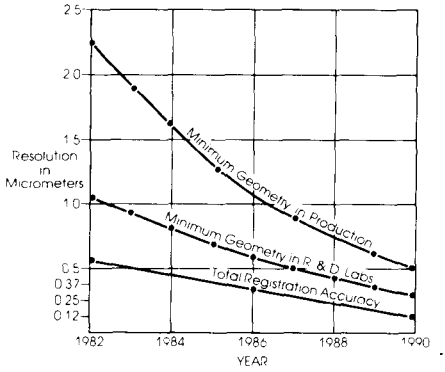

CHART 1 **Integrated circuit feature size and registration control trends (*Semiconductor Information Services, Woburn, Mass.*)**

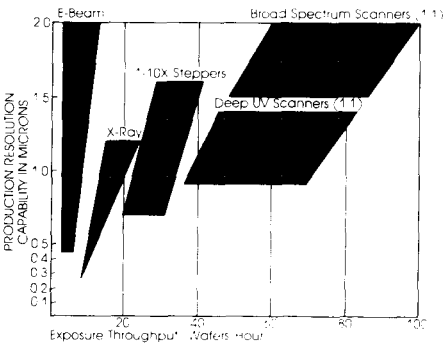

CHART 2 **Wafer exposure system; resolution versus throughput. (*Semiconductor Information Services, Woburn, Mass.*)**

Most experts view lithography as the driving force of both mask and wafer fabrication technology. Special attention has therefore been given in this text to the imaging step in IC fabrication.

David J. Elliott

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Contents

1

Pattern Design and Data Production

INTRODUCTION

The use of computers to provide new device designs has become a matter of fact, and recent very large-scale integration (VLSI) integrated-circuit design has leaned heavily on new and more powerful computing capability. Next-generation components will require even more complexity and utilize more computer time. Computer-aided design (CAD) has grown at an incredible rate, reaching into many fields, including architecture, chemical-experiment design, mathematical modeling, aeronautics, organizational studies, and medicine, to name a few.

The use of CAD in VLSI design is now widespread and extensive, and is considered by many experts to be one of the most well-developed applications of CAD. There are several aspects of VLSI CAD, including

1. Current VLSI CAD capabilities and trends
2. Device modeling
3. Logic simulation, device analysis, and time studies
4. Interconnection strategy
5. CAD relationship to lithographic processes
6. CAD relationship to testing chips and designs
7. Future role of CAD in new devices

The level of integration seems to be a common measure of the rise in integrated-circuit (IC) complexity. Early integrated circuits had up to 10 logic gates, and next evolved into medium-scale integration (MSI) integrated circuits that typically had between 10 and 100 logic gates. Beyond MSI came large-scale integration (LSI) with between 100 and 1000 gates. The current VLSI integrated circuits carry over 1000 gates,

and people are already discussing the next layer of integration as being ultralarge-scale integration (ULSI).

HISTORICAL OVERVIEW

Integrated-circuit fabrication using photolithography started in the early 1950s with pioneering work at Fairchild Semiconductor and Texas Instruments. The basic steps used to conceive, design, test, fabricate, and chip test are essentially the same ones as were used 30 years ago. The method for handling each step has changed considerably, but basic changes have not been introduced. In summary form, these steps are as follows:

1. Define and optimize the IC fabrication and interconnection processes.
2. Electrically define circuit elements.
3. Design logic schematic.
4. Convert logic design to mask patterns (geometries).
5. Electrical test simulation of design to detect flaws.

These steps originally involved many hours of engineering time, since all were performed manually. The pattern dimensions were arrived at by evaluating several different geometries and measuring the yield of each test chip. Final pattern geometries were heuristically derived. After building a chip that met initial yield requirements, tests for rejects, electrical properties, and other parameters were run. The final result of this largely trial-and-error approach was a set of specifications for the electrical parameters and design rules (physical parameters) to match. Tolerances for each geometry were specified as they are today, to keep a maximum yield level.

A given customer, in the 1960s, would begin by putting together a drawing of the chip, called a "logic schematic." This sketch would then be built using discrete-component technology, a process called "breadboarding." Assuming all went well after this step, a layout designer would create the mask-pattern dimensions by drawing a set of mask geometries on paper, one for each level of the process. These drawings were then traced onto Rubylith, a red plastic material made by Ulano that served as the photographic master from which optical reductions were made. The Rubylith patterns were inspected for accuracy against the original drawings of the layout designer, a laborious task. Once again, after making any necessary corrections, the Rubylith masters were "shot" with a large reduction camera and reduced over 100 times to make the final emulsion masks. The devices were then built from the

mask sets, and only after chips were complete could manufacturers get an idea of how their products performed.

In the next decade, as device complexity increased, these manual steps became so cumbersome and labor-intensive that shorter, more effective methods had to be devised to preserve overall process economies. The sheer volume of Rubylith sheets needed in a process area was "eating" an inordinate amount of costly facility real estate. The problem was solved by digitally encoding all the IC pattern geometries. The machine that accomplished this task became known as the optical pattern generator. The actual method involved taking the final drawings and converting them into data tapes. This was done by placing an electromechanical digitizer over the drawings and tracing the circuit pattern.

The major advancement made possible by digitizing the art work was computer handling of the IC pattern data. Now the computerized artwork could be run through a design-rule-check (DRC) program to test for open or short circuits or other design flaws. Once a flaw in the IC pattern artwork was detected, it could be easily changed via the digitizing system. In the earlier example, where Rubylith was used, an entirely new piece of artwork would have to be scribed to correct an error.

Once a series of designer drawings had been converted to digital signals that could be manipulated, corrected, and tested, the job of portraying the images on a screen was tackled. The amount of time saved by digitizing artwork was helpful, but many hours still were needed before a given design could be actually tested for defects. A key shortcut was to use the cathode-ray-tube (CRT) screen for laying out all the IC graphics. In the 1970s, interactive graphics, with the use of computers and screens, helped design engineers actually build prototype arrays much faster. For example, a memory section with many identical elements could easily be generated on the interactive graphics systems. This type of equipment would replicate a given common cell many thousands of times on a given device pattern and arrange or configure the pattern, electronically and rapidly. Prior to the advent of interactive graphics, all such configurations would require hand-drawing. All gate-array and memory-array cells had to be placed individually in the IC artwork. The electronic manipulation of interactive graphics saved hundreds of hours of artwork generation time.

By the mid 1970s, several major problems in IC artwork generation had been solved, namely, the digitizing of engineering drawings and the interactive layout process, both allowing for real-time changes and corrections to original design without replotting or recutting artwork. Further time savings were accrued by rapidly placing the thousands of

identical pattern elements in an array with the use of interactive graphics terminals. Despite these advancements, all IC geometries for all mask levels needed to be "placed in silicon" before actual testing of the device could occur. The need existed, then, for an IC design simulator. The level of device integration was such that individual ICs could not be tested on the chip, and had to be simulator tested.

The next innovation was software to simulate the circuit functions. Many different programs were developed to perform IC simulation, resulting in good verification of the layout designers' work. In addition, the interactive graphics equipment could print out a drawing of the final digitized tape after modifications. An important benefit of this software was the ability to automatically verify the match between design layout metallization or interconnections and the balance of the design. An example of an operator working on an interactive CAD system is shown in Fig. 1-1.

In the 1970s, chips could not be modified, as they are today, to correct a defect or modify the result of a design error. This made it especially important to ensure the accuracy of the complete IC design before sending the artwork into manufacturing. However, ensuring accuracy with computer assistance is a far cry from using a computer to generate an entirely new IC design. Several innovations were needed before the automatic IC CAD system could be put into place. These

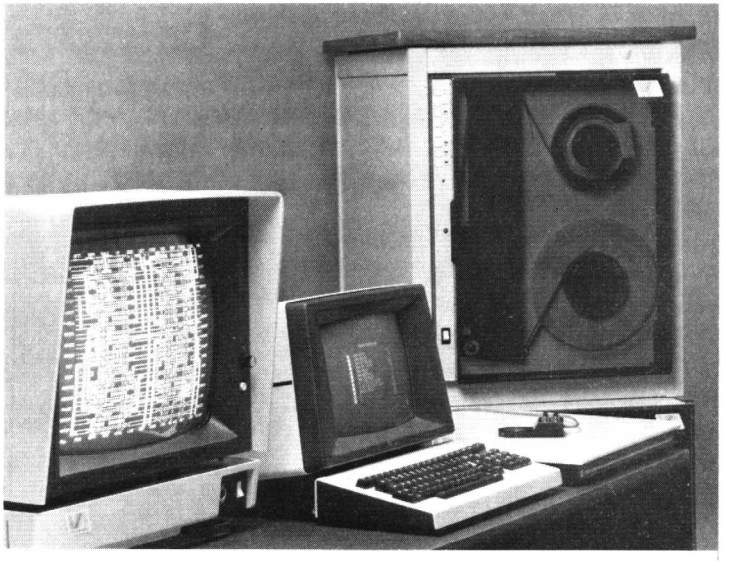

FIG. 1-1 CAD system with interactive graphics. *(VIA Systems, Inc.)*

innovations were assisted by the development of standard cell arrays and gate arrays. From this, Stevens and Hashimoto developed a computer algorithm called the "channel router," which was used to design ICs. Further algorithms were developed to provide the metallization or interconnection patterns for a large number of possible circuit designs.

The increased use of automatic-placement computer programs was helped by newer and simpler design styles. The gate arrays, for example, and other designs with standard cells in a regular pattern were more easily designed because of the repeatability of the units. The gate array, or standard slice, shortened the total design time and did not sacrifice precious silicon real estate in the process. Thus, free-form layout began to give way to automatic design and test programs. All new designs, for the first time, had to be testable *before* they were rendered in silicon. Thus, the responsibility for testing was moved from the postfabrication part of the process to the very beginning. Today, untestable designs are not even considered for possible use.

The overall job of producing first a design and second the data from which masks will be made is complex and involves many individual steps. The basic building blocks used to reach the point of reticle production are shown in Fig. 1-2. Automated design has become mandatory because of the rapid increase in device complexity and the

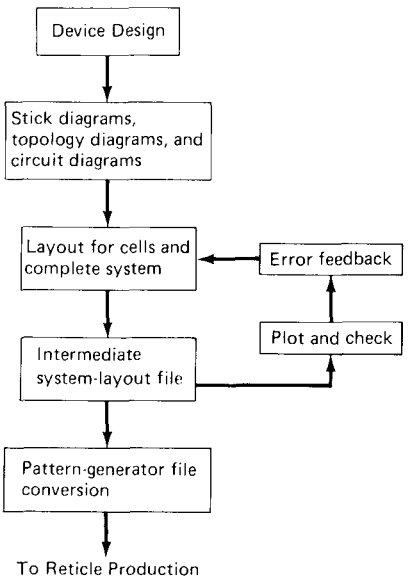

FIG. 1-2 Primary steps in design and data production.

commensurate increase in design time required. A typical 16-bit microprocessor chip requires in excess of 50 worker years of design time alone. The Intel 8086 reportedly required 13 worker years for just the layout phase. An increase in the sophistication of software and hardware has resulted in at least the capability to design even more complex chips than the 32-bit microprocessor. As shown in Fig. 1-3, the design tests are now split into several separate categories, each a separate entity.

COMPUTER-AIDED DESIGN APPROACHES

The design of an integrated circuit is a joint task wherein people utilize computers to perform the necessary functions. The trend toward greater interaction between people and computers has been facilitated by additional software for use with interactive graphics systems. Systems are used where a single operator can completely lay out the electronic parameters for a given VLSI design. The more complex systems save

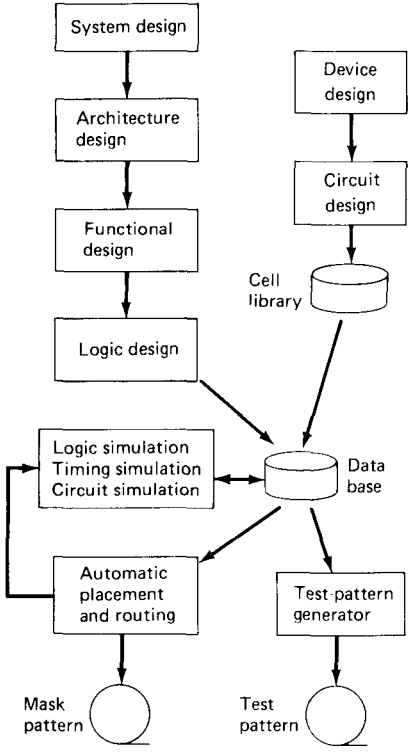

FIG. 1-3 Outline of design tasks. *(Diagram by courtesy of T. Sudo.)*