国外电子信息精品著作(影印版)

片上系统设计

Design of Systems on a Chip: Design and Test

Ricardo Reis
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内 容 简 介

片上系统的研究由来已久，至今仍然保持着很强的生命力，并且越发活跃。该学科涉及面相当广泛，牵涉半导体物理、电路设计理论、仿真软件、算法等各方面，其应用也渗透到电子、通信、控制等方面。

本书内容新颖，实例丰富，全书介绍了芯片核心设计、计算机辅助设计工具、芯片测试方法三个方面，尤其针对基于 SRAM 的可编程门阵列（FPGA）相关的容错技术设计和可测性设计进行了重点的讨论。本书以 FPGA 芯片为例，提出了故障模型和可编程芯片结构中故障造成的严重影响，介绍了现今采用的主要容错设计技术，并对基于 SRAM 的 FPGA 芯片相关的容错设计实例进行分析和研究。本书对于国内芯片可测性设计和分析、电路容错设计、FPGA 芯片设计等领域来说，是一部很有价值的参考书。

该书适应面广，无论对于该学科的专家、教授、研究生，还是本科生、普通技术人员都有极大的参考价值。

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《国外电子信息精品著作》序

20世纪90年代以来，信息科学技术成为世界经济的中坚力量。随着经济全球化的进一步发展，以微电子、计算机、通信和网络技术为代表的信息技术，成为人类社会进步过程中发展最快、渗透性最强、应用面最广的关键技术。信息技术的发展带动了微电子、计算机、通信、网络、超导等产业的发展，促进了生命科学、新材料、能源、航空航天等高新技术产业的成长。信息产业的发展水平不仅是社会物质生产、文化进步的基本要素和必备条件，也是衡量一个国家的综合国力、国际竞争力和发展水平的重要标志。在中国，信息产业在国民经济发展中占有举足轻重的地位，成为国民经济重要支柱产业。然而，中国的信息科学支持技术发展的力度不够，信息技术还处于比较落后的水平，因此，快速发展信息科学技术成为我国迫在眉睫的大事。

要使我国的信息技术更好地发展起来，需要科学工作者和工程技术人员付出艰辛的努力。此外，我们要从客观上为科学工作者和工程技术人员创造更有利于发展的环境，加强对信息技术的支持与投资力度，其中也包括与信息技术相关的图书出版工作。

从出版的角度考虑，除了较好较快地出版具有自主知识产权的成果外，引进国外的优秀出版物是大有裨益的。洋为中用，将国外的优秀著作引进到国内，促进最新的科技成就迅速转化为我们自己的智力成果，无疑是值得高度重视的。科学出版社引进一批国外知名出版社的优秀著作，使我国从事信息技术的广大科学工作者和工程技术人员能以较低的价格购买，对于推动我国信息技术领域的科研与教学是十分有益的事。

此次科学出版社在广泛征求专家意见的基础上，经过反复论证、仔细遴选，共引进了接近30本外版书，大体上可以分为两类，第一类是基础理论著作，第二类是工程应用方面的著作。所有的著作都涉及信息领域的最新成果，大多数是2005年后出版的，力求“层次高、内

容新、参考性强”。在内容和形式上都体现了科学出版社一贯奉行的严谨作风。

当然，这批书只能涵盖信息科学技术的一部分，所以这项工作还应该继续下去。对于一些读者面较广、观点新颖、国内缺乏的好书还应该翻译成中文出版，这有利于知识更好更快地传播。同时，我也希望广大读者提出好的建议，以改进和完善丛书的出版工作。

总之，我对科学出版社引进外版书这一举措表示热烈的支持，并盼望这一工作取得更大的成绩。

中国科学院院士
中国工程院院士
2006 年 12 月

CONTENTS

CHAPTER 1

DESIGN OF SYSTEMS ON A CHIP

Introduction

MARCELO LUBASZEWSKI[1], RICARDO REIS[2], AND JOCHEN A.G. JESS[3]

[1] *Electrical Engineering Department, Universidade Federal do Rio Grande do Sul (UFRGS), Av. Osvaldo Aranha esquina Sarmento Leite 103, 90035-190 Porto Alegre RS, Brazil;*
[2] *Institute of Computer Science, Universidade Federal do Rio Grande do Sul (UFRGS), Av. Bento Gonçalves 9500, Cx. Postal 15064, 91501-970 Porto Alegre RS, Brazil;*
[3] *Eindhoven University of Technology, p.o.box 513, 5600 MB Eindhoven, The Netherlands, Phone: 31-40-247-3353, Fax 31-40-246-4527*

Abstract: This introductory chapter briefly discusses the impacts into chip design and production of integrating highly complex electronic systems as systems on a chip. Technology, productivity and quality are the main aspects under consideration to establish the major requirements for the design and test of upcoming systems on a chip. The contents of the book are shortly presented in the sequel, comprising contributions on three different, but complementary axes: core design, computer-aided design tools and test methods

Keywords: Microelectronics, integrated circuits, VLSI, systems on a chip, cored-based systems, CAD, VLSI testing, design-for-test

1. CHIP COMPLEXITY: IMPACT INTO DESIGN

Chips are nowadays part of every equipment, system or application that embeds electronics. Contrarily to the first decades that followed the transistor invention, the semiconductors market is presently one of the most important segments of the world economy and has become strategic for any country that plans to get some technology independence. In fact, this technology context tends to prevail in next years, since the electronic world will continue expanding fastly through the internet and the wireless communication.

Currently, in a single chip of tenths of square milimeters it is possible to integrate hundreds of thousands of transistors and hundreds of passive components. These chips are real integrated systems and, because of that, they are called systems on a chip. The performance of these systems reaches few gigahertz, while the power

R. Reis et al. (eds.), Design of Systems on a Chip, 1–7.

consumption is of the order of milliwatts. In fact, the growth of the integration density in microelectronics technologies has followed very closely the Moore's Law announced in the sixties: every year the integration density will double, resulting in an exponential growth along the years. Additionally to the increasing electronics density, technology advances have allowed to integrate heterogeneous parts on the same substrate. Digital, analog, thermal, mechanical, optical, fluidic and other esoteric functions can now be put together into the same chip (ITRS, 1999; ITRS, 2003). This obviously adds to chip complexity.

In terms of design, the price to pay for increasing integration scales, densities, performances, functionality, and decreasing sizes and power consumption, is an important growth in the complexity of the design flow. This cost roughly translates into spending more time to produce a new design, or hiring more skilled designers.

In respect to time-to-market, considering the real-life competitiveness, the later a product arrives to market, the lower are the revenues got from. This is illustrated in the simplified model given in Figure 1 (Mourad, 2000).

Starting from the arrival to market, the revenues grow to a peak and then start decreasing to the end of the product cycle. The polygon surface is the total revenues that a product can give along time. A ΔT delay in time-to-market will transfer part of the revenues to competitors, and the maximum instant revenue achievable will thus be decreased by the amount transferred at the delayed arrival time. As shown in the figure, this will drastically reduce the polygon surface and will cause an important loss of revenues.

Regarding the design team, since costs cannot exceed product sales, ways of increasing designer's productivity are preferred to hiring ever more people. Figure 2 reports an increasing gap between circuits complexity and designers productivity (ITRS, 1999).

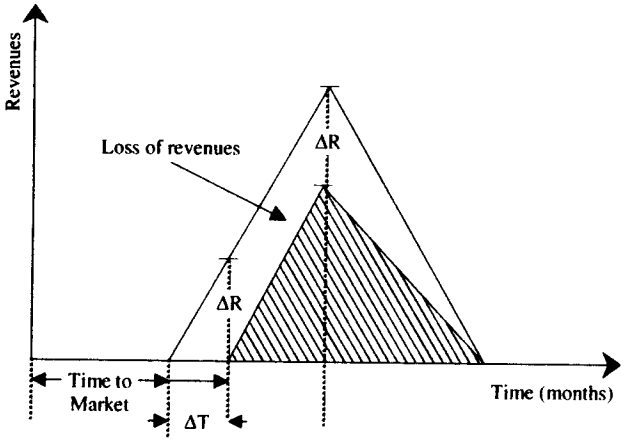

Figure 1. Consequences of time-to-market delays into product revenues

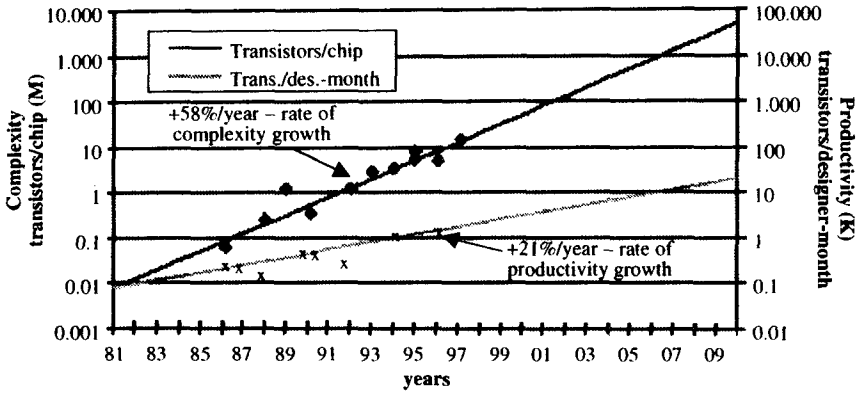

Figure 2. Increasing gap between IC complexity and productivity (ITRS, 1999)

The curves show different growth rates for the number of transistors per integrated circuit and for the number of transistors produced per month by a designer. The former points out to a growth of 58% a year, while the latter only to 21% a year. Reuse and interface standardization initiatives may alleviate the present productivity deficit, but still need to rely on highly automated design environments to cope with the problem.

Typically, state-of-the-art integrated systems are not designed from scratch, designers productivity is enhanced by maximizing reuse. Systems on a chip are currently built from existing microprocessor, memory, programmable logic, mixed-signal, sensor and other pre-designed and pre-verified cores. An appropriate choice of cores, some interfacing work and some user-defined logic design should be enough to customize an integrated system to a given application. However, this system integration work is no simple task. First of all, the selected cores may be described at quite different levels of abstraction: layout, transistor/logic gate netlist, RT level, behavioural HD, etc. Secondly, tools for hardware-software partitioning, for co-simulation, for software compilation, for behavioural, logic and physical hardware synthesis, for design verification and for rapid prototyping shall be available as part of a highly integrated computer-aided design environment to make design possible. Additionally, these CAD tools shall be capable of dealing with hundreds of thousands to a few millions of transistors in an affordable computing time. This can only be feasible if the design environment is highly flexible (accepts descriptions of different levels of abstraction), is highly hierarchical (breaks complexity), allows for step-by-step development (adding details from the system specification to the layout) and makes it possible that detailed design partitions can be dealt with separately and concurrently (improves productivity).

Therefore, design solutions capable to face today's chips complexity shall build around designers with heterogeneous skills (to cope with new technologies), that shall work around core-based systems (to maximize design reuse) and make use

of powerful CAD tools (to improve team productivity). Get to this ideal picture is the challenge that has been faced in last years by many educators, researchers and industrials all over the world.

2. CHIP COMPLEXITY: IMPACT INTO PRODUCTION

Once a new design is ready to go into production, the major features that impact the final fabrication costs are: the integration scale, the transistor density and the chip heterogeneity. They all together determine how complex the integration process, the chip wiring, packaging and testing will be.

To some extent, reuse is also a keyword to make the fabrication of complex chips economically viable. CMOS is definitely the most used technology worldwide. Existing CMOS processes start adding few fabrication steps to allow for the implementation of other than digital functions into the same chip. Analog, optical, mechanical and other functions will ever more join digital, and lead to highly heterogeneous systems on a chip. For specific applications, such as RF, these integrated systems will additionally require special wiring and packaging technologies, increasing even more the chip complexity from the manufacturing point of view.

For a given semiconductor technology, real life chip implementations will be affected by physical defects whose density is a function of the process maturity and the number of fabrication steps. The defects density and the wafer area are the major aspects that determine the fraction of the manufactured chips that will be defect-free. This fraction is known as the IC manufacturing yield. Since the wafer area is increasing constantly, to improve the yield, manufacturers are required, first of all, to understand the existing types of defects. Then, in order to minimize the occurrence of these defects, they need to interfere in the integrated circuit fabrication by improving the various steps of the manufacturing process.

Once the best is obtained from the yield point of view, product reliability can only be further improved by reducing the defect level, that is, the fraction of bad parts that pass the production tests. In practice, low defect levels can only be obtained through tests that provide high fault coverage.

In general, developing and applying these tests take long times and may delay the introduction of the product into the market. Thus, according to the time-to-market model of Figure 1, if it causes delays, and also incurs cost, it turns hard to justify testing on a purely financial basis. However, one should consider that this model does not account for the loss of revenues due to rejects because of problems in the final product. Figure 3 proposes a more realistic model, where product quality, represented by the slopes q and Q, is added to the model of Figure 1: the better the product quality, the greater the slope angle. Then, one can notice from the figure that, although a slight delay may come out due testing reasons, the loss of revenues may be largely compensated for better quality.

As traditional methods, based on external functional tests, continue to be used for increasingly complex systems on a chip, it becomes ever more evident how hard it turns to get good market shares through time and product quality tradeoffs.

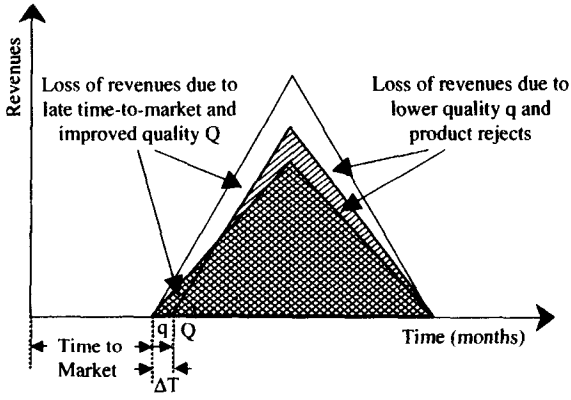

Figure 3. Consequences of rejects into product revenues

State-of-the-art chips have a much larger number of transistors per pin, what makes it much more difficult the access and control of internal nodes by an external tester. This limited access and control leads to a substantial increase in test application times.

Additionally, since these chips operate at much higher frequencies, at-speed testing may only be feasible by using extremely expensive testers that, according to (ITRS, 1999), will cost more than US$20M by the year 2014. The curves in Figure 4 show up how this situation will probably evolve if traditional methods continue dominating the testing scenario: the costs for transistors fabrication will continue falling down and the costs for transistors testing will grow up along the

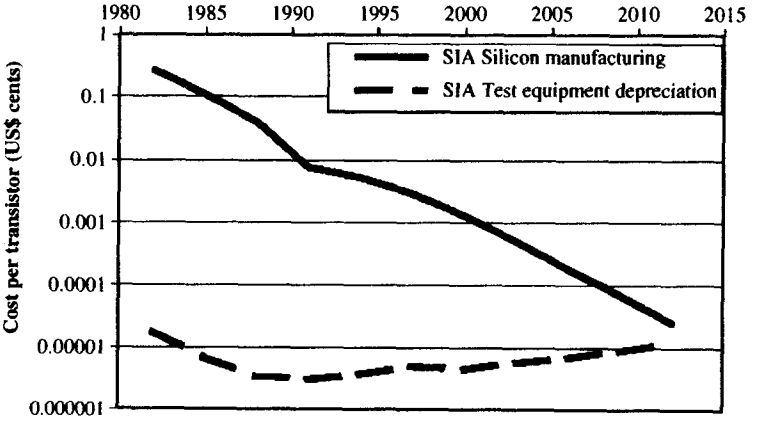

Figure 4. Cost per transistor in microprocessors: fabrication versus testing (ITRS, 1999)

next years (ITRS, 1999; ITRS, 2003). This means that, by the year 2012, testing will start dominating production costs and product competitiveness will establish around cheaper test techniques yet capable of ensuring product quality.

Design-for-test (DfT), that implies moving part or all tester functionalities into the chip, points out as the only viable solution to reduce the tester capability requirements and therefore, the cost of the manufacturing test equipment. Additionally, the use of structured and hierarchical DfT approaches, that provide the means to partition the system and to test multiple parts concurrently, may enable higher fault coverage and shorter test application times. The impact of chip complexity into production may thus be alleviated by DfT, as it ensures product quality at lower costs and simultaneously prevents test from dominating time-to-market (ITRS, 2003).

3. THE SECOND BOOK: DESIGN AND TEST

This book is the second of two volumes addressing design challenges associated with new generations of the semiconductor technology. The various chapters are the compilation of tutorials presented by prominent authors from all over the world at workshops in Brazil in the recent years. In particular, this second book deals with core design, CAD tools and test methods.

To start with cores, a collection of contributed chapters deal with the heterogeneity aspect of designs, showing the diversity of parts that may share the same substrate in a state-of-the-art system on a chip. Three chapters address mixed-signal cores, in particular microsystems embedding electrical and non-electrical parts, and purely digital cores, such as multimedia processors, conventional microprocessors and reconfigurable logic. In Chapter 2, J. M. Wilkinson discusses the evolution, types, fabrication and application of modern microsystems, including examples of technological strategies suitable for small and medium size high-tech companies. Chapter 3, by J. A. G. Jess, reviews the relevant features of digital media applications, discusses core architectures for multimedia processing and addresses the question of software design for these architectures. In Chapter 4, F. Anceau presents the extraordinary evolution of microprocessors to our days, and discusses the challenging future of these devices to keep the evolutionary rate of computing power and binary code compatibility.

Then it comes the turn of computer-aided design tools. The second part of this book discusses CAD in three very different levels of design abstraction. Chapter 5, by R. Reis, J. Güntzel and M. Johann, looks at the various requirements that physical synthesis tools have to meet, such as layouts with smaller silicon areas, shorter signal delays and lower power consumptions, for implementation in submicron technologies. R. A. Bergamaschi, in Chapter 6, tackles the problem of designer's productivity by proposing synthesis algorithms for behavioural descriptions, and by discussing the main advantages and drawbacks of behavioural synthesis along with its insertion into the overall digital design methodology. Finally, in Chapter 7 A. Jerraya and co-authors discuss how, starting from the system specification level,

a heterogeneous architecture composed of software, hardware and communication modules can be generated by means of a co-design tool.

The third and last part of this book, composed of four chapters, deals with test methods. In this collection of chapters, the topic is addressed from various different viewpoints: in terms of chip complexity, test is discussed from the core and system prospective; in terms of signal heterogeneity, the digital, mixed-signal and microsystem prospective are considered. The fundamentals and an overview of the state-of-the-art test and design-for-test methods are given in Chapter 8 by M. Lubaszewski. In Chapter 9, D. W. Bouldin discusses the need, while migrating from a FPGA prototype to an ASIC implementation, to integrate on-chip design-for-test methods that enable to screen out manufacturing defects. H. G. Kerkoff addresses in Chapter 10 test reuse in microsystems and test innovations brought in by the embedded sensors and actuators. Y. Zorian wraps up this part of the book by presenting, in Chapter 11, the challenges of testing core-based system-chips and the corresponding testing solutions for the individual cores and the complete system.

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CHAPTER 2

MICROSYSTEMS TECHNOLOGY AND APPLICATIONS

J. MALCOLM WILKINSON

Technology For Industry Limited, 6 Hinton Way, Wilburton, Ely Cambs. CB6 3SE, U.K., Tel: +44 1353 741 331 Fax: +44 1353 740 665, e-mail: tfi@dial.pipex.com

Abstract: Microsystems are intelligent miniaturised systems comprising sensing, processing and/or actuating functions, normally combining two or more electrical, mechanical or other properties on a single chip or multi-chip hybrid. They provide increased functionality, improved performance and reduced system cost to a large number of products. This tutorial will provide an overview of the evolution, types, fabrication and application of modern microsystems including examples of technological strategies suitable for direct utilisation by small and medium size high-tech companies. The tutorial is divided into the following sections: Fabrication, Packaging Technology, Design and Test, Applications for Microsystems, Factors Limiting Exploitation, Business Strategies for Microsystems Companies

1. INTRODUCTION

The world has been changed dramatically by the integrated circuit, which is now the heart of so much electronic equipment. In the 1980s an important development took place when the same technology, which had been used to make integrated circuits, started to be used to make sensing devices and mechanical components from the same starting material – silicon. During the next ten years, pressure sensors, temperature sensors, imaging devices and a variety of more sophisticated sensors were developed.

The first steps were also taken towards the fabrication of actuators such as valves, pumps and moving mirrors. By the early 1990s it was clear that by integrating sensors, signal processing electronics and actuators together, a complete MICROSYSTEM could be formed on one silicon chip.

The benefits of microsystems stem from the use of the same batch fabrication manufacturing methods which have evolved so efficiently to produce conventional integrated circuits. The technology allows thousands of identical devices to be fabricated at the same time with mechanical tolerances at the micron level and almost identical electrical properties. The batch fabrication processes promise lower cost,

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better performance, smaller size and improved reliability compared with discrete sensors fabricated with technology which pre-dates the microchip era.

Another interesting development has been the use of other materials than silicon to create microstructures. LIGA technology can be used to form mechanical structures in plastic or metal using a combination of X-ray lithography, plating and moulding. This particular technique has found favour because it allows a larger variety of high aspect-ratio shapes to be formed [a few microns wide and up to several hundred microns deep] and although the lithography stage is expensive, the subsequent electroforming and moulding can replicate low cost components from one master structure.

Covering the silicon layers of a microstructure with other materials has enabled a wider variety of sensing structures to be developed. For example, magnetic materials, piezo-electric materials, electro-optic materials and biosensitive materials

Table 1. Classification of Microsystems and Example

Physical Domain	Input Device	Output Device
Mechanical	Airbag accelerometer	Tilting mirror display
Optical	Micro spectrometer	FED display
Fluidic	Airflow sensor	Ink-jet printer
Thermal	Temperature sensor	Bubble-jet printer
Magnetic	Disk Read/Write head	Magnetic ink printing

Table 2. Applications of Microsystems enabled by Low Power VSLI

Product Application	Technical Features
Cochlear Implant	bio compatible packaging long battery life signal coupling through skin small size
Smart Medical Card	long battery life magnetic or optical data I/O large memory capacity small height components
Portable Navigation System	low cost gyroscope long battery life cellular radio/satellite receiver
Remote environmental monitoring	low power radio link self calibrating systems high stability sensors
Implanted Drug Delivery Systems	reliable fluidic devices low power radio/optical links syringe rechargeable reservoirs

are being used to produce devices such as magnetic disk read-write heads, gas sensors, optical switches and sensors for enzyme-catalysed reactions.

Microsystems can be classified by the particular physical domain in which they operate. Table 1 below shows these classifications and gives examples of microstructures from each.

The combination of smart microsystems with low power VLSI will enable many new products to be developed with large market potential. Table 2 gives examples of such products and lists the technical features which will be required.

2. FABRICATION TECHNOLOGY

It is assumed that the reader is familiar with the basic techniques of integrated circuit manufacture such as photolithography, etching, metal deposition, dielectric deposition and polysilicon deposition. In this section we discuss how these basic techniques have been adapted to produce silicon bulk microstructures, and silicon surface microstructures. We also cover the complementary techniques of LIGA and placing additional layers above integrated circuit structures [so-called ABOVE – IC processes].

2.1 Silicon Bulk Micromachining

This technique involves the removal of most of the bulk of the silicon wafer to leave behind the desired structure on the front surface. It can be contrasted with silicon surface micromachining which leaves the wafer intact but builds up additional silicon layers on the surface. Figure 1 shows a bulk micromachined structure designed to accurately locate optical fibres (photo courtesy of IMC, Sweden).

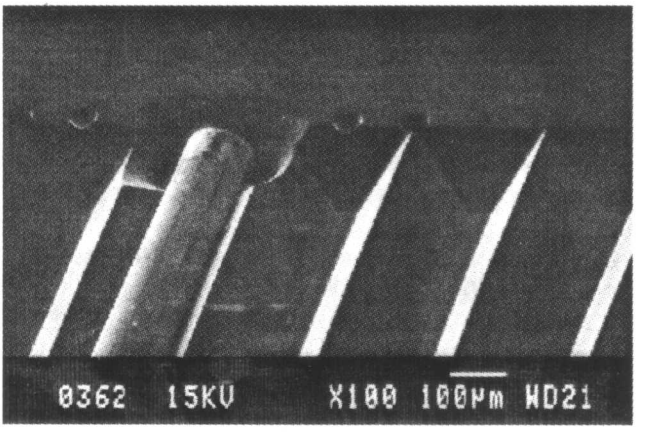

Figure 1. Etched V grooves in silicon