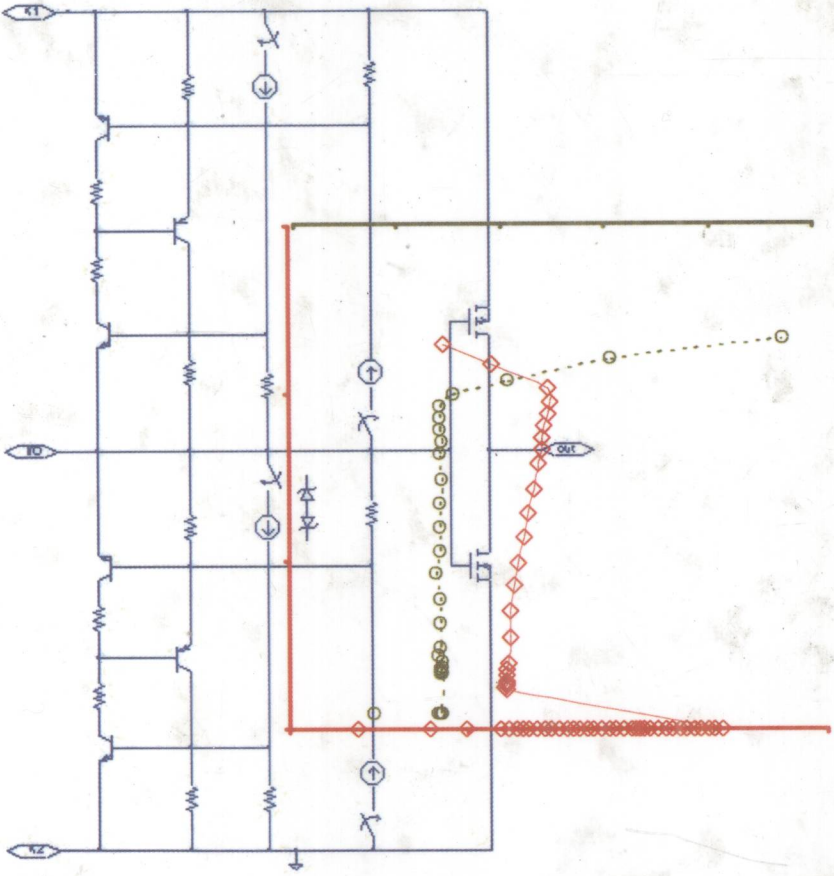
ON-CHIP ESD PROTECTION FOR INTEGRATED CIRCUITS

An IC Design Perspective



Albert Z. H. Wang

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by

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TO MY PARENTS AND FAMILY

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Preface

The author first got in touch with the ESD things in late 1996 when he was a Staff R&D Engineer at the National Semiconductor Corporation, where he was assigned by the boss to develop some on-chip ESD protection circuits for mixed-signal IC chips. Ever since then, the not-so-attractive ESD protection circuit design topics have been on and off the author's table both at the company's cubicle and in the office at the Illinois Institute of Technology, where the author joined its faculty team of Electrical and Computer Engineering in Fall 1998. Exactly like all the other IC designers, the author does not really like the little ESD thing and has no fun in doing ESD protection circuit design. Unfortunately, life is life. One has to deal with some unpleasant issues sometime somewhere somehow. The harsh reality is that an IC designer must find the right ESD protection solution for the IC chips. If there is no ESD protection provided, nobody will buy your chips. If there is no sufficient ESD protection for your chips, you will lose the market to your competitors. Period! What makes an IC designer's life even more miserable is the fact that as IC technologies advance, the customer demands for IC ESD robustness and the complexity of on-chip ESD protection circuit design increase dramatically, as evidenced by the huge amount of related papers published in the past decade. While significant progresses have been made in the field of ESD protection research and design, IC designers are deeply bothered by the situation that there are too much qualitative sayings and too few quantitative analyses on the ESD protection design matters. Hence, very little success in predicting ESD protection circuit design is expected. One question commonly heard in the IC circuit design community is that "*how do I design the ESD protection for my chips, with prediction, as a circuit designer?*" This book tries to

provide the information necessary to address this tough design challenge from an IC circuit designer's angle.

From IC designers' viewpoint, it is not enough to talk about ESD protection design in the process and device physics language only; and it is unacceptable to continuously rely on the traditional, non-predictive, trial-and-error approaches in ESD protection circuit design practices. Since ESD protection phenomena involve complex multiple level process-device-circuit-electro-thermal coupling effects, the task of ESD protection design is not really about designing a stand-alone ESD protection structure itself. One ought to take into account of the complex interactions between the ESD protection structures and the core circuits being protected in order to successfully achieve full chip level ESD protection. An IC designer ought to be enabled to perform full-scale simulation in order to conduct predictive ESD protection circuit design. With these considerations, the book starts with introduction of ESD protection fundamentals including the ESD origins, ESD test models and standards, etc. It moves on to describe the basic ESD protection devices. ESD protection circuit solutions and advanced ESD protection concepts are then discussed in great details. With these preparations, predictive ESD protection simulation-design methodologies and case studies on the complex ESD-to-circuit interactions are presented. A group of practical ESD protection circuit design examples are provided to enhance the theoretical discussions. Finally, the book concludes with a brief summary on current and future work on ESD protection circuit design. The author wants to point it out clearly to IC designers that, please never try to copy a successful ESD protection circuit, either from this book or anyone else, onto your chips. Most of the time, it will not work for you. It is important to understand that ESD protection circuit design is a custom design and is not portable. It is extremely important to treat ESD protection design as a circuit design task and to conduct ESD design simulation as much as possible. After all, describing a problem quantitatively is more scientific than speaking qualitatively.

An IC designer's best wishes to fellow IC designers: Good Luck!

Albert Z. H. Wang
Illinois Institute of Technology
Chicago, October 2001.

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Chapter 1

INTRODUCTION

1.1. A LITTLE HISTORICAL STORY

Electrostatics, or, static electricity, is as old as the time itself. Let us take a quick look into the ancient past. In 600 BC, Greeks discovered static electricity in basic experiments, where they rubbed Amber with a piece of fur and observed attraction of lightweight objects to the Amber. That might not be the very first observation of static electricity generation, however, was believed to be the first documented experiment. Interestingly, the English word "electron" derived from the Greek word "electron" for Amber. Serious work on static electricity might have started with the publication of DeMagnete in 1600 by Gilbert, who also made up the word "electricity". Understandings of modern concepts of static electricity were established after a few more centuries of research activities conducted by Gauss, Coulomb, Faraday, etc. Among them, the famous experiments include that performed by Franklin in 1752, as shown in Figure 1.1, when he flew a kite during a storm and observed the Leyden jar placed close to one end of the kite's wire being charged up; and that conducted by Hertz in 1886, as illustrated in Figure 1.2, where he realized wireless communication by using electrostatic discharge (ESD) devices as transceivers. Interested readers can readily find the detailed information by visiting a Science Museum.

Protection against ESD-caused damages also has a long and rich history as that of taking use of electrostatic discharges. As early as in the fifteenth century, European military agencies started to use a variety of means to handle munitions safely. The lightening rod, invented by Franklin soon after his famous kite experiment, which still benefit us all today, was certainly one of the most significant ESD protection devices in the scientific history.

Figure 1.1 Franklin's kite test in 1752 showing lightening is an ESD event.

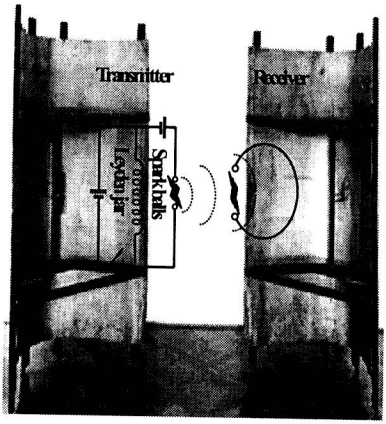

Figure 1.2 Hertz's transmission work in 1886 using ESD spark balls.

Back to today, one could hardly not experience some kind of ESD events in our everyday life. For example, most of us may have experienced the shocking sparks when touching a door handle of a car once and again. One can never image how our everyday life could be without static electricity; meanwhile, one should never overlook the kind of damages caused by ESD as well.

1.2. ESD FAILURE – AN IC RELIABILITY PROBLEM

The ESD problem became a real issue after World War II as highly insulating polymeric materials found widespread usage where substantial static charge accumulation might cause machinery shut downs. However, the devastating ESD damage problem was not taken into serious consideration until the modern microelectronics technologies took the role in our everyday life, which is how ESD failure problem became relevant to semiconductor IC technologies. With the invention of semiconductor transistor in 1947 and development of metal-oxide semiconductor (MOS) technologies in the 1960s, the impact of the invisible ESD phenomena, with a level lower than 1000 volts, became materialized. Some electronic devices can be damaged by an ESD transient of as low as 10 volts. The electronic component and

system failures due to ESD events in the electronics industry escalated almost exponentially in the 1970s. Consequently, the military began to develop related standards to govern ESD immunity of electronic products. Particularly, ESD failure is a profound reliability problem to integrated circuits (IC) and poses a grand challenge to the semiconductor industry. This IC ESD failure problem and the ESD protection solution are the topics of this book. As the semiconductor IC technologies advances into the very-deep-sub-micron (VDSM) regime, IC parts become increasingly susceptible to ESD damages. Statistics indicated that up to 30% of all IC failure might be attributed to ESD, as illustrated in Figure 1.3 [1], which costs the semiconductor industry billions of U.S. dollars annually [2]. Such ESD-induced failures are either catastrophic or latent in nature, with the former causes immediate IC malfunction and the latter leads to future failure and lifetime problem. The nature of ESD failures is associated with either high power, i.e., high current, which causes thermal damages to semiconductors and metal interconnect, or, high electric field that ruptures dielectric thin films in ICs. Accordingly, appropriate ESD protection means are developed to protect IC parts against ESD damages.

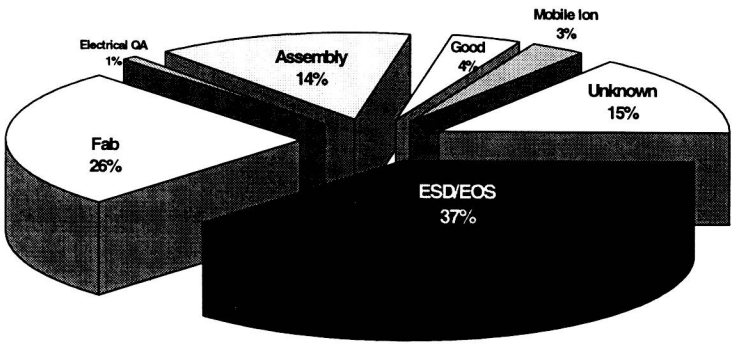

Figure 1.3 Industrial failure analysis reports substantial IC failure rate due to ESD (data from National Semiconductor Corporation) [1] (*Reproduced here by kind permission of the ESD Association and authors*).