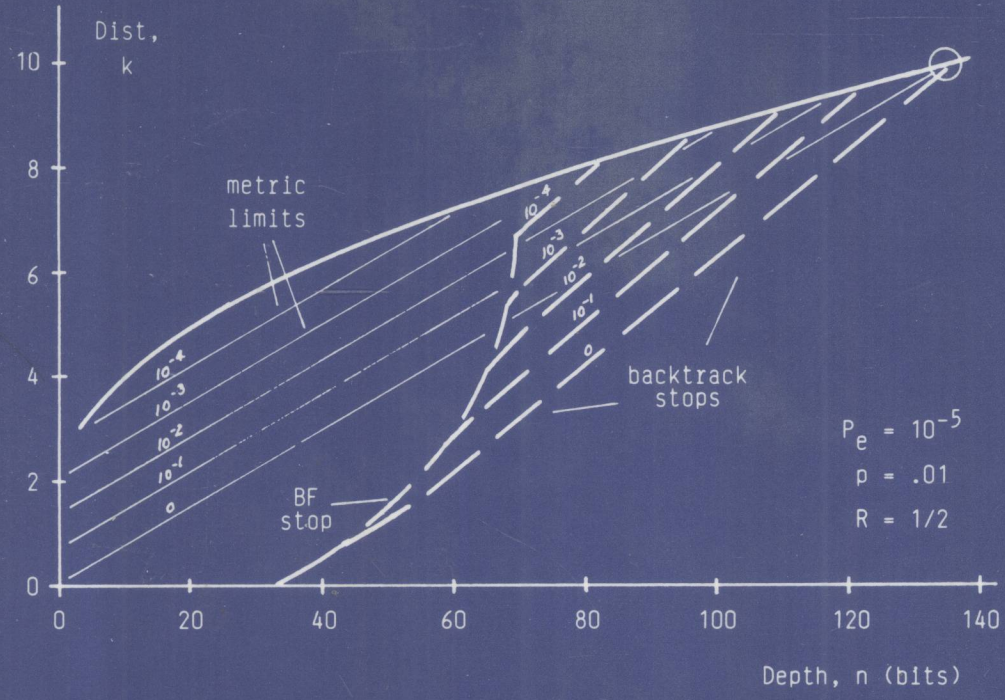
CIRCUIT DESIGN FOR CMOS VLSI



John P. Uyemura

CIRCUIT DESIGN for CMOS VLSI

by

John P. Uyemura
Georgia Institute of Technology

Kluwer Academic Publishers
Boston/Dordrecht/London

Distributors for North America:
Kluwer Academic Publishers
101 Philip Drive
Assinippi Park
Norwell, Massachusetts 02061 USA

Distributors for all other countries:
Kluwer Academic Publishers Group
Distribution Centre
Post Office Box 322
3300 AH Dordrecht, THE NETHERLANDS

Library of Congress Cataloging-in-Publication Data

Uyemura, John P. (John Paul), 1952-
Circuit design for CMOS VLSI / by John P. Uyemura.
p. cm.
Includes index.
ISBN 0-7923-9184-5 (acid free paper)
1. Integrated circuits--Very large scale integration. 2. Metal oxide semiconductors, Complementary. 3. Electronic circuit design. I. Title.
TK7874.U93 1992
621.39'5--dc20 91-33124
CIP

Printed on acid-free paper.

Printed in the United States of America

CIRCUIT DESIGN FOR CMOS VLSI

Foreword

During the last decade, CMOS has become increasingly attractive as a basic integrated circuit technology due to its low power (at moderate frequencies), good scalability, and rail-to-rail operation. There are now a variety of CMOS circuit styles, some based on static complementary conductance properties, but others borrowing from earlier NMOS techniques and the advantages of using clocking disciplines for precharge-evaluate sequencing. In this comprehensive book, the reader is led systematically through the entire range of CMOS circuit design. Starting with the individual MOSFET, basic circuit building blocks are described, leading to a broad view of both combinatorial and sequential circuits. Once these circuits are considered in the light of CMOS process technologies, important topics in circuit performance are considered, including characteristics of interconnect, gate delay, device sizing, and I/O buffering. Basic circuits are then composed to form macro elements such as multipliers, where the reader acquires a unified view of architectural performance through parallelism, and circuit performance through careful attention to circuit-level and layout design optimization. Topics in analog circuit design reflect the growing tendency for both analog and digital circuit forms to be combined on the same chip, and a careful treatment of BiCMOS forms introduces the reader to the combination of both FET and bipolar technologies on the same chip to provide improved performance.

Both designers new to CMOS as well as those with considerable experience will find a rich selection of topics in this up-to-date book, written in a style that is thoughtful, detailed, and broad from the system perspective. Readers can have confidence that designs based on these well-taught principles will produce circuits of outstanding contemporary performance for increasingly demanding applications.

Jonathan Allen
Consulting Editor

Dedication

This book is dedicated to the ladies in my life:

Melba Valerie Uyemura
(my wife)

Ruby Shizue Uyemura
(my mother)

Valerie Elizabeth Hanako Uyemura
(my daughter)

for their love and encouragment.

植村

Preface

The field of CMOS integrated circuits has reached a level of maturity where it is now a mainstream technology for high-density digital system designs. This book deals with circuit design in an integrated CMOS environment. Emphasis is placed on understanding the operation, performance, and design of basic digital circuits such as logic gates, latches, and adders. The topical outline and the level of presentation has been gauged such that the book should be of use to both students and practicing engineers.

CMOS admits to a wide variety of design variations. While static logic is the most common, powerful dynamic system design styles have been developed and applied to improve performance and packing density. When selecting the material for the book, the topics were examined for unique or interesting circuit/systems techniques, useful application examples, and the occurrence of a particular subject in the open literature. Once the topics were chosen for inclusion in the book, decisions on the length and depth of the presentation had to be made. In general, the discussions center around the basic operational and design concepts, with circuit examples to reinforce the material. References are provided at the end of each chapter if more details are needed.

No specific knowledge of CMOS circuits is assumed; however, some background in electronics and integrated circuit fabrication and layout is required to understand some of the more advanced sections. A general treatment of digital ICs at the level of **Analysis and Design of Digital Integrated Circuits** (Hodges and Jackson, McGraw-Hill) is sufficient. Georgia Tech offers a 2-quarter sequence in digital MOS IC design. The first course uses the textbook **Fundamentals of MOS Digital Integrated Circuits** (Uyemura, Addison-Wesley), and centers around the basics of circuits, devices, and chip design. The second course has evolved to the point where it is exclusively devoted to CMOS using this book and the current literature.

This book attempts to present a field which has evolved from a highly specialized technique to the dominant silicon technology over a span of twenty-plus years. It is difficult to give complete discussions of all of the topics which are covered. Hopefully, the knowledge gained from reading the book will be worth the investment of time. I apologize for all errors and omissions in the writing; even with a CMOS-based microcomputer, these problems seem to persist!

Acknowledgments

I would like to thank the reviewers who spent many hours reading the original manuscript. Professor Charles Zukowski (Columbia University) did a amazingly thorough job analyzing the approach, content, and writing. His detailed analyses was a great help when preparing the final version. Professor M. Annaratone (ETH, Zurich; DEC) deserves a special note of thanks. The original proposal for this project was an updating of his earlier title **Digital CMOS Circuit Design** (Kluwer, 1986). However, as the writing progressed, the book took on distinct characteristics of its own due to the dynamic evolution of the field. In spite of the obvious divergence from the original plan, Professor Annaratone graciously read and provided thoughtful comments on the entire manuscript. Professor Reginald J. Perry (FSU/FAMU) also caught many errors in the original manuscript.

Mr. Carl Harris of Kluwer has constantly given encouragement and support to this project. I have watched Carl take Kluwer from a small start-up operation to one which is a leading publisher in the field of advanced electrical and computer engineering. I congratulate him on his success, and am happy that this book can be added to his growing list of titles.

I would like to thank my wife Melba for her love and support during yet another long writing project. Although lost hours can never be regained, she still remains enthusiastic about my work. My parents, Reverend George and Ruby Uyemura, have always supported me in everything I have ever attempted. On this, the occasion of their 50th wedding anniversary, I again extend my love and thanks. Finally, I would like to thank my little Valerie for her help during the writing. She always keeps me in line by making it clear when it is time to stop work and start playing with her and *Bear*. Watching her grow and learn has taught me what is really important in life.

J. P. Uyemura
Atlanta, GA

Contents

Chapter 1

Introduction to CMOS

Integrated electronic circuits which are based on complementary metal-oxide-semiconductor (**CMOS**) technologies are firmly established in modern electronics. CMOS provides the important characteristics needed for high-density logic designs. Moreover, with recent developments in the field of BiCMOS, it is anticipated that we have a technology which will provide a transition to the next century.

In this chapter we will examine CMOS from a bird's eye vantage point in an effort to place the subject into a reasonable perspective. Then we will be in a position to discuss the content and structure of the book.

1.1 Why Study CMOS?

CMOS circuits have many advantages when compared with other integrated circuit technologies. The ones which are most often quoted are

- Low power dissipation
- High integration density

but there are other reasons which make silicon CMOS the technology of choice for many applications. Let's examine some of the more important aspects of the technology.

Power Dissipation

Static CMOS circuits have the nice characteristic that power supply current is only required when a gate is undergoing a switching event. If the inputs are at stable logic 0 or logic 1 values, then the static power dissipation P_{static}

is limited to that generated by leakage currents. When compared with nMOS or bipolar circuits, this is a distinct advantage since it leads to reduced heating.

Although the static power dissipation in a CMOS circuit is very small, the circuit exhibits dynamic dissipation whenever the inputs are changed. The power consumption of a switched network is proportional to the switching frequency:

$$P_{dynamic} \propto f. \tag{1.1}$$

The total power dissipation P of the circuit is then written as

$$P = P_{static} + P_{dynamic}. \tag{1.2}$$

At low frequencies, both contributions are small. However, the dynamic power dissipation increases with switching frequency, and can dominate in high-speed circuits. At the system level, the total power dissipation depends on both the frequency of the switching and the number of gates which are undergoing a transition.

High Logic Integration Density

CMOS circuits can be structured in various ways. Standard static CMOS gates require two transistors for every input. Thus, a 3-input NAND or NOR gate will use 6 MOSFETs. An equivalent nMOS-only design uses 4 transistors, so we can conclude that CMOS does not lead to a smaller device count. Instead, the size of the device becomes the important consideration. CMOS circuit design allows us freedom to adjust the size according to the desired transient response specifications. This results in a tradeoff between speed versus area.

Advances in silicon processing technology have been instrumental in propelling CMOS to the forefront of integrated circuits. Linewidths as small as one-half of a micron are possible using optical lithography; x-ray and electron-beam patterning allows 0.1 [μm] resolution. Logic density is increased as the device size decreases, allowing CMOS to achieve greater integration densities than possible with a bipolar technology. These features have helped propel CMOS to a leading technology.

Logic Swings

CMOS gates allow **rail-to-rail** output logic voltage swings. For example, if a 5 volt power supply is used, then the output voltage range is (approximately) [0,5] volts. As a comparison, a bipolar TTL (transistor-transistor logic) gate only gives outputs in the range [0.3,3.6] volt with the same