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VLSI for Pattern Recognition and Image Processing

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Preface

During the past two decades there has been a considerable growth in interest in problems of pattern recognition and image processing (PRIP). This interest has created an increasing need for methods and techniques for the design of PRIP systems. PRIP involves analysis, classification and interpretation of data. Practical applications of PRIP include character recognition, remote sensing, analysis of medical signals and images, fingerprint and face identification, target recognition and speech understanding.

One difficulty in making PRIP systems practically feasible, and hence, more popularly used, is the requirement of computer time and storage. This situation is particularly serious when the patterns to be analyzed are quite complex. Thus it is of the utmost importance to investigate special computer architectures and their implementations for PRIP. Since the advent of VLSI technology, it is possible to put thousands of components on one chip. This reduces the cost of processors and increases the processing speed. VLSI algorithms and their implementations have been recently developed for PRIP. This book is intended to document the recent major progress in VLSI system design for PRIP applications.

West Lafayette, March 1984 *King-sun Fu*

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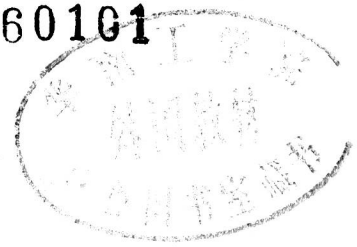

1. Introduction

K.S. Fu

1.1 VLSI System

The Very Large Scale Integration (VLSI) technology [1.1] enables many hundreds of thousands of switching devices to be placed on a single silicon chip with feature sizes approaching 1 micrometer. This advancement of IC technology promises the usage of much-smaller-sized transistors and wires, and has also increased the density of the circuitry. In addition, the reduced size results in faster and/or lower power operations [1.2,3].

Some commercial examples are: Motorola's MC68000 or the 64 K memory chip, HP's 32-bit CMOS processor [1.4] and Intel's iAPX-432 processor [1.5]. As for research projects, RISC [1.6] and MIPS [1.7] are general purpose processors designed to be implemented on a single VLSI chip. These two projects emphasize processors with reduced and simple-instruction sets, they can achieve high throughput. Note that all the systems mentioned so far are sequential computers. The X-tree system [1.8], on the other hand, is a MIMD type parallel computer with each processor, the so called X-node, built upon a single VLSI chip. The systolic searching tree [1.9] is a binary tree-structure system designed for easy implementation with VLSI technology. This tree system is efficient for search problems and operates in a SIMD node.

Special VLSI chips are usually constructed only when they can solve a problem satisfying two criteria; the problem is currently very time-consuming, and the proposed special-purpose device is much more efficient than conventional ways of solving this problem. Therefore, almost all the specially designed VLSI chips take advantage of pipelining and parallelism. The most significant contribution in this area is the concept of a systolic array and many of its applications [1.10,11]. Figure 1.1 demonstrates six different VLSI architectures. The first three parts Fig.1.1a-c, are also called mesh-connected processor arrays. These arrays have simple and regular interconnections, which lead to cheap implementations and high densities. High density implies both high performance and a low overhead for support components. The numerous

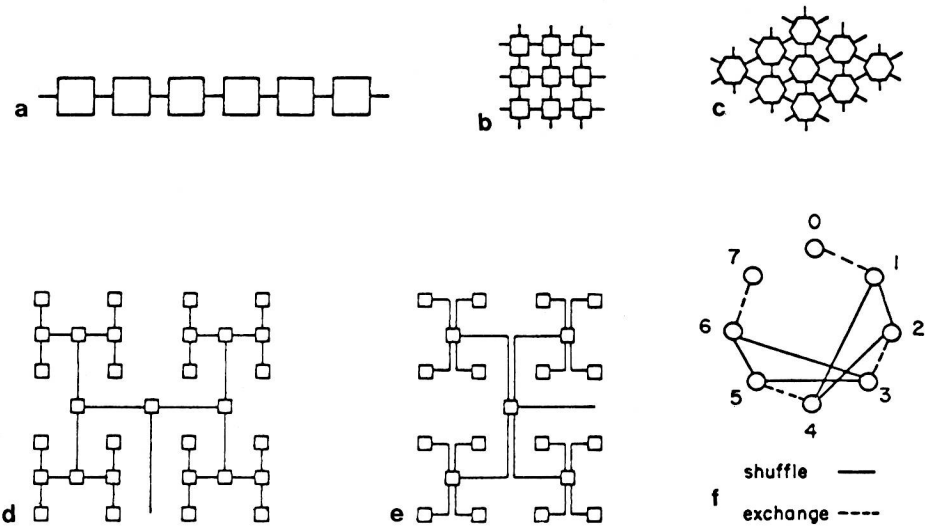

Fig.1.1a-f. VLSI system architectures. a) A one-dimensional linear array; b) a two-dimensional square array; c) a two-dimensional hexagonal array; d) a binary tree; e) a quad-tree; f) a shuffle-exchange network

applications of these arrays have been well discussed. The tree structures are depicted in Fig.1.1d-e. In a tree, the number of processors available increases exponentially at each level. If the problem to be solved has this growth pattern, then the tree geometry will be suitable for the problem. The binary tree system has an interesting aspect, that is, any particular processor in a tree of n processors can be accessed in at most $\log_2 n$ time. This is favorable when comparing with the O(n) access time for a 1-D array or the $O(N^{\frac{1}{2}})$ access time for a rectangular array. The shuffle-exchange network shown in Fig.1.1f is also mesh-connected. It should be mentioned that the particular communication structure of this network makes the system suitable for bitonic sort and n-point Fast Fourier Transform (FFT) [1.12]. However, the shuffle-exchange network, although it has great power in permutation, suffers from a very low degree of regularity and modularity. This can be a serious drawback for VLSI implementation. Consequently, mesh-connected arrays and trees are favorable architectures for special purpose VLSI design.

Many specially designed VLSI arrays and trees are proposed for pattern recognition and image processing tasks. Recently, a few VLSI processors were proposed especially for image processing.

1.2 VLSI Algorithms

Since the advent of VLSI technology, it is possible to put thousands of gates on one chip. This reduces the cost for processors and increases the communication speed. It also changes the criteria for algorithm design [1.13,14]. A good VLSI algorithm has to meet the following requirements: 1) the function of each processor must be kept simple and perform constant-time operation, 2) the communication geometry should be simple and regular, and 3) the data movement should be kept simple, regular and uniform. As mentioned in Sect. 1.1, the mesh-connected arrays and trees are favorable architectures for special purpose VLSI design. Besides the tree and the 1-D array, all other arrays have the mixed blessing of pipelining and parallelism. In order to take full advantage of this computational capability, VLSI algorithms are usually proposed with specific configuration in mind.

In their book *Mead* and *Conway* [Ref.1.1, Sect.8.3] explicitly introduce the VLSI algorithms and their associated processor arrays. For instance, the matrix-vector multiplication on linear arrays; the matrix multiplication, and LU-decomposition on hexagonal arrays; the color-cost problem on tree-structure systems, etc. *Kung* [1.13] provided a table which outlines the wide applications of VLSI algorithms. Many examples were given in his paper like an odd-even transposition sort on linear arrays; search algorithms on a tree machine (also see [1.15]).

Besides the applications mentioned above, VLSI algorithms have seen various applications in pattern recognition and image processing. For example, the pattern matching problem on a 2-D array and multi-dimensional convolution on a two-level linear array; FIR (finite impulse response) filtering and DFT (discrete Fourier transform) [1.16] on a linear array; recognition of finite-state languages on an 1-D array; the running-order statistics problems (a generalization of median smoothing) on a linear array; dynamic programming for optimal parenthesization and CYK (Cocke-Younger-Kasami) parsing on a 2-D triangular array; the convolution of two finite sequences on a tree system, etc.

1.3 Summary of Book

Many pattern-recognition and image-processing algorithms have been regarded computationally expensive. Consequently their utility in real-time applications is often restricted. With recent advances in VLSI technology, design and implementation of VLSI systems for pattern recognition and image processing have received increasing attention. This book is intended to document the recent

major progress in VLSI system design for pattern recognition and image processing.

The contents of the book can be roughly divided into three parts. The first part deals with general VLSI design considerations. H.T. Kung presents some experiences in the implementing of highly parallel processors using VLSI technology. T.Y. Young and P.S. Liu discuss the I/O bandwidth considerations in VLSI arrays for pattern recognition and image processing.

The second part contains three chapters that are devoted to the VLSI system design for pattern recognition. H.H. Liu and K.S. Fu describe the design of VLSI arrays for minimum vector-distance and string-distance classifications. L.M. Ni and A.K. Jain present a two-level pipelined systolic array for pattern cluster analysis. VLSI arrays for syntactic pattern recognition algorithms are treated by Y.T. Chiang and K.S. Fu.

The third part consists of six chapters that are concerned with the use of VLSI systems for image processing. Concurrent systems for image analysis are discussed by G.R. Nudd. S.Y. Kung presents the results of using VLSI wave-front arrays for image processing. C.R. Dyer and M.J. Clarke propose four VLSI designs for line and curve detection in images. A VLSI implementation of cellular logic processors is described by K. Preston. Dynamic scene analysis using a VLSI-based multicomputer architecture is treated by D.P. Agrawal and G.C. Pathak. Z. Stroll and S.C. Kang propose a VLSI system of image resampling for electronic publishing.

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