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System-on-Chip: Next Generation Electronics

Edited by Bashir M. Al-Hashimi

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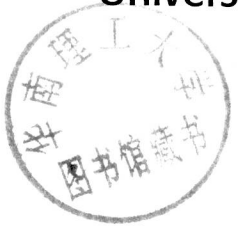

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To May, Sara, Haneen and Zahara

Preface

System-on-chip (SoC) is widely believed to represent the next major market for microelectronics, and there is considerable interest world-wide in developing effective methods and tools to support the SoC paradigm. The work presented in this book grew out of a special issue 'Embedded Microelectronic Systems: Status and Trends', IEE Proceedings: Computers and Digital Techniques, April/June 2005.

Recently, a number of excellent books on SoC have been published, most of which have focused on a particular area of SoC research. The field of SoC is broad and expanding, and the prime objective of this book is to provide a timely and coherent account of the recent advances in some of the SoC key research areas in one volume. In order to achieve this, 25 international research groups were invited to contribute to the book. Each contribution has an up-to-date research survey highlighting the key achievements and future trends. To facilitate the understanding of the numerous research topics covered in the book, each chapter has some background covering the basic principles, and an extensive up-to-date list of references. To enhance the book's readability, the 25 chapters have been grouped into eight parts, each part examining a particular theme of SoC research in depth.

In general, complete SoC designs consist of hardware and software components, which are traditionally developed separately and combined at a later stage of the design. This, however, increases time-to-market and system cost which is in contraction with some of the SoC drivers. To address such difficulties and to cope with the continuing increased design complexity, new design methodologies that support SoCs are needed. Part I of the book contains six chapters (1 to 6) dealing with the systematic and concurrent design, analysis and optimisation of SoC-based embedded systems. Software plays a very important role in the design of SoC; Part II has three chapters devoted to embedded software characterisation (Chapter 7), retargetable compilation (Chapter 8) and power-aware software generation (Chapter 9).

Excessive power dissipation in SoC does not only limit their applications in portable devices, but also results in increased packaging and cooling costs. Managing the power issue is fundamental to successfully expending Moore's law. Until recently, dynamic power has been the dominant source of power consumption, however, leakage power is becoming a significant fraction of the total power in deep-submicron designs. Part III contains four chapters (9 to 13) describing effective techniques

for reducing the dynamic and leakage power consumption. These techniques can be applied at various levels of the design hierarchy to allow designers to meet the challenging power constraints in SoC. There are some compelling advantages of employing reconfigurable devices in SoC in terms of speed, power, cost and time-to-market. Architectures and design methods for reconfigurable computing are discussed in Part IV of the book (Chapter 14).

Telecomm and multimedia applications require mixed-signal SoCs; Chapter 15 of Part V describes methods and tools that automate the process of modelling and generating analogue/RF cores for such SoCs. The International Technology Roadmap on Semiconductors (ITRS – http://public.itrs.net/) predicts that the use of clock-less designs will be increased in future SoCs to cope with timing issues. Chapter 16 of Part five is concerned with the synthesis and design automation of asynchronous systems. A key element in achieving functional design is the on-chip communication that interconnects the SoC cores. Bus-based interconnections provide the current SoC communication. However, SoCs complexity is increasing with the continuing scaling down of CMOS feature sizes. According to ITRS'03, an average SoC will contain >50 processing and memory blocks in 2008 and 100 such blocks in 2012. Consequently, it may not be viable to continue to effectively employ bus-based communication in future SoC. To address this concern, and improve performance of future SoCs, different interconnection technologies are being developed. Part VI (Chapters 17 and 18) is devoted to network-on-chip, a new interconnection technology where SoC cores communicate with each other by sending packets over an on-chip network.

Part VII of the book contains three chapters investigating functional design validation and verification, which are important factors that contribute to the ultimate costs of an SoC. Chapters 19 and 20 focus on simulation-based techniques that have been developed to validate complex hardware/software systems, whilst Chapter 21 considers formal verification as a way of verifying system correctness. The high level of integration is making the cost of testing SoC expensive, mainly due to the volume of test data and limited test access to embedded cores. The ITRS'03 predicts that if the current trends are maintained, by 2015 the cost of testing a transistor will approach or even exceed the cost of manufacturing. Therefore, low-cost design-for-test techniques for SoCs are required, which is the subject of the final part (Part VIII) of the book. This part has four chapters, test-resource partitioning (Chapter 22), multi-site testing (Chapter 23), on-chip timing measurement (Chapter 24) and yield and reliability (Chapter 25).

Book audience

It is the intention of this book to contain a diverse coverage of SoC main research themes, each theme is discussed in depth and therefore the book will appeal to broader readership. SoC is a popular PhD research topic and is appearing as part of the syllabus for both undergraduate and postgraduate Electronics and Computer Engineering courses at many universities, and I hope that this book will complement the research and teaching that is taking place in this area. Also, the book should serve as

a valuable reference for designers and managers interested in various aspects of SoC design and test.

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First and foremost I am indebted to all the contributing authors of this book. I acknowledge the financial support from the Engineering & Physical Sciences Research Council (EPSRC), UK, to my research activities in SoC which made this book possible. I like to thank all the researchers whom I have worked with and who have broadened my knowledge of the SoC field in particular, Dr. M. Schmitz, Dr. P. Rosinger, Dr. T. Gonciari and Dr. D. Wu. Finally, I wish to thank Sarah Kramer (Senior Commissioning Editor) and Phil Sergeant at the IEE, their assistance during this project have been invaluable and Geoff Merrett for his work on the book cover.

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