Integrated circuits

Technology and applications

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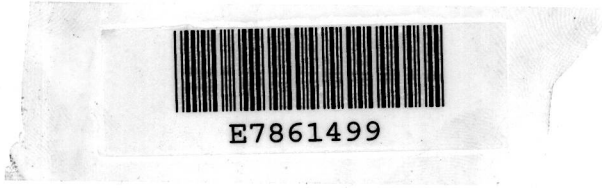

CAMBRIDGE UNIVERSITY PRESS

Cambridge
London · New York · Melbourne

Published by the Syndics of the Cambridge University Press
The Pitt Building, Trumpington Street, Cambridge CB2 1RP
Bentley House, 200 Euston Road, London NW1 2DB
32 East 57th Street, New York, NY 10022, USA
296 Beaconsfield Parade, Middle Park, Melbourne 3206, Australia

First published 1978

Phototypeset by Western Printing Services Ltd, Bristol
and printed in Great Britain by The Pitman Press, Bath

Library of Congress Cataloguing in Publication Data
Mazda, F. F.
Integrated circuits
Bibliography: p. 201
Includes index
1. Integrated circuits. I. Title
TK7874.M35 621.381'73 77-71418
ISBN 0 521 21658 3

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Preface

Perhaps no other field of engineering has progressed so far and so fast as that of integrated circuits. Undoubtedly these developments have been of considerable benefit to mankind. However this rapid progress poses a problem to the would-be author of a book on integrated circuits. He must aim to cover as much of the field as possible in a text which is small enough to be saleable. At the same time he must ensure that further developments have not outdated much of his work before the book goes to print.

The present book aims to overcome both these difficulties by concentrating primarily on the newer technology areas. Well-known and established techniques are only briefly mentioned and the student is directed to the bibliography for further material. Comparatively new devices, however, such as memories and microprocessors are described in greater detail. Not only are these emerging technologies, whose use is likely to increase during the life of this book, but there are few books which cover these topics.

The emphasis throughout the book is on the applications of integrated circuits. However it is important that the user has some understanding of the processes which are involved in fabricating the devices, in order that he may select and utilize them correctly. Therefore the first chapter of the book provides an introduction to the manufacturing techniques used in integrated circuits, and describes the differences between the various types of commercial processes. Packaging technologies are also described since it is an area of vital interest to the user, as often the packaged device is all that he sees.

The next five chapters of the book describe digital applications of integrated circuits. Chapter 2 covers the different circuit techniques which are used to produce families of devices, each family having its own distinct characteristics. Developments in this area have meant that many of the once well-known families are now becoming obsolete and are available commercially only as maintainence types for existing designs. These families are briefly described in the chapter, the emphasis being on new devices.

Chapter 3 introduces mathematical techniques which are used in the design of digital circuits. The binary and octal number systems are described first, followed by sections on Boolean algebra and function minimization techniques. Also described are analytical methods for sequential circuits and a brief introduction to threshold logic circuits. The material covered in chapter 3 is used in subsequent chapters to explain the operation of various integrated circuits.

Integrated circuits are now largely bought as off-the-shelf, 'black-box', devices which have been designed to produce certain output signals for sets of input signals. These devices are available to perform a variety of functions and a selection of these are described in chapter 4. They can all be stated to have low to medium complexity, in terms of number of circuit elements on a die, and are therefore known as small and medium scale integrated components. Complex or large scale integrated devices are described in chapters 5 and 6. Chapter 5 covers the different types of semiconductor memories which are commercially available. The construction of a single cell is first described and this is then followed by a discussion of the different organizations which may be used for an array of static and dynamic memory cells. Applications covered include read only memories, random access memories, and content addressable memories.

Chapter 6 describes devices which may be

considered to be universal logic elements. These are primarily large scale integrated components which can be adapted, with very few modifications, to meet a variety of different applications. Such devices cover uncommitted logic arrays, programmable logic arrays and microprocessors. The chapter describes the construction and applications of all these devices, with the emphasis being placed on microprocessors. Since software forms an important part of a microprocessor system the operation of the device is explained with reference to a list of software commands.

Linear integrated circuits are described in chapter 7. The number of different component types available in this area is very large and ranges from the well-known operational amplifier, to the less well-known charge coupled device. Once again the chapter introduces all the devices, so as to give the reader a feel for the whole field, but the emphasis is placed on new technologies.

This book is primarily intended for practicing engineers and technicians in electronics and other allied disciplines, who need an introduction to modern integrated circuit usage. It also covers the needs of some introductory post-graduate and specialist undergraduate courses.

Many people contributed to the contents of this book, either directly by giving advice, or indirectly through their own publications. I am grateful to them all, and to the countless other engineers and technicians who have been too busy pushing forward the frontiers of our knowledge to have time to write. My special thanks also go to Dr H. Ahmed of the University of Cambridge for reading through the entire draft of this book and for making invaluable suggestions for changes and corrections.

F.F.M.

1978

Contents

1. The technology of integrated circuits

1.1. Introduction

Integrated circuits can be made with one of two technologies, *monolithic** or *hybrid*. In the monolithic circuit all the component parts are formed into a single silicon *die*. The hybrid circuit resembles a miniature printed circuit board. Conductor tracks are built onto a small glass or alumina *substrate* and miniature resistor, capacitor, or semiconductor *chips* can be added. Generally the resistors are not included as discrete devices but are formed as tracks on the substrate surface, the resistance value being determined by the dimensions of the track and the resistivity of the material.

In addition to their production technology, integrated circuits can also be classified according to their application. These are broadly divided into linear and digital circuits. In this chapter the production technology of integrated circuits is briefly introduced. Subsequent chapters develop its applications.

1.2 Monolithic integrated circuits

Monolithic integrated circuits can be *bipolar* or *unipolar*. The difference between these two is best explained by comparing the action of their transistors, as shown in Fig. 1.1. With the *bias* arrangement shown, the holes in the base region are attracted into the emitter region and electrons flow from the emitter to the base. Provided the base region is thin, most of the electrons cross over into the collector and reach the collector terminal. However, some of the electrons combine with holes in the base region, and this is compensated for by a flow of holes from the battery terminal.

* The first occurrence of words that are included in the glossary of terms (p. 203) are given in italic.

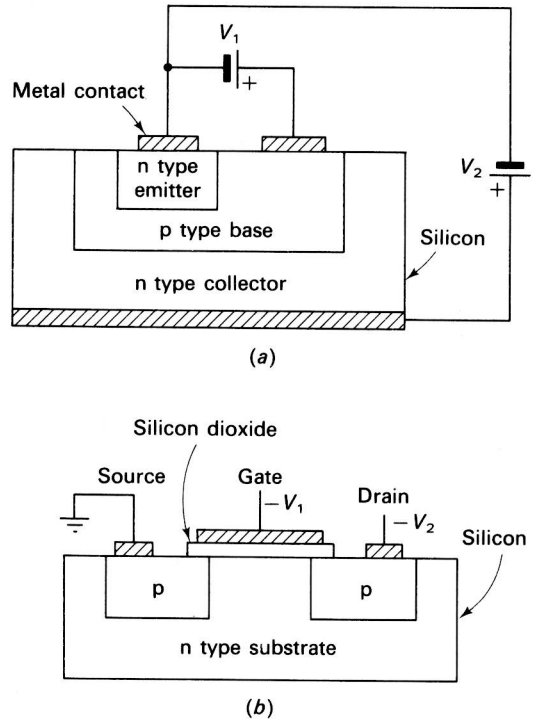


Fig. 1.1. Transistor action; (*a*) bipolar, (*b*) unipolar.

The bipolar transistor action involves both holes and electrons. By contrast the unipolar transistor operates due to a flow of holes or electrons, but not both in the same device. Fig. 1.1(*b*) shows a p-channel unipolar transistor. With no gate bias, current cannot flow between source and drain. If the gate is taken to a high enough negative voltage it will attract holes to the surface between the source and drain so that a conducting channel exists between the two. Similarly if the substrate is of p type material

and the source and drain are of n type then a positive gate bias attracts electrons and forms the conducting channel.

Several *process* steps are used in the production of monolithic integrated circuits. The *wafer* is first prepared by pulling a seed crystal from the silicon melt in a Czochralski puller. p or n type impurities may be added to the melt. The ingot is then cut into slices with a diamond impregnated saw and polished with diamond powder to give a strain free, highly flat surface.

During the processing of an integrated circuit a layer of silicon oxide is often required to be grown over the silicon surface. This can be grown by heating the silicon wafer in a quartz tube and passing wet or dry oxygen, or steam, over it. Selective areas of the silicon dioxide can be removed using photolithography. In this process the whole surface is covered with a photoresist and exposed to ultraviolet light through a mask. If the material used was negative photoresist then the exposed areas harden and the non-exposed areas can be removed by a developer. The surface is now etched with hydrofluoric acid to remove the exposed silicon dioxide layer. *Impurities* can be introduced into the exposed regions by *diffusion*. The wafer is heated and nitrogen gas, which has previously been bubbled through a container of the impurity, is passed over it. At the high temperatures involved, in the region of 1200°C, the silicon atoms are very mobile so that the impurities from the gas rapidly move through the silicon crystal structure. No diffusion can occur in regions protected by a silicon dioxide layer since these absorb the impurities.

An alternative technique for introducing impurities into selected regions of the silicon surface is known as *ion implantation*. In this the ions are accelerated until they attain a high energy and they are then bombarded onto the desired silicon region. The *dopants* force their way into the silicon structure and their concentration and penetration depth can be closely controlled.

The interconnection pattern on the silicon surface is obtained by depositing a layer of aluminium over the surface and then etching it. Vacuum deposition techniques are commonly used in which the silicon *slices* are placed face down on the top of an evacuated bell jar and the metal source is evaporated onto it. The slices are heated so that the metal forms a strong bond with the silicon surface.

The silicon substrate, prepared by means of pulling, usually has a relatively wide tolerance in its impurity doping. It is usual to form a layer, called an *epitaxy*, over the substrate. This is a single crystal silicon structure and is a molecular extension of the original silicon. The epitaxy is built up by heating the silicon slices in an atmosphere of hydrogen carrying silicon tetrachloride. When the vapour reaches the hot silicon surface it dissociates and silicon atoms are deposited on the slice, where they establish themselves as part of the original silicon crystal structure, Dopants can be introduced into the vapour stream and the concentration in the epitaxy layer can be closely controlled.

The masks used in the preparation of integrated circuits can be made by several techniques. The layout drawing for each mask can be cut into a stable Mylar film which is then photographically reduced down to $\times 10$ size and finally to the required die size in a step-and-repeat camera, which produces many identical patterns of the die, covering the entire surface area of the silicon slice. Alternatively the mask can be prepared by writing directly onto the film by a beam of light or by building up the pattern by altering the position and dimensions of a slit and then repeatedly exposing the film through this. For very fine line circuits an electron beam is used to write onto the film since it has a lower wavelength than conventional light.

Fig. 1.2 shows the structure of a typical integrated circuit. An n^+ diffusion, called the buried diffusion, is first formed into the substrate, before the epitaxy is grown over it. This is used to provide a low impedance path for the collector current. p diffusions are made through the epitaxy to link up with the original substrate such that the individual components are formed in the n type epitaxy and are completely surrounded by p type material. If the substrate is now taken to the most negative voltage in the system then the components are all electrically separated from each other by

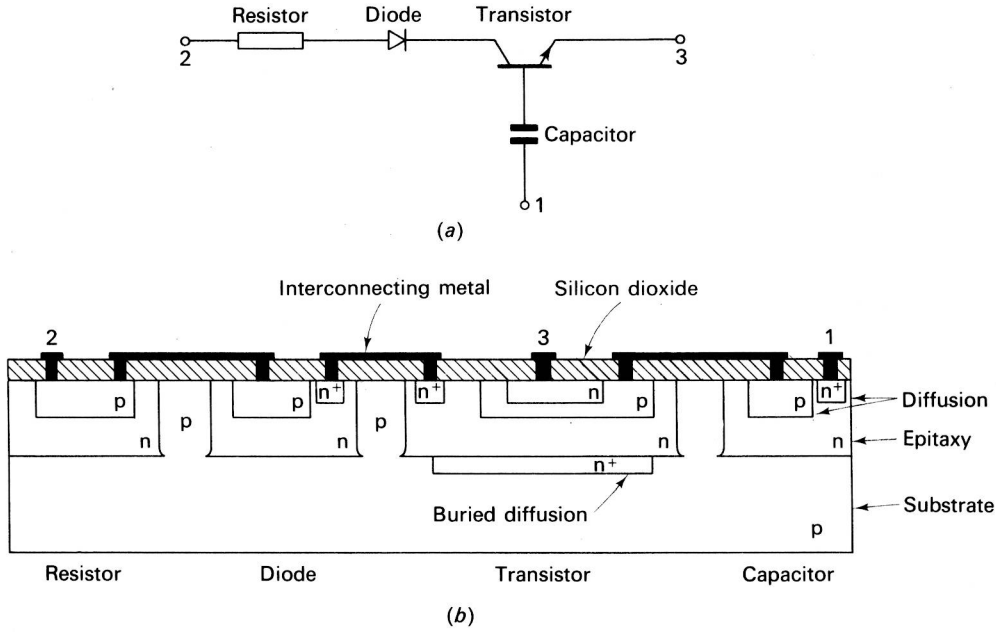


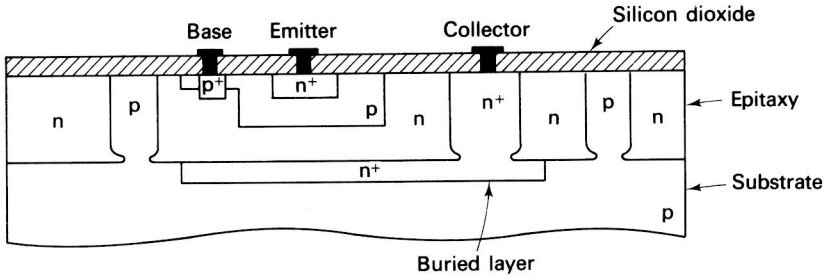
Fig. 1.2. An integrated circuit with diode isolation; (a) electronic circuit, (b) integrated circuit layout.

reverse biased pn junction. This is known as diode *isolation*.

The diodes used in integrated circuits can be formed using the base–emitter or collector–base junction of the transistors. The former is fast but has low breakdown voltage, whereas the latter has a higher voltage rating but is slower. Schottky diodes can also be used in which a metal conductor forms the p electrode and it is placed in contact with a lightly doped n type silicon material. Schottky diodes are very fast. In Fig. 1.2 a collector–base diode is shown and high impurity n^+ diffusions are used under all metal terminals to prevent unwanted Schottky action occurring. The value of the resistors is determined by their dimensions and the resistivity of the diffusion in which they are formed. Integrated circuit resistors are difficult to make to close absolute tolerances although between adjacent resistors on the same die the matching is good. Capacitors can only be built to low values. Fig. 1.2 shows a diffusion capacitor which uses a reverse biased pn junction. Better quality capacitors, having lower leakage, higher Q and a lower voltage coefficient, can be obtained with metal–oxide-semiconductor (MOS) capacitors. In these a thin layer of silicon dioxide acts as the dielectric and is sandwiched between a top metal conductor and a conducting bottom diffusion into the silicon, as illustrated in Fig. 1.4.

Fig. 1.3 illustrates several other techniques which have been used to isolate devices on a silicon chip. Process III is a very fast technology. It uses a very thin epitaxy and shallow diffusions to give narrow transistor bases and low *parasitic capacitance*. The CDI process uses a p dope epitaxy and a non-masked p diffusion over the whole surface. The collector diffusion is taken down to the buried layer and surrounds the whole element, so giving the isolation. The advantage of the system is that no separate isolation diffusion is required so that a larger number of devices can be accommodated on a die.

Silicon dioxide can be used to provide the isolation on the die. The silicon surface is etched to the required depth and oxide is then grown over it. The Isoplanar process gives a high die density since devices can be placed



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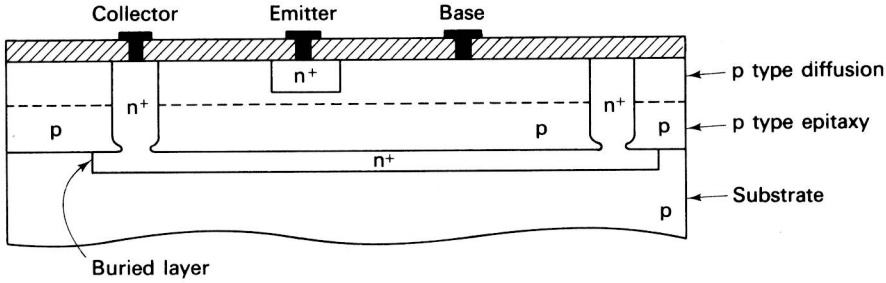

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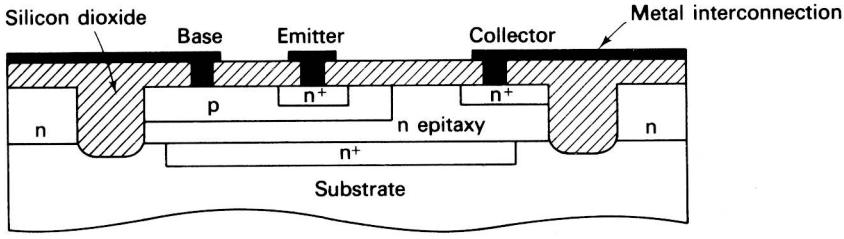

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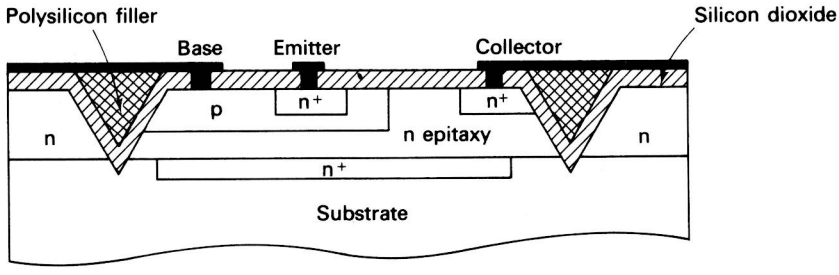

(*d*)

Fig. 1.3. Bipolar isolation techniques; (*a*) process III, (*b*) collector diffusion isolation (CDI), (*c*) isoplanar, (*d*) VIP and Polyplanar.

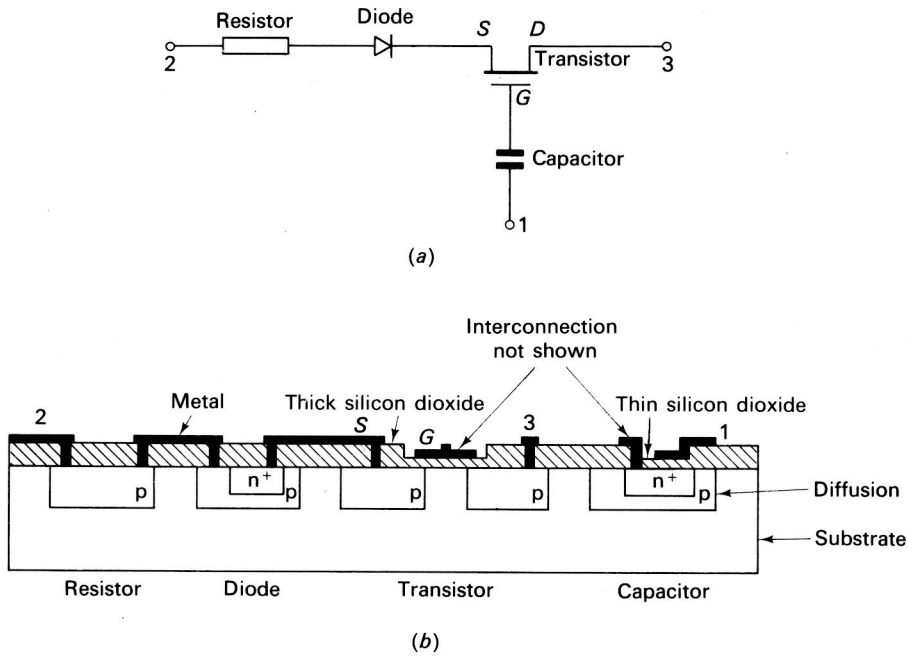

Fig. 1.4. Unipolar integrated circuit; (a) functional diagram, (b) chip construction.

close together. Speeds are also higher since parasitic capacitances, associated with isolation diffusions, are absent. Alternative oxide isolation techniques use V grooves between circuit elements which are then oxidized. Unfortunately the metallization which runs over these grooves is likely to crack due to the sharp bends involved. The V isolation with polysilicon backfill (VIP) process and the Polyplanar process overcome this disadvantage by filling the V groove with polycrystalline silicon before the metallization stage in order to avoid sharp bends in the metal.

Fig. 1.4 shows the structure of an integrated circuit constructed in unipolar technology. The p wells are self-isolating provided the n substrate is taken to the most positive voltage in the system, therefore unipolar circuits are constructionally simpler than bipolar and are capable of greater die densities.

The disadvantages of the unipolar circuit shown in Fig. 1.4 are that it requires a relatively large voltage to turn on the transistors and it is fairly slow due to parasitic capacitances primarily caused by the overlap of the gate electrode over the source and drain diffusions. Fig. 1.5 shows several modifications which have been made to overcome these disadvantages. The metal–nitride–oxide-semiconductor structure (MNOS) uses a nitride layer under the gate, which gives lower threshold voltages. Similarly the threshold can be reduced by using a polycrystalline silicon gate instead of a metal gate. A further advantage of this process is that since the silicon gate can withstand the high temperatures used during the diffusion stage it can be used as a mask during the source and drain diffusion so that the overlap between the gate and these regions is reduced, giving higher operating speeds. The metal gate can be used as a mask during ion implantation, which is a cold process. This again results in a structure which has very little gate overlap and is therefore fast.

Isoplanar techniques can be used in unipolar technology as was done for bipolar.As before, the advantage is reduced stray capacitance and higher speeds. The n channel unipolar device (NMOS) is inherently faster than a p channel

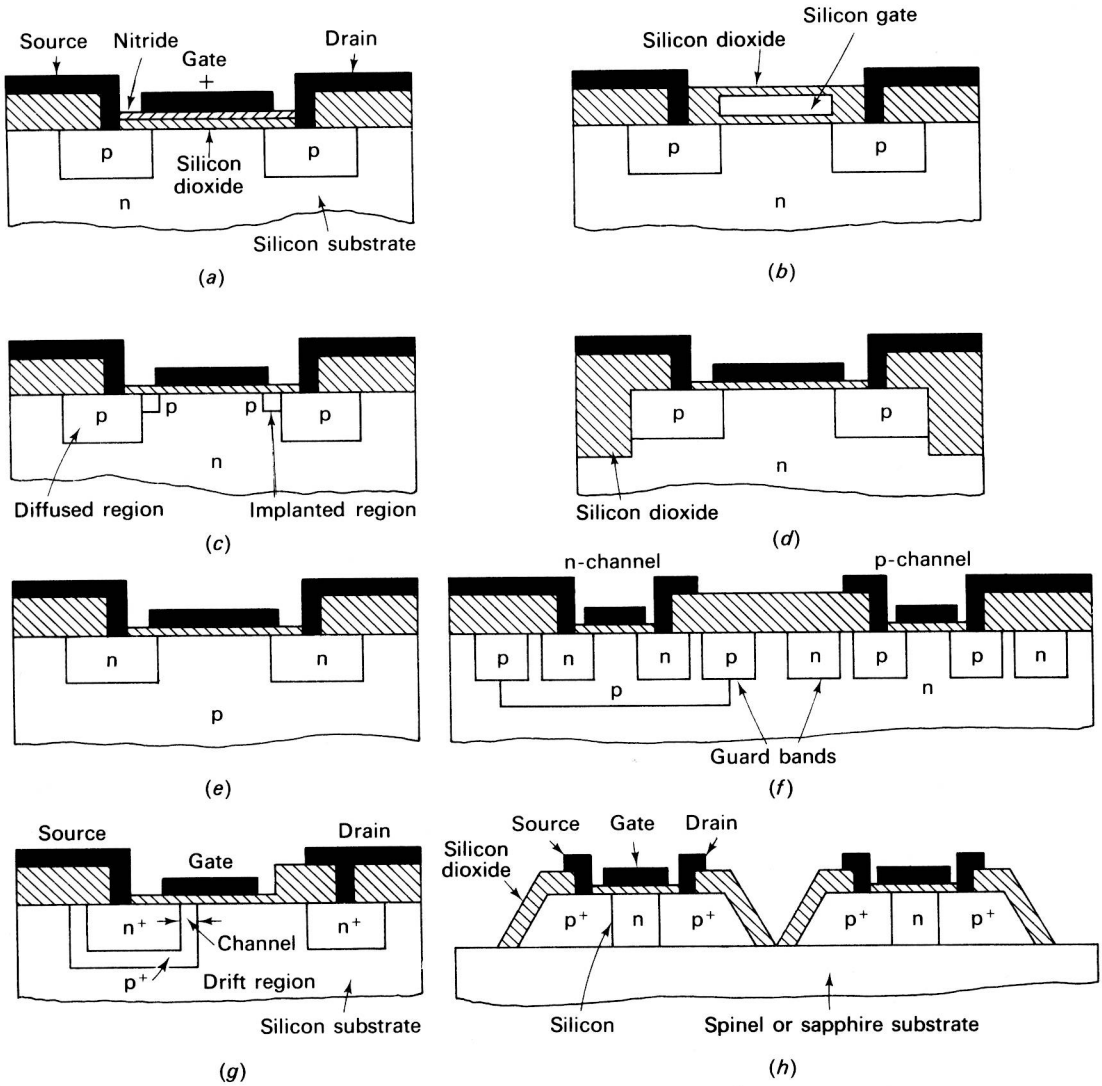

Fig. 1.5. Unipolar processes; (*a*) MNOS, (*b*) silicon gate, (*c*) ion implant, (*d*) isoplanar, (*e*) NMOS, (*f*) CMOS, (*g*) DMOS, (*h*) SOI.

device (PMOS) since the electrons carry the charge in NMOS and these have higher mobility than the holes which operate in PMOS transistors. Both p- and n-channel transistors can be combined to form complementary MOS devices or CMOS. These occupy a large area on the die, specially if guard bands are used to surround groups of like devices in order to prevent leakage between them. The advantages of CMOS are a low threshold voltage and low power consumption.

For very high speeds double diffused MOS or DMOS can be used. The gate channel is formed as the difference between the p and n diffusions and it can be made very narrow, which gives this device its high speed. Silicon on insulator (SOI) is another device which has been developed for high speed applications. The

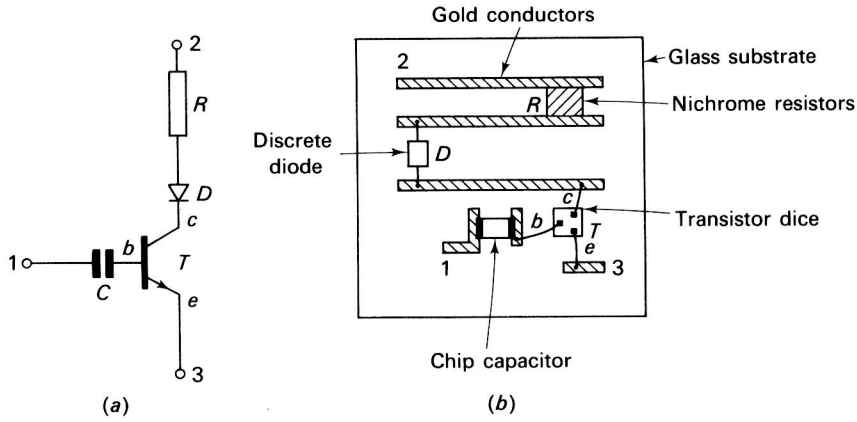

Fig. 1.6. Hybrid thin film circuit; (a) circuit schematic, (b) thin film circuit.

silicon is grown on the insulator, which must have a crystal structure similar to silicon. Sapphire and spinel are suitable materials for this. The silicon is then etched into islands and the unipolar devices are formed into these. The stray capacitance between devices is very low in this technique so that it is capable of high speeds.

1.3 Hybrid integrated circuits

Hybrid integrated circuits can be one of two types, thin film and thick film. Although these circuits look very similar they differ in their production techniques which give the thin film better performance characteristics but makes it more expensive than thick film. Fig. 1.6 shows the construction of a typical thin film circuit. The diode has been shown added in discrete form although unpackaged devices may be used as is done for the transistor. The capacitor is in the form of a miniature block and the conductors and resistor are thin film tracks on the glass substrate. A thick film circuit would look very similar to Fig. 1.6 but would use different substrate, conductor and resistor materials.

Glass is the most frequently used substrate material for thin film hybrid circuits. It must be flat and free from deformation, in order to prevent cracks in the top film, and it must also be chemically stable so as not to effect the film characteristics. Gold is the commonest conductor material since it has a very low resistance, but it does not adhere well to glass. It is usual to cushion the gold with a layer of Nichrome, which is an alloy of about 80 per cent nickel and 20 per cent chromium. Aluminium is also used as conductor material. Although it is cheaper than gold it has a higher resistance and reacts chemically with the gold wires which are sometimes used to connect semiconductor chips to the tracks. Nichrome is the most popular resistor material. It has excellent adhesion to glass and gives resistors with a low temperature coefficient. For high valued resistors materials consisting of a compound of a dielectric and a metal, known as cermets, are used. Capacitors can be added in chip form or built onto the substrate as layers of conductor and dielectric materials. Both tantalum oxide and aluminium oxide are used, and they are formed by first putting down a layer of the metal, oxidizing it to give the dielectric, and then adding the top conductor layer.

The film can be deposited on the thin film substrate by several techniques. Evaporation is the most direct and consists of placing the source material and the substrate in a partial vacuum. The source is heated to vaporize it and this material then settles on the substrate. Source heating can occur by resistance elements or by bombarding it with a beam of high energy electrons. The disadvantage of the evaporation system is that it gives a film which has low adhesion to the substrate and a low density. An alternative technique, known as

sputtering, overcomes these disadvantages but is slower in forming a film of a given thickness. In sputtering a glow discharge is formed in argon at between 0.01 to 1.0 torr, by a high voltage applied between the source to be sputtered (cathode) and the substrate (anode). Argon ions are formed and these strike the source releasing molecules which are negatively charged. These molecules bombard the substrate, giving a film which has good adhesion and density. The track pattern can be formed on the substrate by either covering the whole surface with the track material and then using photolithography to etch out the areas not required, or by placing a mask in contact with the substrate, prior to film deposition, with cut outs in the regions where the film is to be placed on the substrate.

The materials used for thick film production are called *inks* or *pastes*. Many different ink compositions are available, depending on the supplier and whether conductor, resistor or dielectric material is required. Basically all inks are made from fine metal and glass powders which are mixed with an organic solvent. The substrate must be pure and flat with a high mechanical strength. It should have good electrical resistance and low thermal resistance. The thick film process involves very high temperatures, above 1000°C, and the substrate must remain chemically stable throughout. A good general purpose substrate material is a compound of 96 per cent alumina and 4 per cent glass, although 99.5 per cent alumina substrates are also used. Beryllia is preferred for power circuits since it has good thermal conductivity.

Thick film tracks are formed by printing the inks through a nylon or stainless steel mesh. The areas where the ink is not required are blocked off by emulsion. Fig. 1.7 illustrates the print operation. After the ink has been printed onto the substrate it is allowed to stand for a few minutes for the ink to coalesce. It is then dried in an oven or under infrared heaters to remove the volatile components of the paste. Following the drying process the circuit is fired in a zoned oven. This first removes the remaining volatile elements from the ink and carbonizes and oxidizes the organic binders. Then the glass content

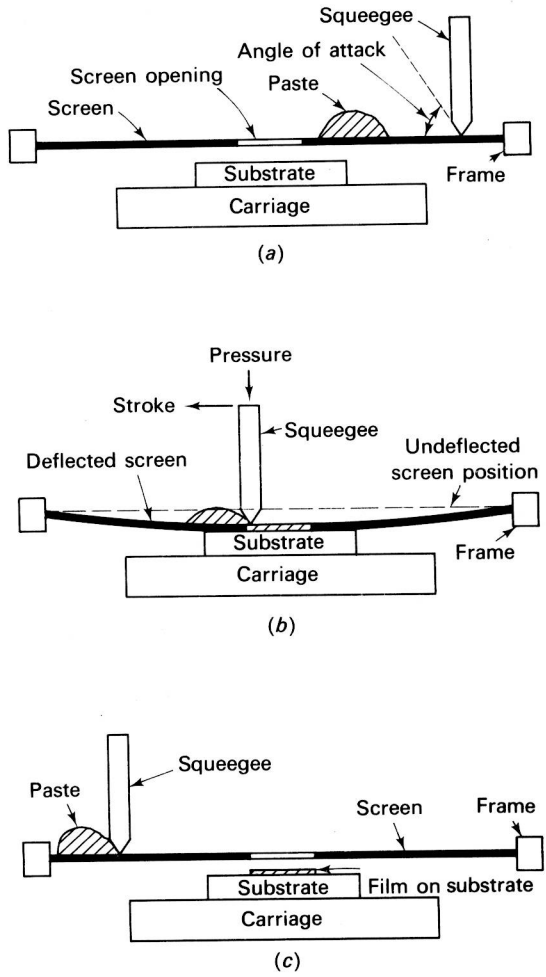

Fig. 1.7. Stages in thick film printing; (a) start of stroke, (b) during stroke, (c) end of stroke.

of the paste is melted, and this forms a seal around the metallic particles as well as fixing the track to the substrate.

Printed resistors have an accuracy between batches of less than 30 per cent. For tighter tolerance, trimming must be used which removes a portion of the track area and so adjusts the resistance value upwards. Two techniques exist for trimming. The first is *air abrasive trimming* and uses a high velocity stream of fine abrasive powder to wear away the film. It does not result in any appreciable temperature rise or shock or vibration, but it does

give an 'overspray' action onto adjoining components. The trimming operation also removes the vitreous parts of the resistor paste and exposes the resistors to subsequent contamination. In laser trimming a high energy laser beam is directed onto the film, raising its temperature and vapourizing the required area. It uses more expensive equipment than air abrasive trimming and the laser needs to be re-tuned each time a different colour resistor is trimmed. However, there is no overspray and the high temperature results in a flow of the vitreous contents of the film so that the cuts are resealed.

1.4 Integrated circuit bonding

There are many techniques in use for connecting a semiconductor die onto a hybrid substrate or into its package. First the die must be connected to the substrate and then conducting bonds must be made to its terminals. Eutectic bonding is commonly used for connecting the chip to the substrate. It relies on the fact that an eutectic alloy such as gold–silicon has a lower melting point than both gold and silicon. The area to which the die is to be attached is gold plated and the chip is then pressed and scrubbed onto it to form the eutectic bond. Alternative techniques for die *bonding* include using silicon or epoxy adhesives, and soldering, which requires both the back of the die and the area on the substrate to be gold plated.

The terminals on the die can be wire bonded to the package pins, or hybrid tracks, using thermocompression or ultrasonic techniques. Thermocompression ball bonding uses gold wires and it relies on heat and pressure to form the bonds. Ultrasonic bonding does not require the substrate to be heated and it uses aluminium wire. The wire is pressed and scrubbed at high frequency against the metal contact area and this removes surface oxides and results in a strong molecular bond. Instead of using wires for bonding, flip chip or beam lead techniques can be used. In flip chip bonding contact bumps are formed on the die or the tracks, and the die is 'flipped' or inverted and then connected to the bumps by soldering, ultrasonic, or thermocompression bonding. In beam lead bonding metal leads or 'beams' overhang the semiconductor die and these are attached to the substrate contact areas. In both flip chip and beam lead techniques no separate die bonding is required since the electrical contact and mechanical support are both provided by the beams and balls.

Film carrier bonding is a relatively new system which is intended to greatly reduce the labour costs involved in wire bonding small chips. In general a trained operator should be capable of making a conventional wire bond in a second. Add to this the time involved in mounting and positioning a die under a microscope, and the average time for a 14 lead package (28 bonds in all) is about a minute. This can be expensive when compared to the cost of a small die mounted in a cheap plastic package. Semi-automatic wire bonders are currently available, but these generally do not perform much better.

The film carrier technique uses a continuous film of polyimide which has copper lead frames mounted on its surface. The whole system resembles a film spool. A window in the film allows the inner leads of the frame to protrude. It is to these fingers that the silicon die is bonded. After bonding the lead frame and die are wound onto a second spool for storage until required. The lead frames are then removed from the film and connected into the required circuit or package by thermocompression, ultrasonic, or solder bonding.

1.5 Integrated circuit packaging

The previous section has described some of the methods used for bonding semiconductor chips to substrates or to metal lead frames. The packages for these frames can be made from *hermetic* or non-hermetic (plastic) material. In addition the packages can have a variety of different configurations, such as TO-5, dual-in-line and flat pack.

The basic principle involved in a plastic package is to assemble the circuit on a substrate or metal lead frame and then to mould the entire structure, apart from the leads, in plastic to form the body of the device. The most commonly used plastic materials are epoxy, phenolic and silicone resins of which epoxy is

the most popular. Several requirements are placed on the plastic material. It should adhere well to the lead frame so that it prevents moisture from creeping in along the package legs. The material must also have a thermal coefficient of expansion which is matched to the rest of the circuit in order to prevent stresses being set up in it which could damage the leads or the thin bonding wires. It is also important that the material does not contain or release any impurities which would contaminate the enclosed silicon.

Plastic packages are low cost, especially when compared to hermetically sealed devices. They are also ideally suited to volume production techniques. However their resistance to moisture and environmental contaminants is not as good as hermetically sealed packages and they can be damaged under thermal cycling conditions. Plastic packages also have lower heat dissipation compared to other types, especially metal packages. Heat dissipation properties can be considerably improved by wrapping the circuit in a metal surround before plastic encapsulation and in some cases bringing out part of this metal for bolting onto an external heatsink. Plastic packages are also usually characterized for operation over the industrial temperature range of 0°C to 70°C while hermetic devices can cover the full military range from −55°C to 125°C. However for normal industrial use plastic devices are very suitable, and with chips which have been passivated with a glass or silicon nitride layer these devices can be made to operate in fairly hostile environments.

A semiconductor chip is sensitive to the presence of contaminants such as sodium ions, hydrogen, oxygen and water vapour. These reduce the collector–base breakdown voltage of on-chip transistors, increase the leakage current and parasitic capacitance, reduce current gain, and attack the chip metallization and the wire bonds. Hermetic sealing aims to minimize these effects by first removing the contaminants from the package, usually by heating it to about 250°C, and then sealing it in the presence of an inert gas. During sealing the package temperature is kept to as low a value as is practical.

A hermetic package usually consists of a base, a body, leads and a cover. Obtaining a seal between metal surfaces is relatively easy and methods of glass to glass seals also present little problem since both surfaces can be fused at high temperatures, or cemented by means of an interconnecting lower melting point glass. The problem arises when glass to metal seals need to be made, such as when metal leads pass through a glass package. The difficulties generally arise due to the unequal heat conduction and thermal coefficient of expansion of the two materials, which make the seal unreliable under temperature cycling conditions. Two methods are generally used to produce glass to metal seals. In the first method a thin oxide layer is grown on the metal surface prior to coating with glass. The surface of this oxide is dissolved into the glass and results in a smooth transition from metal to oxide to glass. This results in a good seal since the oxide in effect acts as an intermediate buffer. The second sealing technique uses a solder glass seal. This is a special composition low melting point glass which is coated onto the two surfaces to be sealed. On heating the interconnecting glass melts and wets the two surfaces, forming a good seal on cooling.

Three types of materials are used for hermetic packages. These are metals, ceramics and glasses. Of the many metals the most popular is a nickel–iron–cobalt alloy called Kovar. It has a relatively low electrical and thermal conductivity and is compatible with standard sealing glass. Ceramics make excellent hermetic packages and are very commonly used. They have high thermal conduction and a thermal coefficient of expansion which is compatible with that of glass. Many different ceramic materials can be used, the most popular being alumina having a purity between 75 and 99.5 per cent. For high power dissipation beryllia is most common although other ceramics in production are stealite, forsterite, titanate and zircon. The thermal coefficient of all these materials is close to that of metal. Glass packages are cheap since they can give good inexpensive seals. They have poor conductivity and are generally not suitable for anything apart from very low power circuits. Hybrid packages using