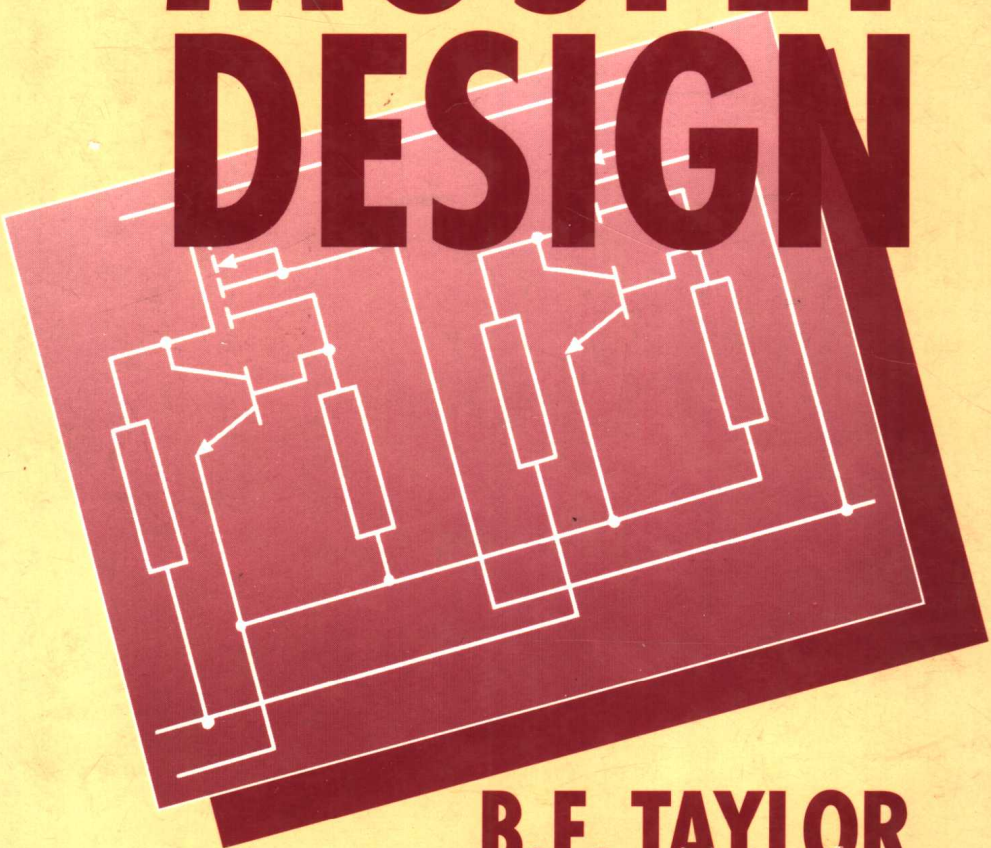
POWER MOSFET DESIGN



B.E. TAYLOR

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Introduction

Over the years several books have been published relating to subjects as diverse as the design of power converters, motor control, cycloconverters and others, all of which may be regarded as being interrelated. The books covering the subject of power converters are mainly concerned with the design of Switch Mode Power Supplies (SMPS). Of late, virtually no subject material has been provided relating to the linear power supply.

The vast majority of the books also cover the use of Bipolar Junction Transistors (BJTs) and this subject material has been backed-up by a large quantity of papers and application notes. However, the abundance of all of this literature relating to the BJT is, in many instances, irrelevant to today's technological requirements.

The introduction, over a decade ago, of the vertical geometry co-planer double-diffused power MOSFET (D-MOS) resulted in the first power semiconductor becoming available to seriously rival the dominant position of the high-voltage fast switching bipolar transistor. The virtual acceptance of the power MOSFET in today's market as a commodity item would have been expected to provide literature which would cater for a very wide spectrum of users and potential users.

Unfortunately, an insignificant number of papers and books are concerned with the actual design philosophy related to circuits which utilise power MOSFETs. When MOSFETs are addressed the range of cover is usually found to be severely restricted. It is not restricted in the sense that the depth of coverage is limited, but in that the material is either aimed specifically at undergraduate students and 'academics' or is so low key in its wording as to be relevant solely to secondary school students and hobbyists. Almost no literature is available which attempts to span the whole range of readership, and to include the practising engineer and technician. This book is an attempt to correct this omission.

The subjects covered are mainly concerned with the driving and protection of all power MOS-gated structures — from the conventional power MOSFET device to those with current-sensing capability and the ones with in-built conductivity modulation. A degree of familiarity with chronologically earlier power transistors (BJTs) will be beneficial to the reader, but not essential. A thorough understanding of the basics related to the subject of power electronics is necessary if a complete grasp of the material is to be achieved. This understanding should also encompass, if possible, the subject of magnetics as perceived today.

I make no apology for the inclusion of some of my favourite circuits. I am well aware that I am leaving myself open to the accusation of being egotistic. My firm belief is that the interest factor of these circuits will be found to stimulate the imagination of the reader. If this stimulation, in turn, fosters the desire towards further experimentation on the part of the reader, then inclusion of these circuits will have proven to have been worthwhile.

The inclusion of some circuits may well be questioned, since these circuits could well be demonstrated as being capable of functioning with BJTs or any other type of semiconductor power switch. It will become obvious that I have included these circuits because of their superior behaviour when they are found to be designed around the power MOS-gated transistor.

Acknowledgements

I am deeply indebted to all my friends and colleagues who have shared their knowledge, wisdom and free time in advising me on the best way to approach the writing of this book.

I would also like to thank all those who have attended the many seminars that I have had the privilege to present. It is to some of those attendees that I am particularly grateful since it was their continued suggestion for me to publish the tips which I gave at the seminars which has resulted in me putting pen to paper.

I am also deeply appreciative of the understanding and encouragement I have received from my family and most especially my wife, who was certainly not aware of the consequences to herself, from the encouragement she gave. It was her unstinting editing and re-typing that has made this publication possible.

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1

MOS-gated Transistors (MGTs): Their Structure and In-circuit Behaviour

It should be made clear to the reader that there is no intention to discuss the *static induction transistor* and the *static induction thyristor* in this book. The reason for omitting these devices is that they do not belong to the family of MOS-gated transistors and more importantly they have been found to be virtual laboratory specimens. The only non-MGT device which I shall, on occasion, refer to is the Bipolar Junction Transistor (BJT), because of certain similarities between the two parts.

There is one area where the MOSFET (and nearly all other MOS-gated transistors for that matter) is vastly inferior to the conventional BJT. The overwhelming superiority of the BJT lies in its circuit symbol.

The power MOSFET's overall structure should be well known by now, since it has been discussed at great length already; and therefore will not be discussed in any significant detail within this book.

It is sufficient to say that once the basic device has been fabricated then continuation of the fabrication of the control structure (the gate) is achieved by covering the exposed upper surface of the device with an insulating material (in this case it is usually silicon dioxide). The gate structure is now deposited upon this insulating medium and after suitable etching to a predetermined (mask) pattern it is covered by another layer of the same insulator material. The fabrication of the Insulated Gate Transistor (IGT) is achieved by a back diffusion into the drain structure of a MOSFET of a minority carrier injection layer. In the case of an N-channel device this injection layer will be a P-type semiconductor; and N-type for a P-channel structure. This last description is an over-simplification of the process for fabricating an IGT. This is especially true of the newer IGTs which have been recently introduced as second generation parts.

It can therefore be seen that, between the gate and the remainder of the MOSFET's structure, there exists a very high resistance. This intrinsically high resistance between gate and the rest of the structure results in the MOSFET having a very high input resistance (which is often erroneously termed as being

a high input impedance). This high input resistance gives the MOS-gated transistor a number of important differences to the BJT. One of these differences will be scrutinised, since this difference is significant enough to quantify the present day popularity of the power MOSFET; and will be of equal importance to the IGT.

The power MGT and the BJT are both characterised as being fundamentally charge controlled. The similarity both starts and ends at this point, in that the BJT's charge is inherently current derived whereas that of the MOSFET is fundamentally voltage derived.

It is now necessary to examine the profound nature of the two devices' charge control characteristics.

1.1 BJT CONTROL CHARGE (Q_{BJT})

Over a relatively short proportion of the total conduction time, of the BJT, the charge can be expressed as:

$$Q_{BJT} = I_b t_{on} \tag{1.1}$$

where I_b is the average value for the base current flowing for the period of time t_{on} (which may be defined as the total switch-on time of the BJT and is the sum of turn-on delay time and current rise time). This charge can be further enlarged to be:

$$Q_{BJT} = I_c / h_{FE} t_{on} \tag{1.2}$$

where I_c is the collector current (averaged over t_{on}), and h_{FE} is the static current transfer ratio of the BJT. If the duration of t_{on} is of the order of a few hundred nanoseconds or even as long as one microsecond, then the use of the static current transfer ratio is perfectly valid. It is also interesting to note that the base charge is proportional to collector current.

The energy (E_{Base}) expended in accumulating this charge can be expressed as:

$$E_{Base} = V_{be}(I_c / h_{FE}) t_{on} \tag{1.3}$$

where V_{be} is the average value of base emitter voltage of the transistor for t_{on}. V_{be} is found to be proportional to the product of the base spreading resistance and the emitter current. The implication therefore is that V_{be} is proportional to the collector current. It can be demonstrated that V_{be} has a logarithmic relationship with the collector current. This logarithmic tendency is of little relevance since for all practical purposes a power transistor will never be used at extremely small values of collector current where the logarithmic effect is most noticeable.

As an indication of the overall drive efficiency it is not sufficient merely to discuss the base control charge. It is equally necessary to discuss the power dissipated in the base and this can be expressed as follows:

$$P_{base} = (E_{base} \times \text{frequency}) + P_{Base}(t_{cond})$$

where t_{cond} is conduction time of the BJT and is that part of the total on-time which does not include the turn-on time.

If

$$t_{ON} = t_{on} + t_{cond}$$

then

$$P_{base} = V_{be}(I_c / h_{FE}) t_{ON} f \tag{1.4}$$

Returning to the subject of transistor control charge it becomes essential to discuss the control charge of the MGT.

1.2 MGT GATE CONTROL CHARGE (Q_{gate})

The MGT gate control charge can be expressed as:

$$Q_{gate} = C_{iss} V_{gs} \tag{1.5}$$

where C_{iss} is the input capacitance of the MGT and V_{gs} is the gate to source voltage of the device. The reader is reminded that C_{iss} is the sum of two capacitances — namely the sum of C_{GS} (the gate to source capacitance) which is a real capacitance; and C_{DG} (the drain to gate capacitance) which is a voltage dependent capacitance. This value of gate to source voltage is a function of the type of device (whether it is a standard or logic level MOSFET or IGT) and the voltage required to achieve full enhancement. It should be noted that the drain current is not mentioned.

Note that the gate charge is difficult to calculate owing to the voltage dependency of C_{DG} and is best measured.

Of greater significance is the energy (E_{Gate}) expended in accumulating this charge which can best be expressed as:

$$E_{Gate} = 0.5 C_{iss} V_{gs}^2 \tag{1.6}$$

Once again, for the purpose of indicating the overall drive efficiency, it is necessary to discuss the power required to drive the gate and this can be expressed as:

$$P_{Gate} = E_{Gate} \times \text{frequency} \tag{1.7}$$

After expansion equation (1.7) becomes:

$$P_{gate} = 0.5 C_{iss} V_{gs}^2 f \tag{1.8}$$

In the case of P_{gate} this power would be dissipated within the gate structure only if the gate structure resistance happened to be significantly higher than the drive circuit impedance. P_{base}, on the other hand, is always dissipated within the transistor structure of the BJT itself. It should be remembered that the magnitude of control power is not important in itself. The real importance of this power is the indication of the drive circuit's power delivery and handling capability.

Having derived equations (1.4) and (1.8), it would be beneficial if the effects can be demonstrated practically. Consider two well known examples of both types of semiconductor: the ubiquitous 2N3055 (BJT) and IRF140 (MOSFET). Both devices will be used in a simple circuit to switch a resistive load at 50% duty cycle and at a frequency of 1 kHz. For simplicity the load current for both devices can be set at 10 A.

For the 2N3055:

$$V_{be} = 1.5 \text{ V}, \quad h_{FE} \text{ (@ } I_c = 10 \text{ A)} = 5$$

Using equation (1.4) we have

$$P_{base} = [\{0.75 \times (1 \times 1E^{-6})\} + \{1.5 \times (10/5) \times 499E^{-6}\}] \times 1000$$
$$= \mathbf{1.49\,775\ W}$$

For the IRF140:

$$V_{gs} = 10 \text{ V}, \quad C_{iss} = 1600 \text{ pF}$$

Using equation (1.8) we have

$$P_{Gate} = \tfrac{1}{2} \times 1600E^{-12} \times 10^2 \times 1000 = \mathbf{80\ \mu W}$$

The disparity between the bipolar and the MOSFET is self-evident. It is fair to acknowledge that it can be demonstrated that the BJT can be improved by converting its structure into a monolithic Darlington; but it is equally fair to say that the improvement would not equate to the drive efficiency demonstrated for the MOSFET.

Just as the preceding paragraphs have been used to highlight the difference between a particular BJT and a particular MOSFET, so it can be demonstrated that equal discrepancies also exist between MOSFETs from one supplier to another, and is not merely confined to the differences between *lateral* and *vertical* structures.

1.3 VARIOUS MGT STRUCTURES AND THEIR EFFECTS

A parasitic BJT is found within every MOSFET structure. This parasitic is easily discernible in Figure 1.1. In the case of the IGT this parasitic component becomes a thyristor. This parasitic thyristor does have the capability of latching on, especially if the IGT is incorrectly fabricated or used.

The possibility of the IGT latching is totally undesirable and the consequences to circuits may well be catastrophic. Techniques to prevent the latching of IGTs will be discussed later. From both of the adjacent cell structures of Figure 1.1, the two-junction transistor (NPN) structures are clearly in evidence. The base–emitter junction of the parasitic transistor within the lateral MOSFET structure indicates that the base of this NPN is open-circuit (it is connected externally to the N emitter), whereas the base–emitter junction of the vertical structure is found to be partially short-circuited by the source metallisation. Extensive detail of the oxide and metallisation is not shown. Very much more detail is given in Figure 1.4.

Examination of the equivalent circuit in Figure 1.2 will show that there is a resistor between the base and the emitter of the parasitic NPN.

The value of this base resistor (R_{be}), is dependent upon several factors — such as the base spreading resistance, the diffusion profile, the concentration of the dopant and the thickness of the source/emitter metallisation. The value for R_{be}, and how low it is will determine how good is the definition of the overall structure.

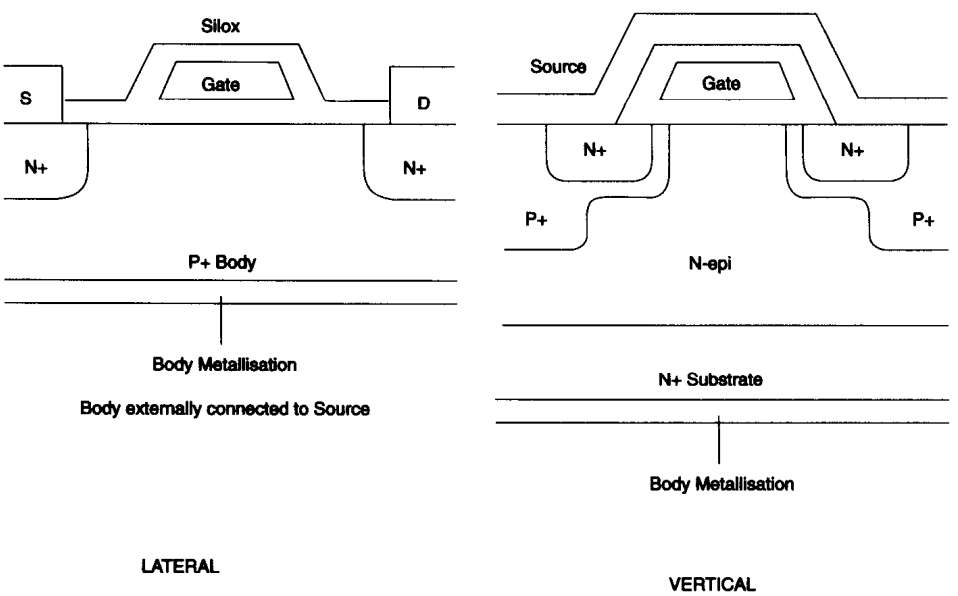

Figure 1.1 Illustration showing structure of MOSFET cell

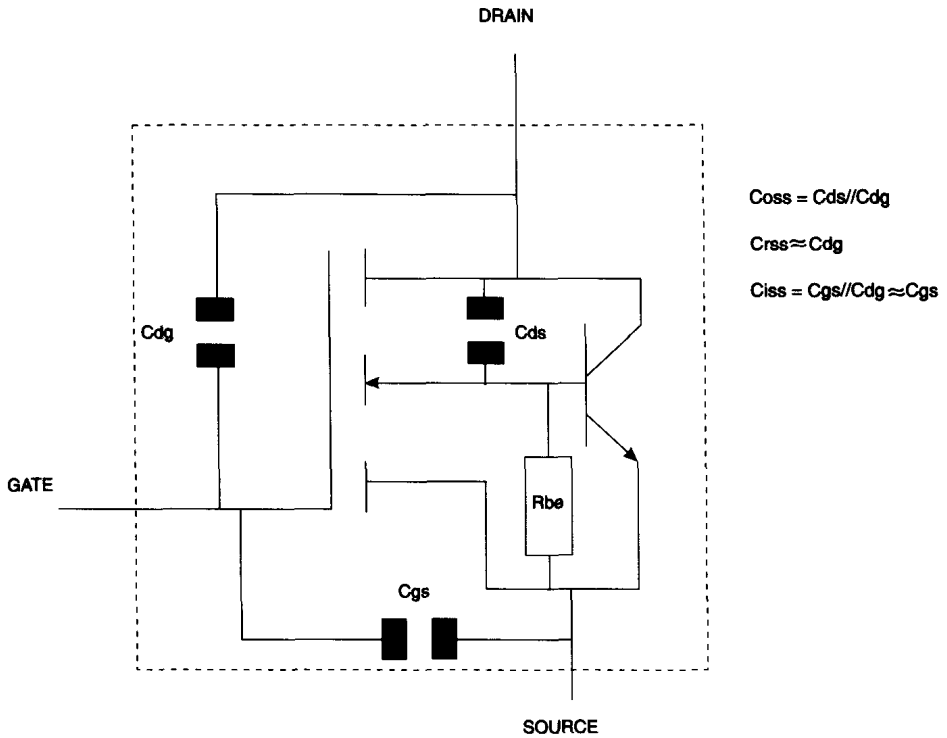

Figure 1.2 Equivalent circuit of MOSFET structure

If R_{be} was shown to be exactly equal to zero, then the only form of break-down which could be sustained by the NPN would be V_{cbo}. Any finite value of resistance (R_{be}) above zero would imply that the break-down characteristic will be modified and that at some value of avalanche current the base–emitter junction would become forward biased and that emitter injection would commence, resulting in the parasitic BJT turning on and entering into second breakdown.

The control of R_{be} and its final value usually indicates some measure of the ruggedness of the MOSFET. The ruggedness of MOSFETs will be found to vary from one manufacturer to another.

When considering the type of MOSFET to be included within any design, the designer should scrutinise the requirements of the design in its entirety. The performance of the chosen device will ultimately be reflected in the total system cost, which in turn will not only include the purchase price of components.

It is of little consequence if the build price of a particular piece of equipment happens to be the lowest in the market-place, if the same equipment proves to be completely unreliable. The cost of warranty service, and possible component replacement, could conceivably negate any profit which may have been accrued. Above all else will be the effect upon the goodwill and esteem of the end-user of the equipment.

The reliability of any piece of equipment can only reflect the equality which has been built into it.

The first golden rule, that will now be stated, should read: *Never skimp on the quality of components.*

It should be obvious that application of this rule should be tempered with some caution.

The designer may well imagine that he/she is forced to walk a tightrope over the decision of quality. This is only partly true, since there are also useful 'trade-offs' which may be made: trade-offs that will enable the use of components reflecting the highest standards of quality.

An excellent example of how 'Trade-offs' can be made is to consider how the use of rugged MOSFETs can lead to real savings in the overall cost of equipment.

Consider the use of a half-bridge topology in an off-line Switched Mode Power Supply (SMPS). In certain instances it would be mandatory to install 500 V (BV_{DSS}) MOSFETs as the power switches. But, virtually identical overall performance can be achieved by the judicious use of 400 V MOSFETs which are endowed with avalanche capability. The 400 V device should have the same $R_{ds[on]}$ as its 500 V counterpart but utilise a device that is possibly 25–50% smaller than its higher voltage sibling.

Proof of this assumption can readily be provided within the following paragraph.

The rectified d.c. bus voltage for a worst case off-line supply is approximately equal to 375 V (UK specification of 240 $\pm$ 10%. It is usual to include a margin of safety, in order that certain International Safety Legislation requirements be complied with. The safety margin will almost certainly include transient over-voltage capability due to stray inductances. In certain instances a double helping of safety is introduced by the incorporation of surge suppressors across the d.c. bus.

It is now prudent to examine all of the assumptions to determine where, if any, further savings may be made for a supply of 500 W of throughput power.

(1) It will be assumed that a RFI/EMI filter is found to be necessary. It is customary for such a filter to include an inductor in series with both line and neutral connections. It is also customary to have a capacitor connected from line to neutral immediately after the line and neutral inductors.

(2) If output hold-up is a specification requirement of the power supply then the capacitance of the reservoir capacitor post rectification will be considerable. The capacitance value for this capacitor can be calculated from:

$$C_{Res} = 2P_{out}/\varepsilon(t_{hold\text{-}up}/(V_1^2 - V_2^2) \qquad (1.9)$$

where $t_{\text{hold-up}}$ is the hold-up time for the output (and is usually quoted for 'half a missing mains cycle' or may for a high specification supply even cater for a 'a whole missing mains cycle' — a part of the specification that is sometimes called the Brown-out specification), P_{out} is the output power of supply, V_1 is the minimum d.c. bus voltage (derived from the supply's input specification), and V_2 is the d.c. bus voltage where output regulation can no longer be maintained, C_{Res} is the capacitance of the reservoir capacitor and ε is the target efficiency of the supply.

For the 500 W supply as (defined earlier) with a hold-up time of 38 ms (one missing 50 Hz cycle); and with an efficiency of 75% and using equation (1.9) it can be shown for $C_{\text{Reservoir}}$ to have a capacitance of 1320 μF.

The energy which this capacitor can absorb without exceeding the BV_{DSS} of the MOSFET can be deduced from:

$$E_{\text{clamp}} = C_{\text{Res}}(V_{\text{DS}}^2 - V_{\text{hl}}^2)/2 \tag{1.10}$$

where E_{clamp} is the energy required to raise the voltage across the reservoir capacitor C_{Res} from the UK high-line voltage of 375 V d.c. to $V_{\text{DS}} = 400$ V, the clamped safe value of BV_{DSS}.

For a high-line voltage of 264 V a.c., and the reservoir capacitance calculated by using equation (1.9) above the clamp energy can be demonstrated to be greater than 12 joules. This energy capability is in excess of the published safety legislation specifications and shows that 400 V MOSFETs can be utilised provided one further precautionary measure is also undertaken.

This measure is to ensure that the total voltage stress which is applied across the MOSFET does not exceed BV_{dss}. This voltage stress will usually be generated by the load and also by any stray inductance within the circuit.

One possible method that is frequently employed is the use of *current snubbers*. The use of current snubbers is advocated across the load (which in this instance will usually be a transformer). The use of other snubbers may, on the other hand, prove to be unwarranted.

The maximum transient voltage owing to stray inductances can be determined from:

$$V_{\text{transient}} = BV_{\text{dss}} - V_{\text{hl}}$$

where V_{hl} is the high-line voltage and has been demonstrated to be equal to 375 V for the d.c. bus. $V_{\text{transient}}$ is regarded as being equal to the integral of L_{stray} and the rate of change of current through the stray inductance L_{stray}.

The value of L_{stray} should be minimised as a matter of principle but can be determined (empirically) as being equal to 10 nH in value for every inch of excess chassis wiring or length of printed circuit-board track.