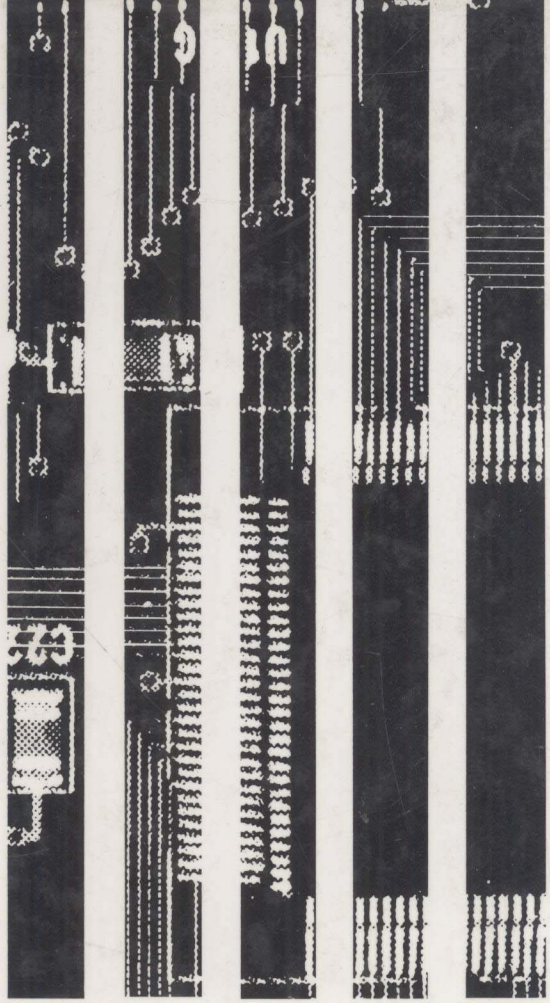

HIGH SPEED DIGITAL ELECTRONICS

L. J. HERBST

High Speed Digital Electronics

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PREFACE

Submicron structures, subnanosecond switching speeds and high function densities spearhead very large–scale integrated circuit (VLSI) development. In respect of speed the thrust for producing faster digital integrated circuits (ICs) is now universal.

The purpose of this text is to impart an understanding of the factors which determine the switching speed of ultrafast bipolar, MOS, and GaAs digital ICs. The foundations for that purpose are device physics, processing technology, and circuit techniques. Microelectronic engineering is basically composed of electrophysics, computing, and systems. It is the electrophysics constituent which is placed to the fore in this book, but not to the point of eclipsing circuit techniques and system aspects.

The approach adopted reflects a trend which is increasingly evident in the USA and in Western Europe, probably more in the former than the latter. A tendency to emphasise circuit techniques and analysis is giving way to a tripartite coverage of device action, processing technology, and circuit techniques, all combined with system aspects.

This book arose out of a course held in 1984. That course was a

collaborative venture by the Science and Engineering Research Council (SERC) of Great Britain and the informatics Technology Group (ITG) within the Scientific and Technical Research Committee (CREST) of the European Community (EC). Following a proposal made in 1982, the SERC/CREST-ITG advanced course 'The Quest for Speed - Sub-nanosecond Digital Electronics' was mounted at Teesside Polytechnic from 3-14 September 1984.

The course was not confined to a coverage of research at the forefront of the subject. Its philosophy also included paying attention to engineering realities. An appraisal of achieving anticipated performance based on research and advanced development imparted an ethos which differed from the customary concentration of many advanced courses on research alone. The fundamentals of the subject naturally occupied a key role, but were supplemented by engineering aspects directed at the art of the possible. The result was a presentation reflecting the engineering 'dimension', which has been discussed so much in Great Britain and the USA and which, for very good reasons, we are being asked to impart in our higher education. Indeed the course had a tutorial character.

An innovative feature of the SERC/CREST-ITG advanced courses was their planning procedure. The majority of the lecturers met for several days in April 1984 at the Education and Training Centre of the Atomic Energy Research Establishment, Harwell, and planned the course in detail. The resulting structure is reflected in this text. Apart from establishing the general course philosophy, which has already been outlined, our deliberations led to a number of other decisions. One of these was to treat MOS ICs in their totality, and not to present CMOS, which was then already the preferred emerging technology, in isolation. Another - probably the most decisive step we took - was to include GaAs. There was next to no US Government support for GaAs ICs in April 1984. The determined move into that field by Japan was

only announced at about the time when the course was held early in September 1984.

With GaAs being the newest of the three technologies for digital ICs, more material is devoted to GaAs than to bipolar or MOS ICs. GaAs subjects occupy six chapters, and there is a further chapter on a GaAs related topic, the heterojunction bipolar transistor. MOS fundamentals are covered in two chapters, which deal with device physics, scaling, and technology. The basic material on bipolar ICs consists of three chapters on processing, modelling, and circuit techniques.

In addition to the subjects contained in the twelve chapters mentioned above, several other topics have been included. One of these is a novel bipolar logic gate with a propagation delay well down in the subnanosecond region. Semiconductor memories occupy a key role in digital electronics. A chapter on nMOS memories highlights the principles of organisation and routing logic. Much of that material also holds for silicon bipolar and CMOS memories. This chapter explains some of the limitation memory architectures impose on speed. Finally, there are two chapters on optical systems and communication requirements. These have been included because telecommunications, which has tremendous growth potential, provides one of the biggest outlets for ultrafast digital ICs.

By and large the coverage of bipolar, MOS, and GaAs technologies given on the course held in 1984 still applies, although some material, take for example references to current practice, is occasionally a little dated. Eleven of the thirteen authors work in industrial establishments at the forefront in their respective fields. Consequently they could interpret the state of their technologies several years ahead of translation into commercial products. Furthermore, a substantial proportion of the text consists of contributions which were completely rewritten, not just revised, in the years 1985 to 1988. The

chapters in question are 2, 3, 7, 8, 9, 12, 13, 14 and 16.

The rewritten contributions not only afforded the opportunity for updating, but are also enlargements of the original material, slanted in directions which make for greater cohesion of the entire text.

This book should have a wide appeal to electronics and computer engineers. Ultrafast digital electronics is no longer the specialist subject it was some years ago. Subnanosecond switching, linked with submicron engineering – which features implicitly in much of the text – is now becoming commonplace, with the structures of commercial VLSI presently on the 1 μm boundary and progressing rapidly to submicron dimensions. This text will be of interest not only to staff in industrial research, development, and production establishments, it will also be attractive for academics and students in higher education, especially for those engaged on taught Masters courses and PhD programs. Its outstanding characteristic is that it combines bipolar, MOS, and GaAs technologies. That feature will enable readers to appreciate their relative merits and to make critical comparisons.

Numerous publishers have kindly given permission to use material from their books or journals. Appropriate acknowledgements are made where due in the text. Chapter 4, a reprint with minor modifications of an article by its author in Electronics, April 1982, is published by permission of Penton Publishing, USA. It remains for me to thank all the authors for their unstinting cooperation, which has made the production of this book possible. Likewise the help and co-operation received from the publisher at all stages is gratefully acknowledged.

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Chapter One

BIPOLAR PROCESSES FOR SUBNANOSECOND DIGITAL ELECTRONICS

P. Ashburn

1.1 INTRODUCTION

Recent advances in bipolar integrated circuit processes, featuring polysilicon and self-alignment techniques, have greatly increased the potential of bipolar technology for realising subnanosecond digital circuits. These advances have led to a reduction of the gate delay of high density, low power I^2L circuits to below 1 ns and of high performance non-saturating circuits to below 100 ps [1]-[5]. This improved performance has been achieved by minimising the large parasitic extrinsic regions of the bipolar device, which degrade the performance and limit the packing density of conventional bipolar circuits.

The earliest techniques for reducing the parasitic extrinsic regions of the bipolar transistor employed polysilicon instead of metal to provide contact to the base of the device [6]. This had the effect of reducing the collector-base area of the transistor by avoiding the limitation imposed by the metal pitch. By combining this technology with a technique for selectively etching the polysilicon, other authors [1]-[5] have shown that the emitter region of the transistor can be self-aligned to the base contact, allowing further significant reduction in