

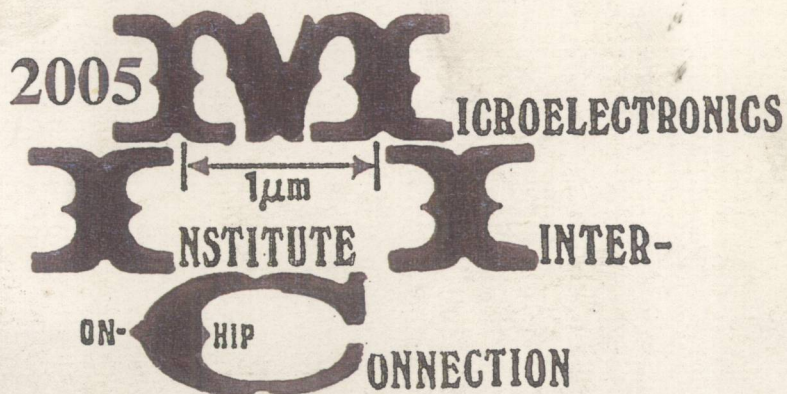
February 23 - 25, 2005

CMP-MIC Catalog No.  
05 IMIC - 1000P

Marriott Hotel  
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2005  
PROCEEDINGS  
NINTH INTERNATIONAL  
CHEMICAL-MECHANICAL  
PLANARIZATION  
FOR  
ULSI MULTILEVEL  
INTERCONNECTION  
CONFERENCE  
(CMP-MIC)

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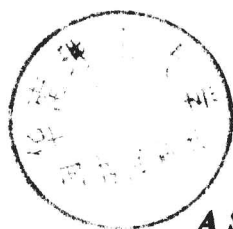
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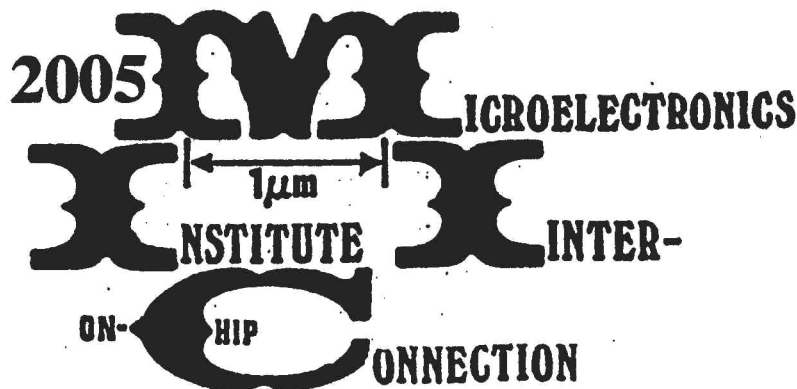
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**2005**  
**PROCEEDINGS**  
**NINTH INTERNATIONAL**  
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**PLANARIZATION**  
**FOR**  
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**INTERCONNECTION**  
**CONFERENCE**  
**(CMP-MIC)**



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**TENTH INTERNATIONAL  
CHEMICAL-MECHANICAL POLISH (CMP)  
FOR ULSI MULTILEVEL INTERCONNECTION  
CONFERENCE PROCEEDINGS**

*A Specialty Conference of IMIC*

**Papers have been printed without editing as received from the authors.**

**All opinions expressed in the Proceedings are those of the authors and are not binding on the CMP Planarization for Multilevel Interconnection Conference organizers.**

**CMP-MIC Catalog Number 05 IMIC-1000P**

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# **CMP-MIC/2005**

*A Specialty Conference of IMIC*

## **CONFERENCE OBJECTIVES**

To assemble researchers and technical support personnel from Industry, Universities and Government Laboratories from around the globe to address all current and future issues related to CHEMICAL-MECHANICAL POLISH (CMP) PLANARIZATION for on-chip ULSI Multilevel Interconnection applications. Topical areas include, but are not restricted to, the following: developments in dielectric and metal CMP processes & control; modeling and simulation theory; CMP process integration for dielectric & metals; contamination and (pre & post) cleaning issues; CMP consumable developments (pads/slurries/etc.); equipment and manufacturing issues; characterization and test; CMP standards developments; alternative global planarization techniques as compared to CMP.

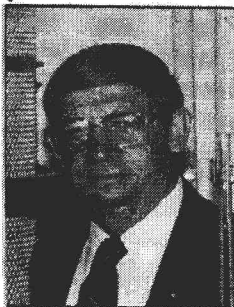
## **WELCOME STATEMENT FROM THE GENERAL CHAIRMAN**

It is my distinct pleasure to extend to you a cordial welcome to the Tenth International CHEMICAL-MECHANICAL POLISH (CMP) for ULSI Multilevel Interconnection Conference held at the Marriott Hotel in Fremont, CA. An outstanding program has been planned consisting of over 95 technical papers (involving some 250 authors) from 32 different semiconductor industries, universities and government laboratories from across the U.S. as well as 4 other countries. I wish to express my sincere appreciation to the 2005 CMP-MIC Executive Committee members for assisting with this program.

Concerning the topic of this conference, there are many challenges and much to be accomplished. For as the density of ULSI circuits continues to increase for decreasing design dimensions, resulting from improved lithography and associated patterning technology, it becomes imperative that a multilevel interconnection system incorporating a global planarization system (like CMP) be employed in order to accommodate the lithography requirements, and to make systems incorporating submicron features a reality. This conference is complimented by another IMIC Specialty conference usually held in the Fall which looked at a number of issues related to the on-chip dielectrics and conductors ('05VMIC) for application in ULSI multilevel interconnection. Low dielectric constant insulating materials, global planarization using CMP and high conductivity metals are some of the most important issues in advancing multilevel interconnection into the next century. In order to maintain our rate of scaling ULSI circuitry in the future, these and other issues must be addressed.

It is anticipated that this conference as well as future VMIC Conferences and IMIC Specialty Conferences will address many of these issues such that workable solutions may be derived.

Again, welcome to CMP-MIC/05.



**Thomas E. Wade, Ph.D.  
General Chairman**



## CONFERENCE REGISTRATION

2005 CMP-MIC participants may register either in advance or at the door. For **Advance Registration**, your application and payment check or money order must be received no later than **February 12, 2005**. Those who register in advance may pick up all conference information (including Proceedings) at the registration desk. Additional registration forms may be obtained by calling the CMP-MIC Conference Secretary at (813) 978-3552. **Applications received without payment will not be honored as advance registration. Also, no confirmation of advance registration receipt will be sent.**

**Cancellation:** Refunds for cancellations of advance registration will be honored provided the request to cancel are made in writing and are received no later than **February 11, 2005**. No telephone calls will be accepted. All refunds for cancellation will be subject to a \$50.00 handling charge. Refunds will be sent after the Conferences.

**Registration** entitles an attendee admission to all sessions, handouts, coffee breaks, a set of the official Proceedings of the Conference, a box lunch on Wednesday, and the CMP-MIC Luncheon on Friday.

**Payment for Advance Conference Registration must be in the form of a check (in US dollars drawn on a US bank), money order, travelers checks or credit cards. Purchase orders can not be accepted.**

**At-the-Door Registration** may be accomplished at the following times:

### CMP SHORT COURSE REGISTRATION

Tuesday, Feb. 22.....7:00 a.m.- 3 p.m.

### CMP-MIC REGISTRATION

Tuesday, Feb. 22..... 4:00 p.m. - 6:00 p.m.

Wednesday, Feb. 23 .....7:30 a.m. - 12 p.m.

Thursday, Feb. 24.....7:30 a.m. - 12 p.m.

Friday, Feb 25 .....7:30 a.m. - 11 a.m.

## CONFERENCE BADGES

All attendees **must wear** their conference badge for admission to **all sessions**. For this meeting, there will be no single day registration option.

## TECHNICAL POSTER SECTION

The 2005 CMP-MIC will sponsor a "Technical Poster Section" in an adjacent room to the Lecture Hall. Posters will be on display Wednesday, Thursday and Friday, Feb. 23 - 25 from 9 a.m. until 4 p.m. A four-page extended abstract of each poster paper will be published in the 2005 CMP-MIC Conference Proceedings.

## FREMONT MARRIOTT HOTEL

**Fremont Marriott Hotel** is set at the gateway to Silicon Valley, between the McCarthy Ranch and Pacific Commons office parks, the Fremont Marriott is conveniently located at the southern tip of the San Francisco Bay just north of San Jose. As the only full-service hotel in Fremont, it provides an elegant and accommodating atmosphere, near numerous Bay Area attractions, the Napa Valley and world-renowned high-tech headquarters. Attractions & Landmarks includes the Shoreline Amphitheatre, Great Mall of the Bay Area, Paramounts Great American Theme Park, Compaq Arena - San Jose Sharks, Livermore Valley Wineries, Network Associates Oakland Coliseum, etc.

Parking is free for CMP-MIC hotel guest.

## **2005 CMP-MIC COMMITTEES**

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Jerry Yang, ROHM & HAAS  
Akihiko Yamane, SEIMITSU  
Tao Zhang, JAZZ SEMI**





**TENTH INTERNATIONAL  
C.M.P. PLANARIZATION  
FOR ULSI MULTILEVEL INTERCONNECTION  
CONFERENCE**

**February 23 - 25, 2005**

Wednesday, February 23, 2005  
**OPENING SESSION - 8:30 A.M.**

Welcoming Remarks  
**Dr. Thomas E. Wade, Gen. Chmn.**  
University of South Florida

**SESSION I -- 8:30 A.M.**

**KEYNOTE ADDRESS - Part I**

From a Semiconductor Manufacturers' Perspective for  
Future CMP, Where Should the Following be Targeted:

- Industry/University R & D Efforts
- Government/Consortia Funding
- CMP Vendor Developments

**PANEL MODERATOR**

Peter Singer  
Editor-in-Chief

*Semiconductor International*

**SEMICONDUCTOR IND. PANEL**

Laertis Economikos, IBM, Hopewell Jct., NY  
Mark Buehler, Intel, Hillsboro, OR  
Chris Raeder, AMD, Austin, TX  
Pete Beckage, Freescale, Austin, TX  
Takeshi Nogami, Sony, Tokyo, JAPAN  
Peter Thieme, Infineon, Dresden, GERMANY

A brief Question & Answer period will follow  
formal presentations.

Coffee Break 10:30 - 10:45 AM

**SESSION II - 10:45 A.M. - 12:00 P.M.**  
**VLSI MULTILEVEL INTERCONNECTION**  
**CMP CONSUMABLES - PART I**

**Chairman:** Dr. Ara Philipossian  
UNIV. Of ARIZONA  
Tucson, Arizona

- 2.A "Challenges of Implementing New Slurry  
Chemistries in High Volume Manufacturing" by  
B. Ferney, S. Narayanan and J. Thibado; INTEL  
CORP.; Hillsboro, OR. 17  
*Invited Paper*
- 2.B "Design Rules for CMP Pad Based on Pad-  
Characterization and its Prototype Fabrication  
Using Micro Molding" by S. Lee, H. Kim and D.A.  
Dornfeld; UNIV. Of CALIFORNIA, Berkeley, CA. 25
- 2.C "Pad Conditioning and Textural Effects in  
Chemical Mechanical Polishing" by A.S. Lawing;  
ROHM & HAAS; Phoenix, AZ. 33  
*Invited Paper*

- 2.D "Effect of Diamond Disc Conditioner Design and  
Kinematics on Process Hydrodynamics During  
Copper CMP" by A. Philipossian, Z. Li, H. Lee;  
UNIV. Of ARIZONA; Tucson, AZ.; L. Borucki,  
INTELLIGENT PLANAR; Mesa, AZ., R. Kikuma,  
N. Rikita, K. Nagasawa; MITSUBISHI; JAPAN. 43  
*Invited Paper*

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- 2.E "Chemical Analysis of Copper CMP Slurries  
Before and After Polishing for Defect Reduction"  
by F. Odeh, K. Cheemalapathi, V.R. Duvvuru, D.K.  
Bundi, S. Dhane and Y. Li; CLARKSON UNIV.;  
Potsdam, N.Y. 53
- 2.F "Cermet Ceramic Coating of Diamond Dresser for  
In-Situ Dressing of Chemical Mechanical  
Planarization" by J.C.M. Sung and K. Kan; KINIK;  
Taiwan, R.O.C. 58
- 2.G "Filled Polyurethane Pad for Chemical Mech-  
anical Polishing" by G. Wu, P. Galvez, S. Kirtley,  
T. West; THOMAS WEST; Sunnyvale, CA. 62
- 2.H "Characterization of a Copper CMP Slurry" by  
R.K. Singh, C. Patel; MYKROLIS; Billerica, MA.;  
B.R. Roberts; BOC EDWARDS; Santa Clara, CA.;  
and R. Viscomi; CABOT MICRO; Phoenix, AZ. 67

**SESSION III - 1:00 - 3:00 P.M.**

**VLSI MULTILEVEL INTERCONNECTION**  
**CMP PROCESS MONITORING & CONTROL**

**Chairman:** Dr. Norm Gitis  
CENTER FOR TRIBOLOGY  
Campbell, California

- 3.A "Analysis of Particle Flow During CMP Process  
Using Particle Image Velocimetry" by Y.H. Koh,  
H. Kim, B.U. Yoon, C. Hong, H. Cho and J.T.  
Moon; SAMSUNG; Yougeen, SOUTH KOREA;  
and S. Shin, M. Kim and Y. Yoon; SEOUL UNIV.;  
Seoul, SOUTH KOREA. 73
- 3.B "CMP Consumables Characterization" by N.  
Gitis, M. Vinogradov, S. Kuiry; CTR. for  
TRIBOLOGY; Campbell, CA. 82
- 3.C "Particulate Flow Tribological Issues During  
CMP of Nanostructures" by C. F. Higgs III, E.  
Terrell, J Garcia; CARNEGIE MELLON UNIV.;  
Pittsburg, PA. 87  
*Invited Paper*
- 3.D "Instantaneous, High Resolution, In-Situ Imaging  
of Slurry Film Thickness During CMP" by C.  
Gray, D. Apone, C. Rogers and V. Manno; TUFTS  
UNIV.; Medford, MA.; C. Barns, M. Moinpour;  
INTEL CORP; Santa Clara, CA.; S. Anjur; CABOT  
MICRO.; Aurora, IL.; and A. Philipossian; UNIV.  
Of ARIZONA; Tucson, AZ. 97

- 3.E "Measurement and Control of Slurry Film Thickness and Wafer Surface Temperature in CMP" by G.P. Muldowney, J. J. Hendron; ROHM & HAAS; Newark, DE. 105

--- POSTER PAPERS ---

- 3.F "CMP Process and Consumables Evaluation With PadProbe™" by S. Hosali, E. Busch; SEMATECH; Austin, TX.; and M. Vinogradov, N. Gitis; CENTER for TRIBOLOGY; Campbell, CA. 115
- 3.G "Friction Force Monitoring System in CMP Process" by H. Jeong, B. Park, H. Lee, H. Kim, H. Seo, G. Kim and K. Park; PUSAN NAT'L UNIV.; Pusan, KOREA; and M. Kinoshita, J. Park; NITTA HAAS; Nara, JAPAN. 119
- 3.H "Use of Segmented Algorithm to Improve Endpoint Repeatability for Copper CMP" by R. Carpio and E. LaBelle; ATDF; Austin, TX. 123
- 3.I "Erosion Characterization and Process Control in Copper CMP Process" by S. Lee, Z. Liu, C. Saravanan, J. Hu and R. Korlahalli; NANO-METRICS; Milpitas, CA. 127

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SESSION IV - 3:15 - 5:00 P.M.

VLSI MULTILEVEL INTERCONNECTION  
C.M.P. MODELING & SIMULATION -  
PART I

Chairman: Dr. Mike Fury  
DUPONT EKC TECH.  
Hayward, California

- 4.A "Applications of Full-Chip CMP Modeling: Copper, STI and Beyond" by T. Smith, D. White, R. Moore, B. Lee and A. Gowen-Hall; PRAESAGUS; San Jose, CA. 133  
*Invited Paper*
- 4.B "A Pad Wear Model for CMP Process Optimization" T.P. Merchant, J.N. Zabasajja; FREESCALE SEMI; Tempe, AZ.; L.J. Borucki; INTELLIGENT PLANAR; Mesa, AZ.; and A. S. Lawing; ROHM & HAAS; Phoenix, AZ. 143
- 4.C "Accurate 3-D Capacitance Test and Characterization of Dummy Metal Fills to Achieve Design for Manufacturability" by K. J. Chang, D.C.H. Lyu; TSING HUA UNIV.; Taiwan, R.O.C.; and Y.C. Chiu, E. Chang and L. Chen; UNITED MICRO. CORP; Taiwan, R.O.C. 151
- 4.D "Optimization of CMP Pad Groove Arrays for Improved Slurry Transport, Wafer Profile Correction and Defectivity Reduction" by G.P. Muldowney; ROHM & HAAS; Newark, DE. 156

- 4.E "Flash Heating in Chemical-Mechanical Polishing" by L. Borucki; INTELLIGENT PLANAR; Mesa, AZ.; and Z. Li, Y. Sampurno, J. Sorooshian, Y. Zhuang and A. Philipossian; UNIV. Of ARIZONA; Tucson, AZ. 168

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- 4.F "The Multi-Product Oxide CMP Mixing Process Control by Auto Feedback System" by Y. Hung, A. Su and M. C. Yang; PROMOS TECH.; Taiwan, R.O.C. 179
- 4.G "A Theoretical Study on the Relationship Between Wafer Surface Pressure and Wafer Backside Loading in CMP" by G. Fu and A. Chandra; IOWA STATE UNIV.; Ames, IA. 183

Thursday, February 24, 2005

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**KEYNOTE ADDRESS - Part II**

From a Vendor / Marketing Consultants Perspective for Future CMP, Where Should the Future Advancements be Targeted?

**PANEL MODERATOR**

Peter Singer  
Editor-in-Chief

*Semiconductor International*

**VENDOR / MKT. PANEL**

Cathie Markham, VP Tech., Rohm & Haas  
Cliff Spiro, VP Res., Cabot Microelectronics  
Robert Castellano, Pres., Information Network

A brief Question & Answer Period will follow formal presentations.

Coffee Break - 9:15 A.M. - 9:30 A.M.

SESSION VI - 9:30 A.M. - 12:30 P.M.  
VLSI MULTILEVEL INTERCONNECTION  
CMP PROCESS CHARACTERIZATION  
& POST-CLEANING PROCESSES

Chairman Dr. Mansour Moinpour  
INTEL CORP.  
Santa Clara, California

**CMP PROCESS CHARACTERIZATION**

- 6.A "Electro-Chemical Mechanical Planarization and Its Evaluation on BEOL with 65 nm Node Dimensions" by A. Sakamoto, T. Nogami; SONY; Tokyo, JAPAN; L. Economikos, W.T. Tseng; IBM MICRO; Hopewell Junction, N.Y.; P. Ong, Y. Moon; AMD Corp.; M. Naujok; INFINEON TECH.; J. Salfelder, A. Duboust; APPLIED MATERIALS; Santa Clara, CA. 191  
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- 6.B "Use of an Electrochemical Quartz Crystal Microbalance to Elucidate the Adsorption of Glycine and Hydrogen Peroxide on Copper Surfaces" by L.Wang, F. Doyle, UNIV. CALIF; Berkeley, CA. 200  
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- 6.C "Dielectric and Copper CMP - the Evolution of Integrated Process Control and Solutions Down to 65 nm and Below" by M. Finarov, A. Ger and G. Dishon; NOVA INST.; Rehovoth, ISRAEL. 210  
*Invited Paper*

- 6.D "Manipulation Effects in Chemical-Mechanical Polishing" by M. Kulkarni, D. Ng, H. Liang; TEXAS A & M UNIV.; College Station, TX.; J. Johnson and A. Zinovev; ARGONNE NAT'L LAB; Argonne, IL. 219  
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- 6.E "Effect of Slurry Temperature and Flow Rate on Material Removal In Chemical Mechanical Polishing Process" by H. Kim, S. Lee, J. Choi and D. Dornfeld; UNIV. Of CALIFORNIA; Berkeley, CA.; and H. Jeong; PUSAN UNIV.; KOREA. 225

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- 6.G "A Non-BTA Based Novel Post CMP Clean/Holding Solution" by J. Zhao, D.K. Bundi, K. Cheemalapati, V.R. Duvvuru and Y. Li; CLARKSON UNIV.; Potsdam, N.Y. 239  
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- 6.H "Experimental and Modeling Study of Submicron Particle Removal from Deep Trenches" by K. Bakhtari, R.O. Guldiken and A.A. Busnaina; NORTHEASTERN UNIV.; Boston, MA.; J.G. Park; HANYANG UNIV.; Ansan, KOREA. 244  
*Invited Paper*

- 6.I "Advancements in Post Copper CMP Cleaning Solutions" by C. Shang, D. Frey, D. Maloney; DUPONT/EKC TECH; Hayward, CA.; K. Matsumoto; DUPONT/EKC TECH; Kawasaki, JAPAN. 248  
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- 6.K "Device Failure Mechanism Through Particle Adhesion" by G.S. Cho, H.S. Kim, J.K. Lee, J.D. Jeong, D.Y. Kim, Y.W. Lee, H.P. Kim, H.S. Jeong, H.W. Ha, W.S. Yang; ANAM SEMI.; Kyunggi, KOREA. 263

- 6.L "Effect of Barrier Slurry Properties on Post-CMP Cleaning Efficacy" by D. Peters, K. Bartosh, C. Watts and C. Tran; ATMI; Allentown, PA. 267

Thursday Lunch on Your Own  
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#### SESSION VII - 1:15 P.M. - 2:30 P.M. VLSI MULTILEVEL INTERCONNECTION DEDICATED TIME FOR CMP POSTER PAPERS, EXHIBIT VIEWING

#### SESSION VIII - 2:30 P.M. - 5:45 P.M. VLSI MULTILEVEL INTERCONNECTION C.M.P. CONDUCTOR & DIELECTRIC PROCESSES

Chairman: Dr. David Dornfeld  
UNIVERSITY OF CALIFORNIA  
Berkeley, California

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- 8.A "Stress-Free Copper Planarization Using A Modified Electrochemical System" by J. Huo and J. McAndrew; AIR LIQUIDE; Countryside, IL. 277
- 8.B "Effect of Hydrogen Peroxide on Frictional and Thermal Characteristics During Copper CMP" by J.G. Park, H. Eom; HANYANG UNIV; KOREA. 284  
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- 8.C "Competative Surface Adsorption of Key Chemicals on Abrasive Particles in Copper CMP Slurry" by S.K. Govindaswamy, F. Odeh, S. Dhane and Y. Li; CLARKSON UNIV.; Potsdam, N.Y. 292
- 8.D "Novel Low-Abrasive Slurries and Abrasive-Free Solutions for Copper CMP" by I. Belov, J.Y. Kim, T. Moser, K. Pierce; PRAXAIR; Indianapolis, IN. 300

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- 8.E "Copper Surface Roughness Management for Optimal Copper CMP Performance in 65 nm Technology Node and Beyond" by C.L. Hsu, W.C. Su, C.C. Huang; UNITED MICRO CORP.; Taiwan, R.O.C.; and Q.C. Ye, T. Thomas, R. Lavoie and C.F. Dai; ROHM and HAAS; Newark, DE. 311
- 8.F "Chemical Inert Tungsten Particle in a Tungsten CMP Process" by L.H. Whye, A. Tan, R. Soh, T.C. Yong, C.K. Wei, C.C. Peng, T. A. Seng, N.T. Leong. W.F. Inn; S.S.M.C.; SINGAPORE. 315
- 8.G "Copper Removal Rate Control in Chemical Mechanical Polishing of Barrier Materials" by Z. Liu and R. Schmidt; ROHM & HAAS; Newark, DE. 320



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- 8.H "Polishing Performance of CeO<sub>2</sub> Base Slurry and Surfactant on STI Structure Wafers" by P.H. Sun, Y.C. Chen, K.T. Liao, T.H. Yu; WINBOND; Taiwan, R.O.C. 327  
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- 8.I "Investigation of Ceria-Silica Interactions During STI Polishing" by J. T. Abiade, S. Jung, S. Yeruva; UNIV. Of FLORIDA; Gainesville, FL.; and R.K. Singh; UNIV. Of TEXAS; Austin, TX. 335  
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- 8.J "STI CMP Scratch Reduction by Slurry Improvements: Additive & Abrasive Control & Optimization" by J.H. So, D.J. Lee, N.S. Kim, K.M. Kang, S.M. Chun; SAMSUNG; Youngin, KOREA; and S.M. Yang; KOREA INST. Of SCIENCE & TECH; Daejeon, KOREA. 339  
*Invited Paper*
- 8.K "Process Development of a Hybrid Fixed Abrasive STI CMP for Logic Applications at 65 nm Technology Node" by T.C. Tsai, N. Chen, S.K. Chu, C.H. Chen, C. Huang and S.F. Tzou; UNITED MICROELECTRONICS CORP; Taiwan, R.O.C. 348  
*Invited Paper*
- 8.L "Effects of Abrasive Size and Surfactant Concentration in Ceria Slurry for Shallow Trench Isolation CMP" by H.S. Park, J.G. Jung, J.Y. Park, J.H. Shin, C.H. Ryu, H.C. Sohn; HYNIX SEMI; Kyunggi, KOREA; H.G. Kang, T. Katho and J.G. Park; HANYANG UNIV.; Seoul, KOREA. 357
- 8.M "Fumed Ceria for Use in ILD and STI CMP" by M. Kroll, W. Lortz; DEGUSSA; Hanau, GERMANY; R. Brandes; DEGUSSA; Piscataway, N.J.; and A. Philipossian; UNIV. Of ARIZONA; Tucson, AZ. 366
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- 8.N "Recent Advances in Ceria-Based Slurries for STI and ILD Applications" by B. Her, D. Merricks and B. Santora; FERRO; Penn Yan, N.Y. 377
- 8.O "CMP Performance of NF<sub>3</sub> Added SiO<sub>2</sub> Film Using Two Kind of Slurries" by J.H. Kim, H. Lee, H.J. An, Y.H. Yoon, H.H. Kim, E.R. Hwang, S.H. Pyi, B.H. Choi, J.W. Kim and S.W. Park; HYNIX SEMI; Kyungki, KOREA. 387
- LATE NEWS PAPER --
- 8.P "A Method of Reducing the Effect of Heat on the Spindle Pressure Regulators in the Applied Materials Mirra Polisher" by M.K.M. Fei, H.S. Hyun, N.T. Leong, P.C. Siong, L.T. Wei, L.K. Fai, K.C. Chyan and P.Y.K. Hoe; S.S.M.C.; SINGAPORE. 393

## Friday, February 25, 2005 SESSION IX - 8:00 A.M. - 9:20 A.M. VLSI MULTILEVEL INTERCONNECTION CMP INSTRUMENTATION & HARDWARE

**Chairman:** Dr. David Hansen  
NOVELLUS CORP.  
San Jose, California

- 9.A "Wide Area AFM With Digital Probing Method for CMP Process Evaluation" by H. Koyabu; HITACHI; Tokyo, JAPAN; Y. Kembo; HITACHI; Tsuchiura, JAPAN; S. Hosaka; GUNMA UNIV.; Gunma, JAPAN. 397
- 9.B "Precision Point-of-Use Blending for CMP and Post-CMP Cleaning Chemicals" by D.J. Albrecht and B. Paterson; ENTEGRIS; Minneapolis, MN. 405
- 9.C "In-Situ Acoustic Emission Monitoring of Surface Chemical Reactions for Copper CMP" by J. Choi, D.E. Lee and D.A. Dornfeld; UNIV. Of CALIFORNIA; Berkeley, CA. 415
- 9.D "PiezoChuck Technology for Improved CMP Planarization Result" by V. Galazky, C.T. Weber, J. Weiser; IGAM ENGR; Barleben, GERMANY. 423

## -- POSTER PAPERS --

- 9.E "Shear Force Study of Low-k / Copper CMP For 65 nm Generation and Beyond" by L.G. Chen, H.H. Lu, W.C. Chiou, Y.H. Chen, S.M. Jeng, S.M. Jang, C.H. Yu and M.S. Liang; T.S.M.C.; Taiwan, R.O.C. 431
- 9.F "Spectral Imaging Technology for Fast Characterization of CMP Test Wafers" by C. Chen, S. Chalmers and R. Geels; FILMETRICS; Sunnyvale, CA. 436

Coffee Break 9:20 A.M. - 9:35 A.M.

## SESSION X - 9:35 A.M. - 12:00 P.M. VLSI MULTILEVEL INTERCONNECTION C.M.P. CONSUMABLES Part II

**Chairman:** Dr. Paul Feeney  
CABOT MICRO.  
Aurora, Illinois

- 10.A "The Effect of Pad Topography on Surface Non-Uniformity in Copper CMP" by K. Noh, K. Kopanski, N. Saka and J.H. Chun; M.I.T.; Cambridge, MA. 443

- 10.B "Break-In Pad Surface Analysis With FT-IR and Raman Scattering Spectroscopy" by T. Fujita, O. Kinoshita; SEIMITSU; Tokyo, JAPAN; M. Ishikura, N. Kawai, Y. Morioka; NITTA HAAS; Tokyo, JAPAN. 452
- 10.C "Fujimi Next Generation Tungsten CMP Slurry" by P. Lefevre, K. Sakai, K. Ohno, K. Tamai and K. Ina; FUJIMI; Tualatin, OR. 460
- 10.D "Direct Wafer Polishing With 5 nm Diamond" by J.C.M. Sung; KINIK; Taiwan, R.O.C. 471
- 10.E "Advanced Barrier Slurries for 65 nm and 45 nm Technology Nodes" by A. Zutshi, K. Oka, H. Nojo, F. Coder, Q. Arefeen, J. Siddiqui; DUPONT NANOMAT'L; Hayward, CA. 479  
*Invited Paper*
- 10.F "The Effect of Ceria Slurry pH and Hersey Number on CMP of Silicon Dioxide" by J.H. Lim, S.K. Yun, J.D. Lee, B.U. Yoon, C. Hong, H.K. Cho and J.T. Moon; SAMSUNG; Gyeonggi, KOREA. 488
- 10.G "The Evolution of IC 1000™ in CMP" by D. Chambers and H. Rayle; ROHM & HAAS; Newark, DE. 494
- POSTER PAPERS ---
- 10.H "A Study of a Centipede Pad Dresser With Individual Controllable Leveling of Single Diamond Grits in Break-In Process" by Y.L. Pai, C.C. Teng, M.H. Chan, S.C. Huang, J. Sung; KINIK; Taiwan, R.O.C. 501
- 10.I "Politex Prima Pad: Continuous Improvement on Industry Standard Material" by K.S. White, N. Chechik, H. Sanford-Crane; ROHM & HAAS; Newark, DE. 505
- 10.J "A Novel Rotary Pad Material for Improved Lifetime in Copper CMP" by D. Lamb, C. Forrestal, K. Pierce; PRAXAIR; Indianapolis, IN.; J. Cianciolo, T. Dunn, C. Galloway; PRAXAIR; Salem, NH. 509
- 10.K "A Study on the Cutting Phenomena of the Pad Used in CMP Process by Single Diamond Grit" by C.C. Teng, J. Sung; KINIK; Y.S. Liao, H.W. Chou; NAT'L TAIWAN UNIV; Taiwan, R.O.C. 513
- 10.L "Characteristics of A New Pad With Micro-Holes on The Surface" by J.C. Yang, D.W. Kim, S.M. Cheon, J.D. Kim, S.H. Ryu; SAMSUNG; Gyeonggi, KOREA; J. Kim, J.Y. Lee, I.H. Park; SKC CHEMICAL; Chungbuk, KOREA. 517

**CMP-MIC LUNCHEON - 12:15 - 2:00 P.M.**

**"CAN SIX SIGMA WORK IN A FAST MOVING CMP INDUSTRY ?"**

**Cliff Spiro**

**Vice President for Research & Development**

**Adam Weisman, VP Operations**

**Julie Hensel, Director QC**

**CABOT MICROELECTRONICS CORP.**

**Aurora, Illinois**

**SESSION XI - 2:00 P.M. - 4:00 P.M.**

**VLSI MULTILEVEL INTERCONNECTION  
C.M.P. APPLICATIONS & RELIABILITY**

**Chairman: Dr. Peter Burke**  
**LSI Logic**  
**Santa Clara, California**

**CMP APPLICATIONS**

- 11.A "Carbon Nanotube Vias for Multilevel Interconnects Using CMP Techniques" by M. Nihei, A. Kawabata, S. Sato, D. Kondo, M. Horibe, H. Shioya, T. Iwai and Y. Awano; FUJITSU; Atsugi, JAPAN. 527  
*Invited Paper*
- 11.B "Chemical Mechanical Polishing: A Enabling Technology for 3-D Memories" by V. Dunton and S. Sivaram; MATRIX SEMI; Santa Clara, CA. 535  
*Invited Paper*
- 11.C "Innovation in Traditional CMP Applications" by P. Feeney, R. Vacassy, A. Walters, S. Anjur and T. Dear; CABOT MICRO; Aurora, IL. 542  
*Invited Paper*
- 11.D "Integration of CMP Into a 3-D Memory Process" by V. Dunton; MATRIX SEMI.; Santa Clara, CA. 547
- POSTER PAPERS ---
- 11.E "Accurate Characterization of Flash Memory Cell Capacitance for Optimal Sub-100 nm Embedded Flash Memory Process Design" by J.S. Wang, K.J. Chang; eMEMORY TECH.; Taiwan, R.O.C. 557
- 11.F "Development of a New Tungsten Polishing Pad Utilizing Outsource CMP Capabilities" by R.L. Rhoades; TOTAL FAB SOLN'S; Tempe, AZ.; and J. Bare, A.J. Clark and E. Atkinson; PSILOQUEST; Orlando, FL. 560

## **CMP RELIABILITY ISSUES**

- 11.G **"Study on the Degradation of the TDDB Reliability of Copper / Low-k Interconnects Caused by Copper CMP Process"** by Y. Yamada, N. Konishi, S. Watanabe, J. Noguchi, T. Jimbo and O. Inoue; HITACHI; Tokyo, JAPAN. 567  
*Invited Paper*
- 11.H **"Failure Analysis and Characterization Methods for Copper CMP"** by S. Kordic, L.F.T.z. Kwakman, M. de la Bardonnie, A. Berthoud; PHILIPS SEMI.; F. Lorut, S. Petitdidier, S. Courtas, C. Wyon, C. Trouiller; ST MICRO; K. Ly, M. Zaleski, B. Smith; FREESCALE; Crolles, FRANCE. 577  
*Invited Paper*

## **--- POSTER PAPERS ---**

- 11.I **"Design of Diamond Conditioner for Preventing Diamond Pull Out"** by J.F. Jiang, J. Tsay, Y.J. You, and S.N. Peng; T.S.M.C.; Taiwan, R.O.C.; P. Kim, E. Jan; SHINHAN DIAMOND; Shanghai, CHINA. 589



**TENTH INTERNATIONAL  
CHEMICAL-MECHANICAL POLISH (CMP)  
FOR  
ULSI MULTILEVEL INTERCONNECTION  
CONFERENCE**

**Wednesday, February 23, 2005  
8:30 - 10:30 A.M.**

**KEYNOTE ADDRESS - PART I**

**“From a Semiconductor Manufacturers’ Perspective for Future CMP,  
Where Should the Following be Targeted:**

- Industrial/University R & D Funding**
- Government/Consortia Funding**
- CMP Vendor Developments”**

**PANEL**

**Laertis Economikos, IBM, Hopewell Jct., NY  
Mark Buehler, Intel, Hillsboro, OR  
Chris Raeder, AMD, Austin, TX  
Pete Beckage, Freescale, Austin, TX  
Takeshi Nogami, Sony, Tokyo, JAPAN  
Peter Thieme, Infineon, Dresden, GERMANY**

**PANEL MODERATOR**

**Peter Singer  
Editor-in-Chief  
*Semiconductor International***



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CONFERENCE**

**SESSION II**

**Wednesday, February 23, 2005  
10:45 A.M. - 12:00 PM**

**VLSI MULTILEVEL INTERCONNECTION  
CMP CONSUMABLES - PART I**

**Chairman:**

**Dr. Ara Philipossian  
UNIVERSITY OF ARIZONA  
Tucson, Arizona**

