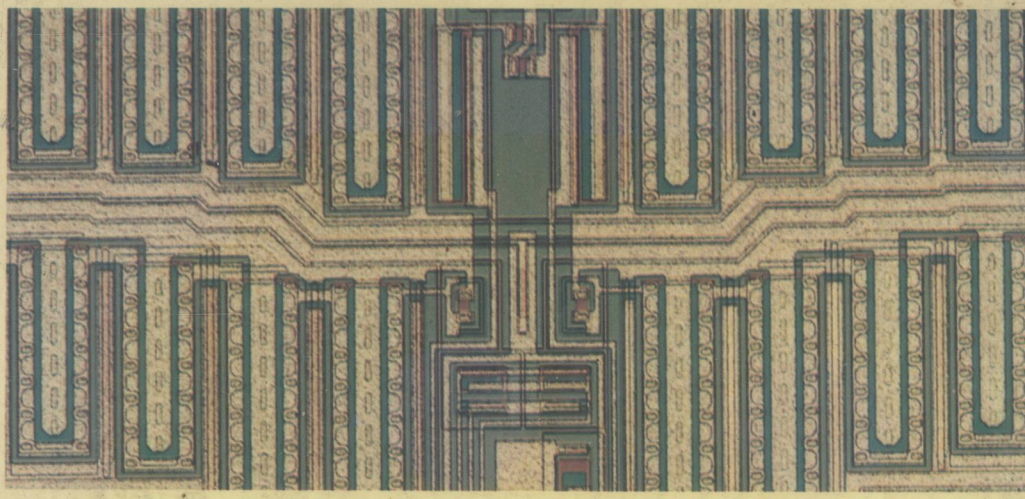
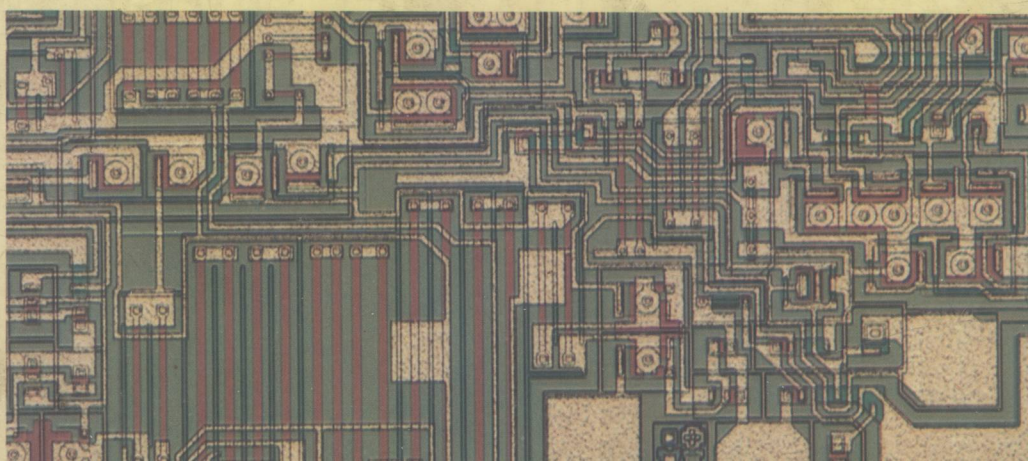


POWER INTEGRATED CIRCUITS

PHYSICS, DESIGN, AND APPLICATIONS

PAOLO ANTOGNETTI
EDITOR



POWER INTEGRATED CIRCUITS: Physics, Design, and Applications

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POWER INTEGRATED CIRCUITS: Physics, Design, and Applications

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Foreword

The economic importance of integrated circuits that perform functions involving large power on-chip power dissipation (power integrated circuit) has grown continually since the first such circuits were implemented in the late 1960s. The realization of low-level analog and digital processing circuitry on the same integrated circuit with power transistors handling large voltages and currents has resulted in the implementation of complete functions such as voltage regulators and audio amplifiers at lower cost than had been the case for discrete power transistor realizations. This growth will continue as improved technology and circuit design techniques allow higher levels of integration to be achieved in these circuits both in terms of their power handling capability and the complexity of the low-level signal-processing circuitry that can be included on the same chip.

The design of power integrated circuits has historically presented a special set of problems to the circuit designer. These problems involve technological, device, circuit, and packaging considerations resulting from the required high levels of voltage, current density, and power density. At the technology level, perhaps the most pervasive problem is the realization of power devices with sufficiently large current-handling capability and voltage capability in the same technology with standard integrated circuit components. A related important problem is the simultaneous implementation of digital circuitry of sufficient density and speed together with high voltage devices.

At the device level, the design of MOS and bipolar power devices that reliably achieve the necessary levels of power dissipation and safe

area of operation while consuming the minimum possible silicon die area is a key problem. The problem of prediction a priori the detailed electrical behavior of a power transistor structure with complex electrical and thermal topology under transient conditions of high voltage, high current, and high level injection is still not fully solved.

At the circuit level, many unique problems present themselves. One is the problem of designing circuitry which protects the circuit from catastrophic failure under worstcase load-fault conditions. A second aspect that is unique to power ICs is the thermal interaction between the devices on the chip which dissipate large power and the low-level analog circuitry on the same chip. This problem can result if grossly degraded performance is not properly considered during the design and layout phase.

Finally, at the packaging level, the development of a physical structure that can be manufactured at low cost, which has a sufficient number of electrical connections, which is capable of conducting sufficient thermal energy from the die with a given maximum allowable temperature drop, and which is compatible with component insertion equipment for low cost of manufacture is a challenging task.

Because of these and other specialized problems, the design of power integrated circuits and devices has evolved into a separate specialty within the field of integrated circuit design. In comparison to the skills required to undertake the design of more conventional integrated circuits, the design of a power integrated circuit requires an understanding of a broader set of physical principles. These include thermodynamics, thermal properties of materials, a detailed understanding of the effects of temperature variations on devices, high-level injection effects in transistors, high-field mobility behavior in silicon, complex electro-thermal interaction phenomena, and so forth.

This book is the first attempt to compile a volume specifically focused on the problems of power integrated circuits. In it, contributions from leading experts in the field have been assembled. The result is a reference work that should be invaluable to those involved in the design of this highly challenging and interesting type of integrated circuit.

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University of California, Berkeley

Preface

As described by P. Gray in his Foreword, this book represents the first attempt to compile a volume specifically focused on power integrated circuits (PIC). After an introductory chapter, which gives an interesting historical perspective, technological problems related to the fabrication process are described, as well as the particular features of power devices. Both types of power devices are considered, bipolar and FET, and their treatment concerns theoretical and practical aspects. Subsequent chapters discuss other important topics, such as packaging, which represents a fundamental part of the design cycle of a PIC, and reliability, which enables the designer and the process engineer to improve the quality of their products. Finally the core of the book focuses on the design and applications of PIC's. General aspects of the design process for power circuits are described first, as opposed to the design of regular, low power IC's. In the second part of the book, five chapters are dedicated to the description of special designs for particular applications, such as audio amplifiers, PIC's for industrial applications, regulators, and interface circuits to the external world.

The book has been edited with contributions from leading experts in the field, from Europe, the United States, and Japan. However, the backbone of the book has been written by authors from the SGS company in Milan, Italy. SGS is generally considered a leader in the field of PIC's. The other authors represent the following companies: Fairchild, Sprague, Siliconix, and NEC. One author is affiliated with Stanford University.

The authors have assumed that the reader is familiar with the basic

aspects of semiconductor devices and processing technology, as well as design criteria for low power IC's. The book is aimed at design engineers and process engineers in semiconductor houses, specialized in the fabrication of power circuits, and at application engineers in system houses, where power electronics is relevant in the design of an electronic system.

Each chapter contains many circuit schematics, die photos, plots and charts. This book will most certainly prove a valuable reference tool for designers in industrial research and application labs. The first part of the book covers in detail theoretical aspects of device physics, both bipolar and FET, and will probably appeal also to graduate students desiring a thorough treatment of power devices.

I would like to extend my gratitude to Dr. P. Pistorio, Chairman of SGS, for his initial and decisive encouragement and support; I would also like to thank Mr. B. Murari of SGS for his enthusiasm in supporting the initial idea of this book, and all the authors for the time spent working on their chapters, mostly taken from their leisure time; in particular I wish to thank two authors, Mr. T. Kikkawa of NEC and Dr. M. Felici, formerly of SGS, for their timeliness and precision.

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Contents

CHAPTER 1

Power Integrated Circuits: An Introduction

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In the 1980s, integrated electronics is dominated by the acronym VLSI (*v*ery *l*arge *s*cale *i*ntegration). Without doubt this is a fascinating subject, and for some time, rapid and continuous development in the field has justified research aimed at identifying the physical limits of the process of integrating micrometric devices.

At the same time there has been an equally significant, though perhaps less visible, development in the field of *power integrated circuits* (PICs). This we can identify, for brevity and for an objective dualism, by the acronym VLAI (*v*ery *l*arge *a*rea *i*ntegration). The meaning that we intend to attribute to this acronym reflects the dimensions of the elementary device (a power transistor) and the dimensions of the resulting integrated circuit. With this the intention is to stress the increase in power density—in terms of both voltage and current—and

in the total number of components included in a power integrated circuit.

Technological advances and circuit and systems development activities involved in the realization of a monolithic electronic power system have now reached a level of maturity that suggests the drafting of a volume that collects the contributions of numerous experts in the field. Such a volume should offer a reasonably complete review of past developments, of the state of the art, and of the emerging prospects in this sector of integrated electronics.

The guideline for development is obviously industrial needs, which can be expressed as reduction in costs, improved performance, and ever-improving reliability. The results achieved demonstrate the continuing interaction between circuits and technologies. This interaction spreads ever more frequently beyond the relatively restricted environment of the semiconductor manufacturer to create new developments in the architecture of electronic systems, which are essential for optimizing the industrial economy offered by the new designs. This confirms, among other things, the decidedly interdisciplinary character of integrated circuit engineering.

Moreover, technological developments in PICs often yield results which are of interest to the world of VLSI, and vice versa. It is the conviction of the authors that the electronic revolution fired by power integrated circuits will also bring results as far-ranging as those obtained so far in the undoubtedly fascinating field of submicrometric devices.

1.1 PRELIMINARIES

PIC engineering can be divided into three parts: semiconductor technology, circuits, and packages. In turn, each part presents a variety of problems which often impinge on other parts. In the semiconductor technology field, for example, the optimization of the most important elementary cell, the power transistor, entails modeling a circuit type such that maximum equalization of current distribution is possible when several elementary transistors are connected in parallel.

In the circuitry field, as we will see, a possible overcurrent protection network configuration exploits a minimum-resistance sensing element obtained by placing two Kelvin contacts on a suitable geometry. In the assembly field, certain operations (finishing of the back of the silicon wafer, for example, or the mechanical die-separation technique) determine the performance of the device and require an extensive knowledge of electrothermic problems.

Electrothermic effects in integrated circuits are known and are gen-

erally controllable with sufficient precision (thermal feedback in an operational amplifier is a typical example), but the fundamental problem in PICs becomes exquisitely thermodynamic, in three dimensions and in a medium anything but homogeneous. The determination of the temperature field in such a system constitutes a formidable problem both from the point of view of numerical analysis and from that of strict experiment.

A determining element in the economy of an integrated circuit is obviously the area of the silicon die. Current and voltage are not equal in their effect on the power density obtainable in an integrated circuit. We will briefly describe here the interrelationship between system application and silicon die area, using bipolar technologies. The current density is determined by the characteristics of the base-emitter junction, i.e., the doping profile in a relatively superficial region; however, the breakdown voltage required by the process is a determinant of the characteristics of the isolation junction and thus affects considerably the surface area of each isolated device. The power required from an integrated circuit often determines the individual voltage or current as a function of the characteristics of the user system so that the choice of technology for the semiconductor manufacturer is obligatory.

Bipolar devices, by definition, depend in their mode of operation on the transport, trapping, and/or recombination of the two types of carriers. Bipolar device operation takes place essentially in the bulk of the semiconductor. Indeed, the most famous member of this category, the bipolar transistor, was invented by Shockley and coworkers to avoid the problems connected with the surface. However, since no devices of infinite or semi-infinite extent exist, regions of transition from one conductivity type to another eventually also arrive at the surface. Thus, surface effects still play a role in the operation of such devices, often a crucial one in determining final IC performance. High-voltage bipolar transistors are, in fact, very complicated structures for both process and geometric design, and a deep knowledge of surface problems is required in order to avoid accidentally creating parasitic MOS devices.

Thus, to produce good PICs certain basic conditions have to be met: the availability of silicon technologies suitable for the integration of high-voltage and high-current devices, the availability of power packages capable of dissipating the heat generated, and the ability to design innovative circuits and systems. Mainly because of this last need, the design of PICs becomes every day less exclusively the domain of the semiconductor manufacturer and involves (already remarkably) the designer of electronic systems, which play a much more essential role than in the recent past.

Several times we have used the term *electronic system* and perhaps,

at this point, it merits a few words of comment. Radios, telephones, television sets, automobiles, and typewriters, for example, are electronic systems in which the most natural division of functions can be illustrated: supply, transduction, processing, and actuation (see Fig. 1-1). In general, each function requires a dedicated technology. The natural application domain of power technologies comprises mainly the supply and the actuation functions. This does not exclude a more or less relevant part of the signal processing function from the power circuit. A recurring example is provided by parallel printer-driver circuits, where serial transmission of the data to be transferred permits a definite economy in the number of pins used but obviously requires a serial-parallel conversion inside the power circuit. Even this relatively simple problem requires new technological performance such as the coexistence of analog and digital functions and the minimization of the area of silicon necessary to implement digital functions at high voltages. A notable example in the bipolar field is provided by high-voltage technologies, which, with minimum process complications, allow the integration of I^2L structures.

Direct interfacing with microprocessors and peripherals and direct driving of actuation systems are a measure, as a function of the total cost, of the excellence of VLAI technology.

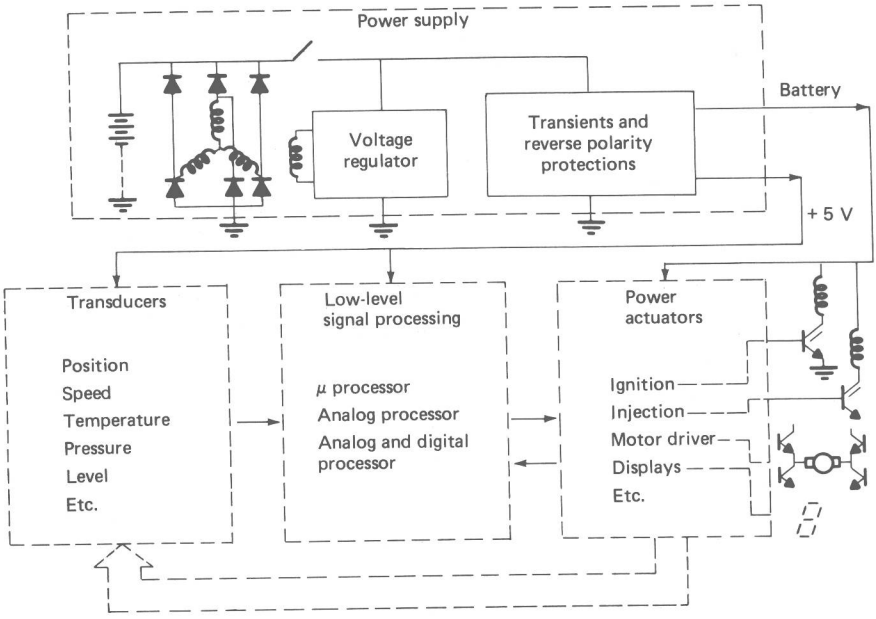

FIG. 1-1 A typical electronic system partition.

1.2 SEMICONDUCTOR TECHNOLOGIES

An important parameter in PIC process design is the maximum voltage that can be impressed on the collector with respect to the emitter (the worst-case situation is circuit operation with a high impedance at the base terminal). The resulting common-emitter breakdown voltage is the lowest expected breakdown configuration resulting from a current-gain multiplication of collector-base junction leakage. The collector avalanche voltage can be limited by several effects, including junction curvature at edges or, worse, at corners; one-dimensional breakdown calculations usually must be modified to take this into account.

The most significant limitation upon nominal *collector-base* junction breakdown voltage *is* one-dimensional in nature and so is directly related to vertical doping profile. If the collector depletion region reaches the n^+ buried layer before the collector-base junction breaks down as a result of another limitation (perhaps junction curvature), the electric field builds up at a higher rate because additional charge depletes at a slower rate. Within this so-called reach-through condition, the limitations arising from diffused-junction isolation or deep n^+ (to lower collector series resistance) can be realized by considering the amount of n^+ buried-layer outdiffusion caused by the large amount of post-epitaxy high-temperature processing. Variation in epitaxial thickness results in a direct variation in the post-epitaxy diffusion length required to reach the substrate and thus in a buried-layer outdiffusion that can consume almost one-half the width of the epitaxial layer.

Ion-implanted depositions allow the isolation and sinker regions to be produced from top and bottom and this results in a consistent reduction of post–epitaxial deposition high-temperature processing. This is one of the most attractive applications of ion implantation in high-voltage processes. It is not the only one. Vertical *pnp* transistors can also be obtained by using selectively placed dual buried layers with implanted boron, which will outdiffuse more rapidly than the antimony host layer. This technique is widely used also in VLSI technologies: I^2L upward operation and the VMOS active channel region give well-known examples.

Thus ion implantation (but also process and device computer-aided design, or CAD) reveals a strong influence in the evolution of PIC processes which is closely related to the corresponding evolution in MOS processes.

Polycrystalline silicon deposition is another technique widely used by bipolar process engineers: device isolation, field-plate surface protection, and deposited resistors are the most important applications in high-voltage technology. Furthermore, it should be remembered that, in order to obtain really effective surface protection, one has also to

prevent thermal-aided gate movement due to oxide charge mobility. Problems of this kind are closely linked to overall IC reliability.

High-current devices for integrated circuits present quite the same design problems as in the case of discrete components; some further complications may arise because of the need to limit device size and to put the collector contact on the front of the chip. Nevertheless, a deep understanding of high-injection effects in bipolar transistor operation (e.g., base widening and current crowding) is required. Emitter efficiency and perimeter-to-area ratio are the most common technological parameters to be optimized, particularly when high-voltage processes are necessary and epitaxial-layer thickness and resistivity cannot be tailored for high-current operation. What is much more difficult to improve, in comparison with discrete devices, is transistor ruggedness against direct and reverse second breakdown failure. To improve direct second breakdown protection while maintaining acceptable device characteristics, a number of emitter "fingers" are used and provisions are made for so-called ballasting resistors in each finger in order to equalize currents and prevent hot spots from occurring. But second breakdown in power transistors will not cease being an actively discussed subject, and likewise in IC applications. What one has to explain, at least from a phenomenological point of view, is a failure that is preceded by a rapid drop in the voltage across the device and a rapid increase in the current.

There are many theories about second breakdown mechanisms and initiation processes, but we still have no unified global approach. Solutions can be applied locally upon further investigation after an a priori choice among contending theories.

Precision and matching of parameters are frequently essential in analog circuits. This is true, for example, of resistor values. Beyond the effects induced by the natural dispersion of process parameters, one of the determining mechanisms is found to be sensitivity to mechanical stresses. As is known, these modify the energy band structure of the semiconductor or modify to a lesser degree the mobility of carriers and their intrinsic concentration. Mechanical stresses arise during both the process phase and the assembly phase. In the first case, everything is traceable to the differing coefficients of thermal expansion of the materials used (silicon, silicon dioxide, silicon nitride, etc.). In the second case, chip soldering techniques and the mechanical deformation of the resin in the polymerization phase prove to be the most critical processes. As far as piezoresistive effects are concerned, in particular, the choice of ⟨100⟩ substrate allows an orientation of the critical layers with minimum sensitivity of stresses. In the first case again, copper, for example, has a thermal expansion coefficient significantly different from that of silicon. When thermal dissipation requirements compel the use