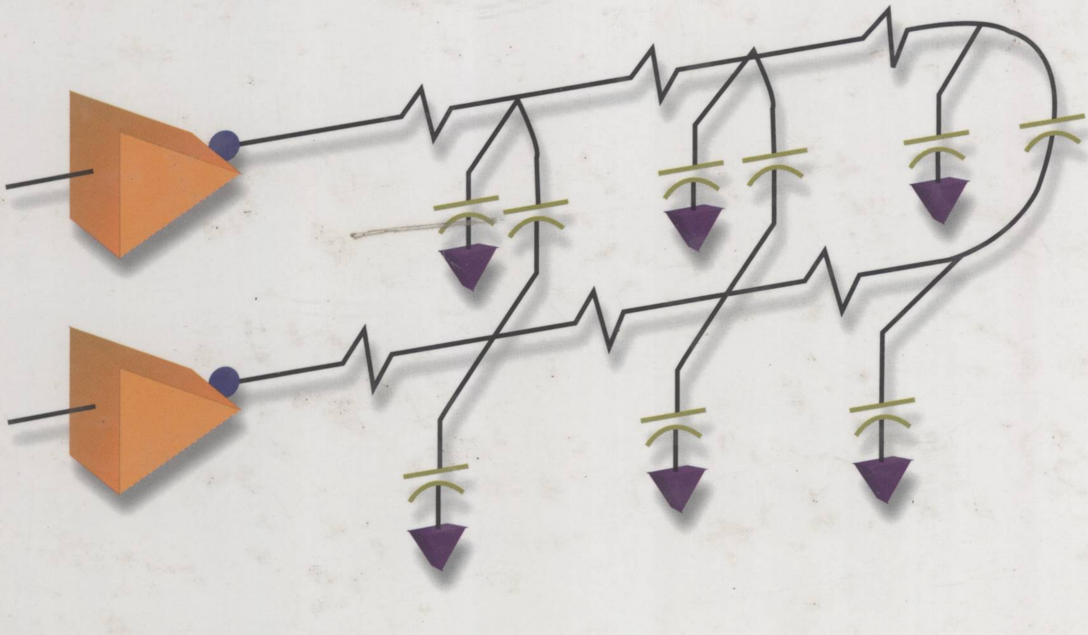
Third Edition

Modern VLSI DESIGN

System-on-Chip Design



Wayne Wolf

Prentice Hall Modern Semiconductor Design Series

Modern VLSI Design

System-on-Chip Design

Third Edition

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PH
PTR

Prentice Hall PTR
Upper Saddle River, NJ 07458
www.phptr.com

ISBN 0-13-061970-1
90000
9 790130 619708

Library of Congress Cataloging-in-Publication Data

A CIP catalog record for this book can be obtained from the Library of Congress.

Editorial/production supervision: *Patti Guerrieri*
Acquisitions editor: *Bernard Goodwin*
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Prentice-Hall, Inc.
Upper Saddle River, NJ 07458

Illustrated and typeset by the author. This book was typeset using FrameMaker. Illustrations were drawn using Adobe Illustrator, with layout plots generated by cif2ps.

Photo credits: Example 1-1: Intel Corporation; Figure 2-2: IBM; Figure 2-5: Agere; Figure 2-15: UMC; Figure 2-16: IBM; Figure 6-1: Hewlett-Packard Company; Example 7-1: Tom Way, IBM Microelectronics, Essex Junction, VT; Figure 7-19: Wayne Wolf; Figure 7-20: Wayne Wolf and IBM; Example 8-4: Philips.

Second edition published under the title *Modern VLSI Design: Systems on Silicon.*

Printed in the United States of America
10 9 8 7 6 5 4 3 2

ISBN 0-13-061970-1

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Pearson Education Australia PTY, Limited
Pearson Education Singapore, Pte. Ltd.
Pearson Education North Asia Ltd.
Pearson Education Canada, Ltd.
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for Nancy (as always)

Preface to the Third Edition

This third edition of *Modern VLSI Design* includes both incremental refinements and new topics. All these changes are designed to help keep up with the fast pace of advancements in VLSI technology and design.

The incremental refinements in the book include improvements in the discussion of low power design, the chip project, and the lexicon. Low power design was discussed in the second edition, but has become even more complex due to the higher leakages found at smaller transistor sizes. The PDP-8 used in previous editions has been replaced with a more modern data path design. Designing a complete computer is beyond the scope of most VLSI courses, but a data path makes a good class project. I have also tried to make the lexicon a more comprehensive guide to the terms in the book.

This edition shows more major improvements to the discussions of interconnect and hardware description languages. Interconnect has become increasingly important over the past few years, with interconnect delays often dominating total delay. I decided it was time to fully embrace the importance of interconnect, especially with the advent of copper interconnect. This third edition now talks more thoroughly about interconnect models, crosstalk, and interconnect-centric logic design.

The third editon also incorporates a much more thorough discussion of hardware description languages. Chapter 8, which describes architectural design, now introduces VHDL and Verilog as the major hardware description languages. Though these sections are not meant to be thorough manuals for these languages, they should provide enough information for the reader to understand the major concepts of the languages and to be able to read design examples in those languages.

As with the second edition, you can find additional helpful material on the World Wide Web at http://www.ee.princeton.edu/~wolf/modern-vlsi. This site includes overheads useful either for teaching or for self-paced learning. The site also includes supplementary materials, such as layouts and HDL descriptions. Instructors may request a book of answers to the problems in the book by calling Prentice Hall directly.

I'd like to thank Al Casavant and Ken Shepard for their advice on interconnect analysis and Joerg Henkel for his advice on low power design. I'd also like to thank Fred Rosenberger for his many helpful comments on the book. As always, any mistakes are mine.

Wayne Wolf

Princeton, New Jersey

Preface to the Second Edition

Every chapter in this second edition of *Modern VLSI Design* has been updated to reflect the challenges looming in VLSI system design. Today's VLSI design projects are, in many cases, mega-chips which not only contain tens (and soon hundreds) of millions of transistors, but must also run at very high frequencies. As a result, I have emphasized circuit design in a number of ways: the fabrication chapter spends much more time on transistor characteristics; the chapter on gate design covers a wider variety of gate designs; the combinational logic chapter enhances the description of interconnect delay and adds an important new section on crosstalk; the sequential logic chapter covers clock period determination more thoroughly; the subsystems chapter gives much more detailed descriptions of both multiplication and RAM design; the floorplanning chapter spends much more time on clock distribution.

Beyond being large and fast, modern VLSI systems must frequently be designed for low power consumption. Low-power design is of course critical for battery-operated devices, but the sheer size of these VLSI systems means that excessive power consumption can lead to heat problems. Like testing, low-power design cuts across all levels of abstraction, and you will find new sections on low power throughout the book.

The reader familiar with the first edition of this book will notice that the combinational logic material formerly covered in one chapter (Chapter 3) has been split into two chapters, one of logic gates and another on combinational networks. This split was the result of the great amount of material added on circuit design added to the early chapters of the book. Other, smaller rearrangements have also been made in the book, hopefully aiding clarity.

You can find additional helpful material on the World Wide Web at http://www.ee.princeton.edu/~wolf/modern-vlsi. This site includes overheads useful either for teaching or for self-paced learning. The site also includes supplementary materials, such as layouts and VHDL descriptions. Instructors may request a book of answers to the problems in the book by calling Prentice Hall directly.

I would especially like to thank Derek Beatty, Luc Claesen, John Darringer, Srinivas Devadas, Santanu Dutta, Michaela Guiney, Alex Ishii, Steve Lin, Rob Mathews, Cherrice Traver, and Steve Trimberger for their comments and suggestions on this second edition.

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Preface

This book was written in the belief that VLSI design is *system* design. Designing fast inverters is fun, but designing a high-performance, cost-effective integrated circuit demands knowledge of all aspects of digital design, from application algorithms to fabrication and packaging. Carver Mead and Lynn Conway dubbed this approach the tall-thin designer approach. Today's hot designer is a little fatter than his or her 1979 ancestor, since we now know a lot more about VLSI design than we did when Mead and Conway first spoke. But the same principle applies: you must be well-versed in both high-level and low-level design skills to make the most of your design opportunities.

Since VLSI has moved from an exotic, expensive curiosity to an everyday necessity, universities have refocused their VLSI design classes away from circuit design and toward advanced logic and system design. Studying VLSI design as a system design discipline requires such a class to consider a somewhat different set of areas than does the study of circuit design. Topics such as ALU and multiplexer design or advanced clocking strategies used to be discussed using TTL and board-level components, with only occasional nods toward VLSI implementations of very large components. However, the push toward higher levels of integration means that most advanced logic design projects will be designed for integrated circuit implementation.

I have tried to include in this book the range of topics required to grow and train today's tall, moderately-chubby IC designer. Traditional logic design topics, such as adders and state machines, are balanced on the one hand by discussions of circuits and layout techniques and on the other hand by the architectural choices implied by scheduling and allocation. Very large ICs are sufficiently complex that we can't tackle them using circuit design techniques alone; the top-notch designer must understand enough about architecture and logic design to know which parts of the circuit and layout require close attention. The integration of system-level design techniques, such as scheduling, with the more traditional logic design topics is essential for a full understanding of VLSI-size systems.

In an effort to systematically cover all the problems encountered while designing digital systems in VLSI, I have organized the material in this book relatively bottom-up, from fabrication to architecture. Though I am a strong fan of top-down design, the technological limitations which drive architecture are best learned starting with fabrication and layout. You can't expect to fully appreciate all the nuances of why a particular design step is formulated in a certain way until you have completed a chip design yourself, but referring to the steps as you proceed on your own chip design should help guide you. As a result of the bottom-up organization, some topics may be broken up in unexpected ways. For example, placement and routing are not treated as a single subject, but separately at each level of abstraction: transistor, cell, and floor plan. In many instances I purposely tried to juxtapose topics in unexpected ways to encourage new ways of thinking about their interrelationships.

This book is designed to emphasize several topics that are essential to the practice of VLSI design as a system design discipline:

- **A systematic design methodology reaching from circuits to architecture.** Modern logic design includes more than the traditional topics of adder design and two-level minimization—register-transfer design, scheduling, and allocation are all essential tools for the design of complex digital systems. Circuit and layout design tell us which logic and architectural designs make the most sense for CMOS VLSI.
- **Emphasis on top-down design starting from high-level models**. While no high-performance chip can be designed completely top-down, it is excellent discipline to start from a complete (hopefully executable) description of what the chip is to do; a number of experts estimate that half the application-specific ICs designed execute their delivery tests but don't work in their target system because the designer didn't work from a complete specification.
- **Testing and design-for-testability.** Today's customers demand both high quality and short design turnaround. Every designer must understand how chips are tested and what makes them hard to test. Relatively small changes to the architecture can make a chip drastically easier to test, while a poorly designed architecture cannot be adequately tested by even the best testing engineer.
- **Design algorithms**. We must use analysis and synthesis tools to design almost any type of chip: large chips, to be able to complete them at all; relatively small ASICs, to meet performance and time-to-market goals. Making the best use of those tools requires understanding how the tools work and exactly what design problem they are intended to solve.

The design methodologies described in this book make heavy use of computer-aided design (CAD) tools of all varieties: synthesis and analysis; layout, circuit, logic, and architecture design. CAD is more than a collection of programs. CAD is a way of thinking, a way of life, like Zen. CAD's greatest contribution to design is breaking the process up into manageable steps. That is a conceptual advance you can apply with no computer in sight. A designer can—and should—formulate a narrow problem and apply well-understood methods to solve that problem. Whether the designer uses CAD tools or solves the problem by hand is much less important than the fact that the chip design isn't a jumble of vaguely competing concerns but a well-understood set of tasks.

I have explicitly avoided talking about the operation of particular CAD tools. Different people have different tools available to them and a textbook should not be a user's guide. More importantly, the details of how a particular program works are a diversion—what counts is the underlying problem formulations used to define the problem and the algorithms used to solve them. Many CAD algorithms are relatively intuitive and I have tried to walk through examples to show how you can think like a CAD algorithm. Some of the less intuitive CAD algorithms have been relegated to a separate chapter; understanding these algorithms helps explain what the tool does, but isn't directly important to manual design.

Both the practicing professional and the advanced undergraduate or graduate student should benefit from this book. Students will probably undertake their most complex logic design project to date in a VLSI class. For a student, the most rewarding aspect of a VLSI design class is to put together previously-learned basics on circuit, logic, and architecture design to understand the tradeoffs between the different levels of abstraction. Professionals who either practice VLSI design or develop VLSI CAD tools can use this book to brush up on parts of the design process with which they have less-frequent involvement. Doing a truly good job of each step of design requires a solid understanding of the big picture.

A number of people have improved this book through their criticism. The students of COS/ELE 420 at Princeton University have been both patient and enthusiastic. Profs. C.-K. Cheng, Andrea La Paugh, Miriam Leeser, and John "Wild Man" Nestor all used drafts in their classes and gave me valuable feedback. Profs. Giovanni De Micheli, Steven Johnson, Sharad Malik, Robert Rutenbar, and James Sturm also gave me detailed and important advice after struggling through early drafts. Profs. Malik and Niraj Jha also patiently answered my questions about the literature. Any errors in this book are, of course, my own.

Thanks to Dr. Mark Pinto and David Boulin of AT&T for the transistor cross section photo and to Chong Hao and Dr. Michael Tong of AT&T for the ASIC photo. Dr. Robert Mathews, formerly of Stanford University and now of Performance Processors, indoctrinated me in pedagogical methods for VLSI design from an impressionable age. John Redford of DEC supplied many of the colorful terms in the lexicon.

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