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1978 MIDCON Technical Sessions

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Single-Chip Microcomputers—Distributed and Multiprocessing Techniques

1978 Midcon Professional Program

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SINGLE-CHIP MICROCOMPUTERS-- DISTRIBUTED AND MULTI-PROCESSING TECHNIQUES

SESSION ORGANIZER AND CHAIRMAN

Jim Vittera
Mostek Corp.
Carrollton, Tx.

MULTI-MICROCOMPUTER AND DISTRIBUTED ARCHITECTURE SYSTEMS WITH THE MC6801 SINGLE CHIP MICROCOMPUTER

By
Mike Wiles and Fuad Musa
Motorola Inc., Integrated Circuit Division
Austin, Texas

INTRODUCTION

The MC6801 represents the state-of-the art in single-chip microcomputers with the primary objective of reducing system cost by utilizing advances in VLSI, scaled NMOS process technology. The silicon implementation of the MC6801 is equivalent to eight LSI 6800 family chips--see Figure 1. It comprises in a single 40-pin package a complete monolithic microcomputer function: CPU (8-bit), ROM (2K-byte), RAM (128-bytes of which 64-bytes can be retained under power-down conditions), four Parallel I/O Ports (31 pins), a Serial Communications Port, a multipurpose Timer (16-bit), and a Clock. The single most noteworthy accomplishment of the MC6801 is probably the system's integration of these components into a powerful single-chip microcomputer.

SOFTWARE INNOVATIONS

The MC6801 CPU is object-code compatible with the MC6800. In addition, significant improvements and additions have been incorporated. The MC6800 programmer will feel very much at ease with the MC6801 instruction set. All of the MC6800 instructions are implemented. In addition several new and powerful instructions have been added. which make the MC6801 capable of handling 16-bit arithmetic operations. The A-and B-accumulators have been concatenated into a single 16-bit accumulator "D", (see programming model shown

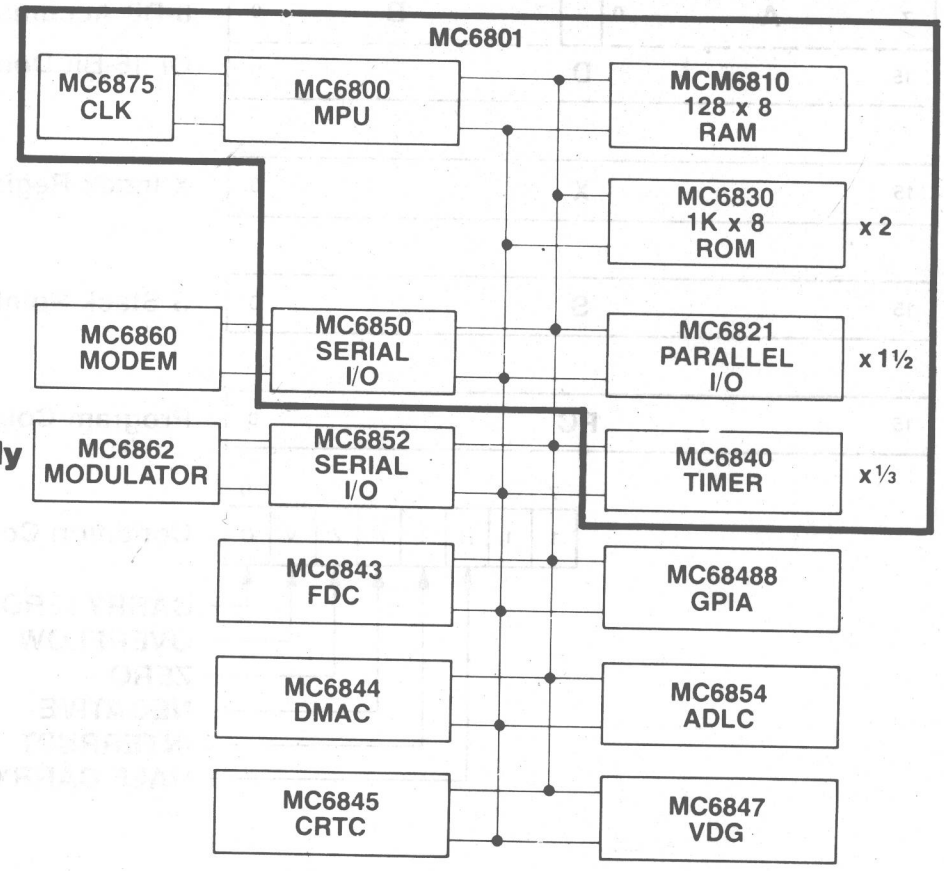

FIGURE 1

MC6801 Single-Chip Microcomputer Family

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in Figure 2), for which a full set of 16-bit arithmetic instructions have been added. These include: Load, Store, Add, Subtract, Shift Left and Shift Right. These new double accumulator instructions have been implemented with all of the addressing modes available for the MC6800-single-accumulator instructions.

Indexing has been greatly enhanced by adding three key new instructions: Add B to X, Push X, and Pull X.

A fast hardware multiply instruction was also added (A times B with the result placed in A:B).

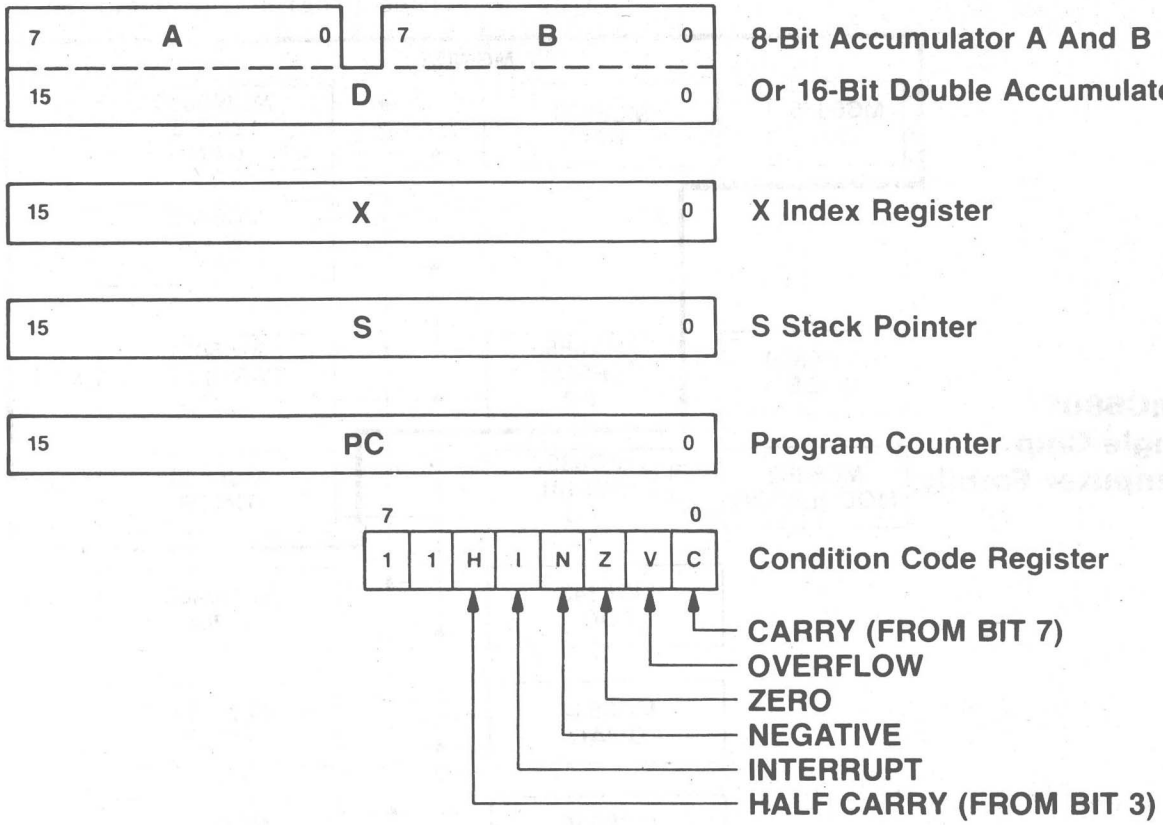
Further CPU improvements involve reduced execution cycles for certain key instructions: all stores (-1), all branches (-1), all indexed (-1), BSR (-2), JSR (-2 Ind., -3 Ext.), INS and INX (-1), DES and DEX (-1), PSHA and PSHB (-1), TSX and TXS (-1).

FEATURES

The MC6801 has been designed with sufficient flexibility and power to deal with an extremely wide and vastly different variety of applications extending into the 1980's. Emphasis was placed on minimization of system part count, and making increasing use of distributed and multi-processing. The compatibility with the 6800 family and the consistent method of systems integration will serve to minimize the new skills which must be mastered by the user.

The MC6801 is designed with two mask options. In the first option-designated MC6801-the clocks are generated on the chip with the frequency source being either a crystal-controlled oscillator or a simple TTL input, of a frequency equal to 4x system clock frequency. The clock outputs are E (system clock) and AS (address strobe). The

FIGURE 2 **MC6801 Programming Model**



latter is used to latch the high-byte of address in the expanded-multiplexed-mode of operation. In the second Mask option-designated MC6801E-both E and AS are generated externally and are supplied to the chip.

Modes of Operation

Both MC6801 and MC6801E have three basic modes of operation: single-chip, expanded-non-multiplexed, and expanded-multiplexed modes (see Figure 3). These modes are selected by programming I/O Port #2 while in the RESET condition.

In the single-chip-mode, the MC6801 is a powerful microcomputer (see Figure 4) which can be configured either as a master or a slave. Communication between the master and the slave is achieved via the handshake capability provided on I/O Port #3 (see Figure 5). The MC6801E is configured in the single-chip mode as an intelligent peripheral controller which interfaces directly to the MC6800 bus. In this configuration I/O Port #3 can be addressed, read from, or written to by another MPU (MC6800, MC6802, MC6801, or MC6809).

In the other two-modes of operation, both MC6801 and MC6801E perform nearly the same function. Figure 6 shows a system configured for operation with the MC6801 in the expanded non-multiplexed mode. This configuration allows standard MC6800 I/O devices (MC6820, MC6821, MC68488, MC6854...etc) to be placed on the expanded bus without the need for any external address latches. Two hundred and fifty six external memory locations (hex locations 0100 thru 01FF) can be addressed as shown in the memory map of Figure 7. Data is output via I/O Port #3, and the low byte of address is output via I/O Port #4.

Figure 8 shows a system configured for operation with the MC6801 in the expanded multiplexed mode. In this configuration the MC6801 is expandable to the full 65K-byte address space of the MC6800. In this mode, data (DØ thru D7) and the low byte of address (AØ thru A7) are multiplexed and output via I/O Port #3 as shown in the basic block diagram of Figure 9. The high byte of address is output via I/O Port #4. However, if the address requirements are less than 65K-bytes, any number of the address bits A8 thru A15 can be configured via software as input I/O pins.

Inputs/Outputs

As shown in Figure 9, the MC6801 contains four I/O Ports. Each port has its own data direction register and input/output latches. Each I/O bit is bi-directional and software programmable.

Port #1 is a parallel byte I/O port similar to an MC6821 PIA (B-side).

Port #2 is basically a 5-bit port similar to side A of the MC6821. Also, this port can be structured via software to serve the input and output functions of the Timer and the Serial Communication Port as well as an external input clock for baud-rate generation.

Port #3 is a parallel byte I/O port with load drive capability of one TTL and 130 pf. This port has a control and status register as well as two handshake control signals (input strobe $\overline{IS3}$ and output strobe $\overline{OS3}$) to allow communication between processors as will be described later.

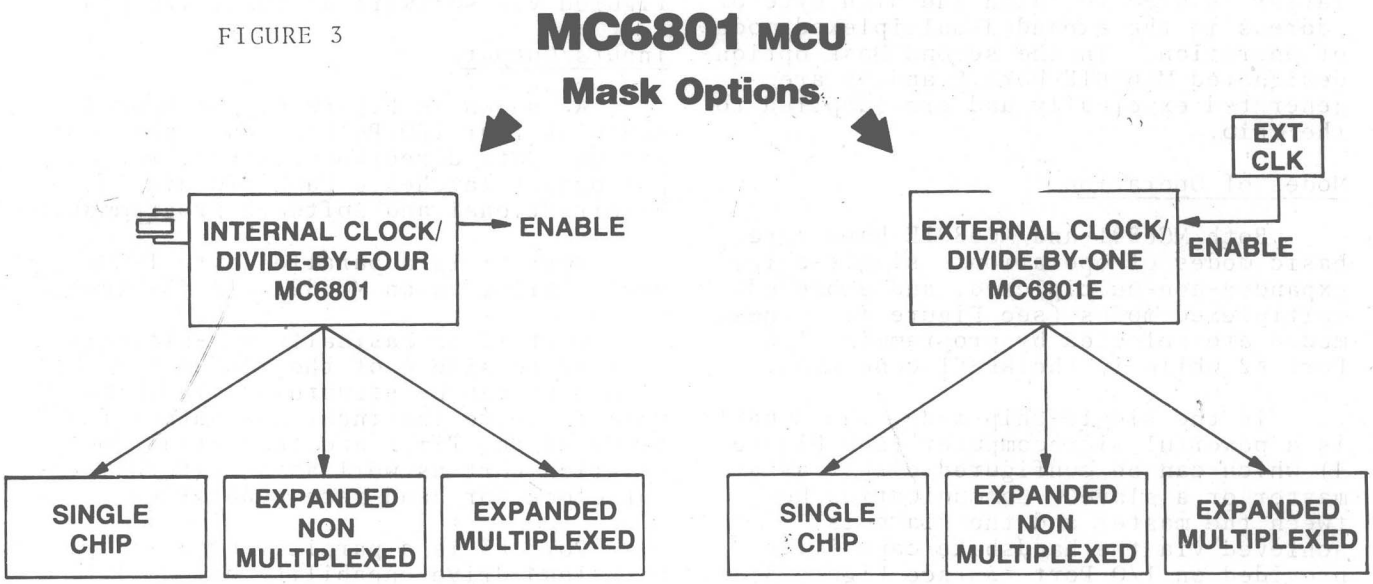
Port #4 is also a parallel byte oriented I/O port with a load drive capability of one TTL and 90 pf.

Timer

The MC6801 contains an on-chip programmable timer which can be accessed through I/O Port #2. As shown in the block diagram of Figure 10, the Timer consists of a 16 bit free running counter (driven by the MPU E clock) plus an overflow bit, a 16-bit input capture register, a 16-bit output compare register, and an 8-bit control/status register.

The counter value can be read by the MPU software at anytime. Thus, the timer can be used to perform measurement on an input waveform such as pulse width or frequency measurements while simultaneously and independently generating an output waveform--pulse width generation. Pulse widths for both input and output waveforms may vary from a few microseconds -- the minimum width is restricted by software -- to several seconds with an accuracy of 2 μsec at a bus clock rate of 1MHz.

FIGURE 3



MC6801
Single Chip Mode

FIGURE 4

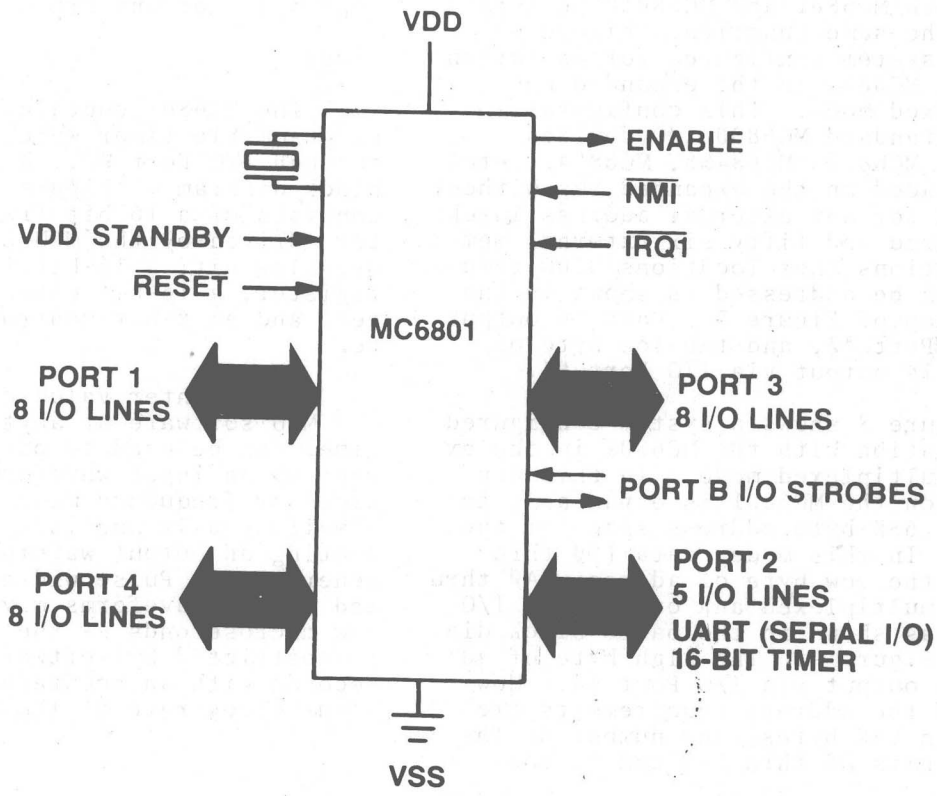


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FIGURE 5

MC6801 Single Chip
Dual Processor Configuration
PARALLEL I/O INTERFACE

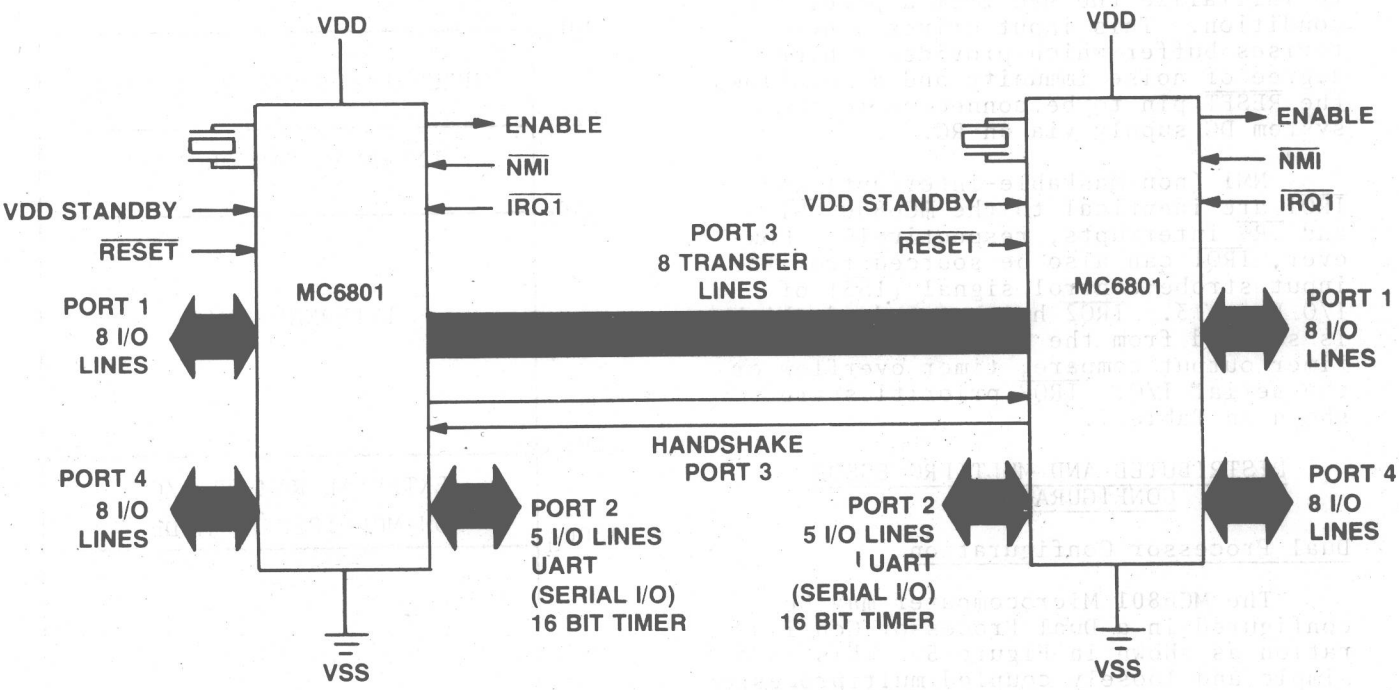

FIGURE 6

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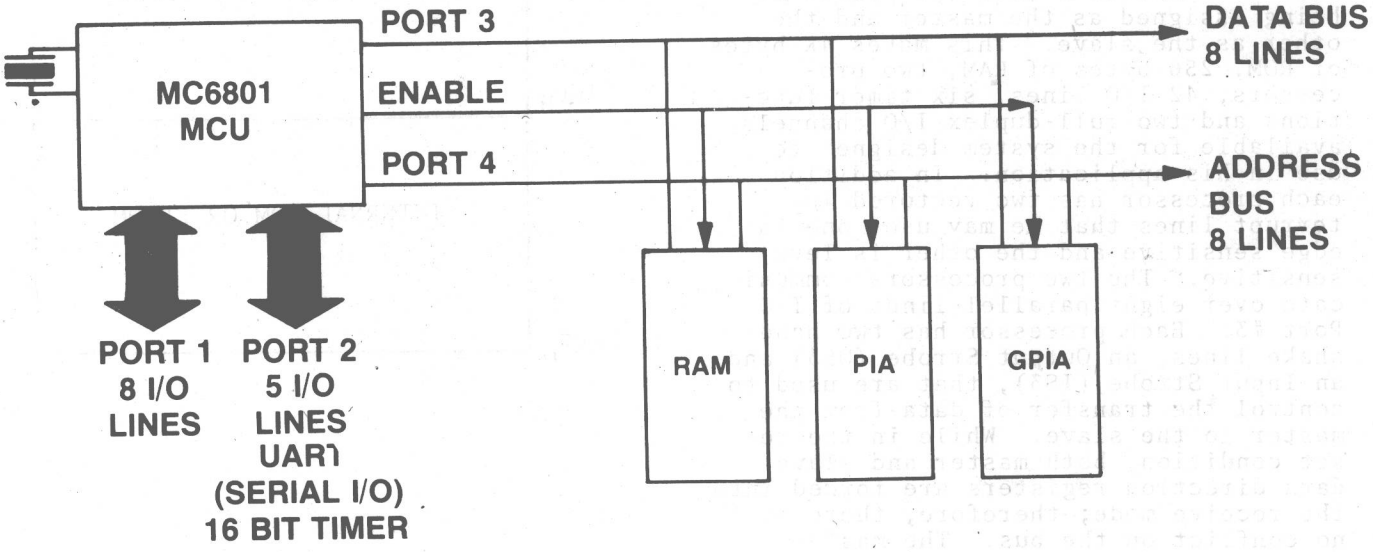
MC6801
Expanded Non-MUX'ed Configuration



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Interrupts

The MC6801 has eight prioritized vectored interrupts including reset. Table I lists these interrupts and their order of priority as well as their vectored addresses. The interrupt structure of the MC6801 is very similar to that of the MC6800. $\overline{\text{RESET}}$ is used to initialize the MPU from a power down condition. This input drives a hysterises buffer which provides a high degree of noise immunity and also allows the $\overline{\text{RESET}}$ pin to be connected to the system DC supply via an RC.

$\overline{\text{NMI}}$ (non-maskable-interrupt) and $\overline{\text{IRQ1}}$ are identical to the MC6800 $\overline{\text{NMI}}$ and $\overline{\text{IRQ}}$ interrupts, respectively. However, $\overline{\text{IRQ1}}$ can also be sourced from the input strobe control signal ($\overline{\text{IS3}}$) of I/O Port #3. $\overline{\text{IRQ2}}$ has been added which is sourced from the timer input capture, timer output compare, timer overflow or the serial I/O. $\overline{\text{IRQ2}}$ priorities are shown in Table I.

DISTRIBUTED AND MULTIPROCESSOR CONFIGURATIONS

Dual Processor Configuration

The MC6801 Microcomputer may be configured in a Dual Processor Configuration as shown in Figure 5. This is a simple and loosely coupled multiprocessor configuration since the memory of each processor is not addressable by the other. The advantages of this configuration is that the task may be broken up into two functions with one processor being assigned as the master and the other as the slave. This makes 4K bytes of ROM, 256 bytes of RAM, two processors, 42 I/O lines, six timer functions and two full-duplex I/O channels available for the system designer to use in his application. In addition each processor has two vectored interrupt lines that he may use, one is edge sensitive and the other is level sensitive. The two processors communicate over eight parallel lines of I/O Port #3. Each processor has two handshake lines, an Output Strobe (OS3) and an Input Strobe (IS3), that are used to control the transfer of data from the master to the slave. While in the reset condition, both master and slave data direction registers are forced into the receive mode; therefore, there is no conflict on the bus. The master

FIGURE 7

MC6801 MEMORY MAP

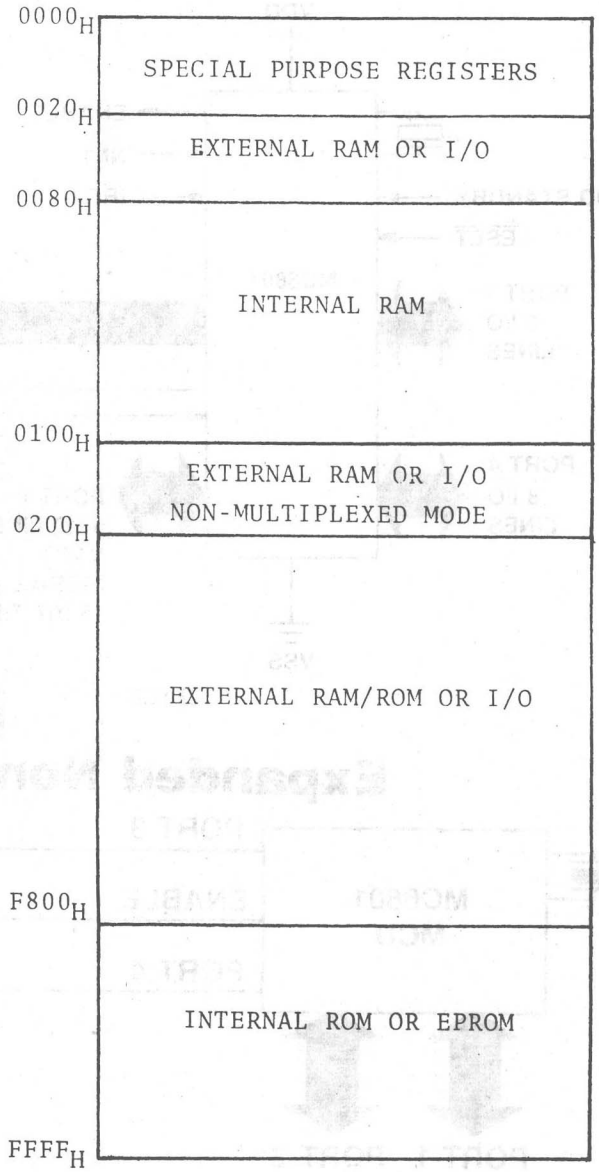


FIGURE 8

MC6801 MCU
Expanded Multiplexed Configuration

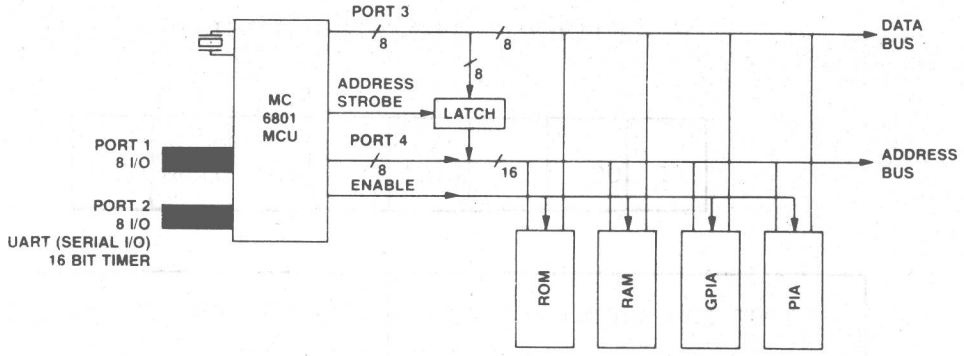


FIGURE 9

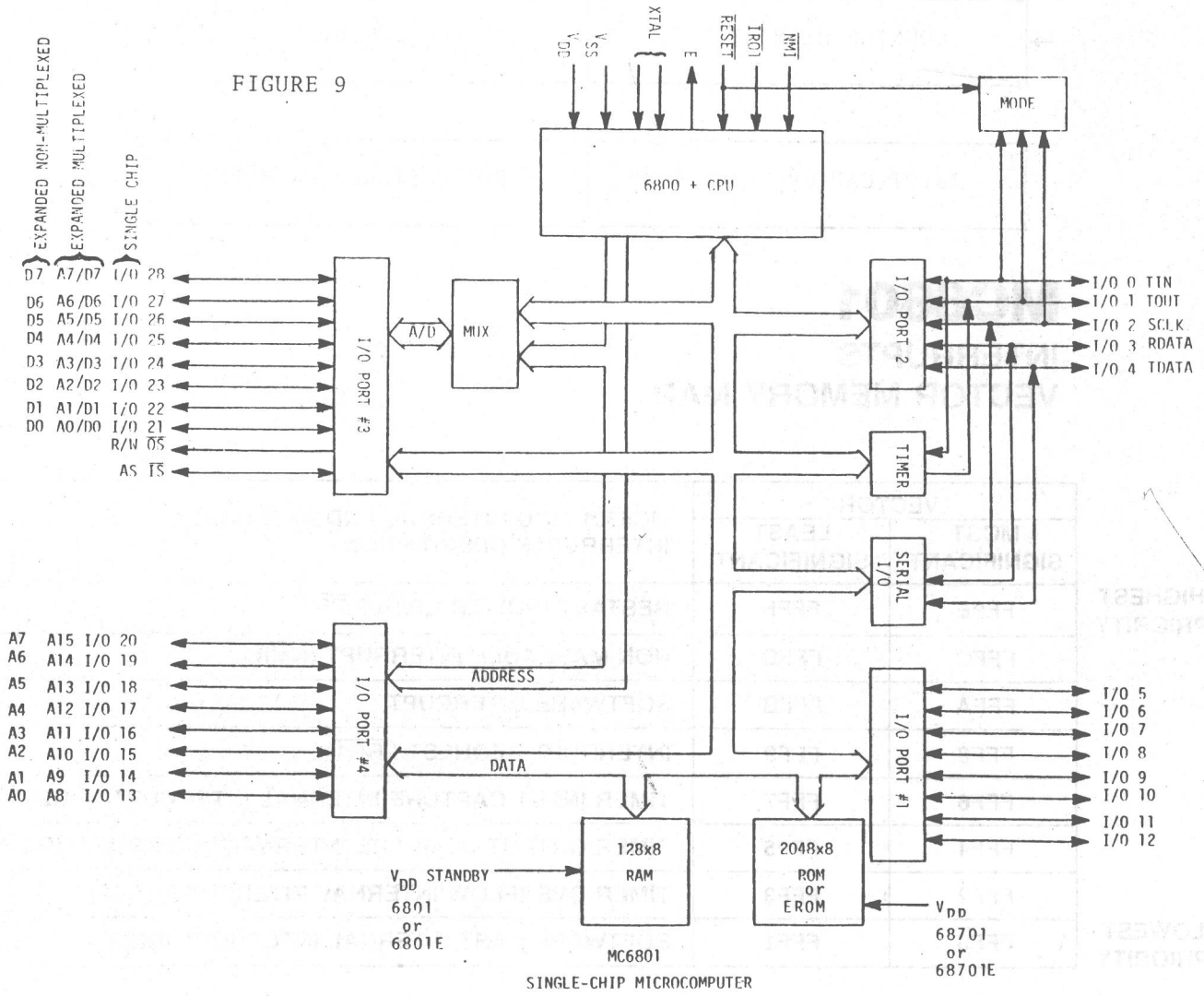
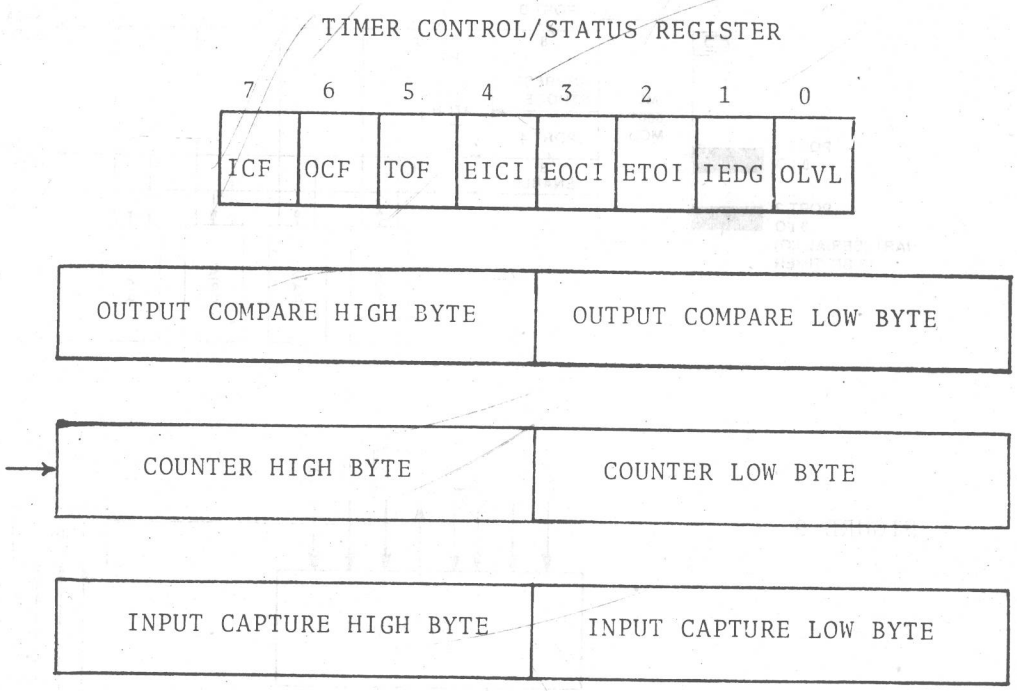


FIGURE 10

TIMER BLOCK DIAGRAM



MC6801

INTERRUPTS VECTOR MEMORY MAP

TABLE I

	VECTOR		MC6801 MCU INTERNAL AND EXTERNAL INTERRUPTS DESCRIPTION
	MOST SIGNIFICANT	LEAST SIGNIFICANT	
HIGHEST PRIORITY	FFFE	FFFF	RESTART (POWER UP/$\overline{\text{RESET}}$)
	FFFC	FFFD	NON-MASKABLE INTERRUPT ($\overline{\text{NMI}}$)
	FFFA	FFFB	SOFTWARE INTERRUPT
	FFF8	FFF9	INTERRUPT REQUEST ($\overline{\text{IRQ1}}$)
	FFF6	FFF7	TIMER INPUT CAPTURE INTERNAL INTERRUPT (IRQ2)
	FFF4	FFF5	TIMER OUTPUT COMPARE INTERNAL INTERRUPT (IRQ2)
	FFF2	FFF3	TIMER OVERFLOW INTERNAL INTERRUPT (IRQ2)
LOWEST PRIORITY	FFF0	FFF1	SOFTWARE UART INTERNAL INTERRUPT (IRQ2)

then configures his data direction register as a transmitter, giving him control of the I/O bus. To transfer a character to the slave a simple write to I/O Port #3 will generate an output strobe signal which latches the data from the master into the slave and sets the IS3 Flag indicating to the slave that data is ready. This IS3 Flag may also be used to generate an interrupt that tells the slave MPU that data is ready. When the data register is ready, it generates a handshake response back to the master indicating that data has been taken. For the slave to transfer data back to the master the I/O bus must be turned around so that the slave is transmitting and the master is receiving. This is accomplished by changing I/O Port #3 Data Direction Register in each MC6801. The Data Direction Registers may be configured by using a software protocol between the Master and Slave identifying whether data is being transmitted or received. An alternate approach, for fast turnaround, would use two hardware lines between the Master and the Slave, one being a Bus Request generated by the Slave and the other a Bus Grant generated by the Master. This would give the Slave the ability to take control of the I/O bus very rapidly.

Thus this configuration using parallel I/O Interface is a simple yet powerful means of inter-processor communication.

Another Dual Processor configuration using a full-duplex serial I/O interface may be configured with the MC6801 as shown in Figure 11. In this system, two MC6801 processors can communicate serially via the full-duplex serial I/O ports without the need for handshake-control, bus request, or bus-grant lines. This configuration is attractive in an I/O intensive system since it provides for 58 parallel I/O lines in addition to the serial ports. All hardware necessary for serial to parallel conversion is implemented on chip as well as all interrupts. Data can be transferred serially at a maximum bit rate of 76.8K bits/sec in each direction.

Distributed Processor Configuration

The MC6801 Microcomputer Unit may be configured into a Distributed Processor system as shown in Figure 12. This configuration takes advantage of the serial I/O port of the MC6801. The user has the ability to configure the serial I/O to be either full-duplex or half-duplex. The MC6801 also provides two programmable formats: the first is the industry standard mark/space (NRZ) used typically with modems or terminals, and the second is a self-clocking bi-phase format intended primarily for use between processors. Both serial I/O formats begin with a start bit (always "0") and end with a stop bit (always "1"). The standard mark/space (NRZ) format results in the assertion of a level corresponding to the bit value for each bit time. The bi-phase format, also called Bi-Phase-M, FM, F/2F, and Manchester, requires a transition of either direction at every bit time and an additional transition at the half-bit time of every bit with a value of 1. This bi-phase format can tolerate a greater difference in transmit receive oscillator frequencies than can NRZ.

The serial I/O is implemented in hardware which results in a very efficient means of communication between processors and also makes an efficient use of the parallel I/O pins of the MC6801 microcomputer. With the hardware implementation, the user's job of designing a distributed processor hardware system is simplified since he only has to decide whether he wants full-duplex or half-duplex, and whether he wants to use NRZ or Bi-Phase.

The main task facing the system designer is the determination of software protocol and the allocation of system time and hardware resources. The software protocol usually includes a destination address in the initial bytes of the message. In order to permit non-selected microcomputers to ignore the remainder of the message, a special "wake-up" feature is included whereby further interrupts may optionally be inhibited until the beginning of the next message. When the next

message appears, the hardware re-enables itself or "wakes-up" the interrupt processing for the next message. This results in a more efficient use of each individual microcomputer, especially where a large number of microcomputers may be connected on the same communication channel. The distributed processor configuration of the MC6801 microcomputer, thus, provides the user flexible alternatives for solving system problems.

Peripheral Processor Configuration

The MC6801E Microcomputer may be configured as a slave peripheral processor as shown in Figure 13. In this configuration the MC6801E is used in the single-chip mode. I/O Port #3 is used to interface the MC6801E to the master processor bus. This frees I/O Ports #1, 2 and 4 to interface the peripheral processor to the device being controlled (such as a matrix printer or a smart data-link controller).

I/O Port #3 contains data-in, data-out, and control registers to interface the Slave to the Master. During reset, the control register if the MC6801E is initialized thus giving control of the interface to the Master. The Master regulates the transfer of data in either direction between the Master and the Slave via the R/W control which is input to the Slave. The Master, therefore, either reads from the data-out register or writes to the data-in register. The MC6801E also has the capability to read from or write to the data registers from its own internal bus. Figure 14 shows the configuration of I/O Port #3 data and control registers. Each processor has the capability to generate interrupts indicating whether data is ready or taken. The interrupts are generated by a write or read to the data registers, the interrupt being selected by the IRQ Flag Select. The IRQ ENABLE bit, however, allows each processor to mask interrupts if desired. The Communication Request/Grant Bit (COMM R/G) is used by the slave to ask to become a talker on the bus and by the master to grant the request.

CONCLUSION

The MC6801 Single Chip Microcomputer and the MC6801E Peripheral Processor provide the system designer with flexible system building blocks that may be used to configure stand alone microcomputers, distributed microcomputer systems and master/slave microcomputer configurations.

FIGURE 11 **MC6801**
Single Chip
Dual Processor Configuration
FULL DUPLEX INTERFACE