CIRCUITS AND SOFTWARE FOR ELECTRONICS ENGINEERS

Edited by Howard Bierman,
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CIRCUITS & SOFTWARE FOR ELECTRONICS ENGINEERS

PREFACE

□ Growth and change are two characteristics long associated with the electronics industry. As applications of ever more sophisticated integrated circuits and other solid-state devices extend farther into such markets as appliances, photography, automobiles, and home entertainment, the electronics engineer is faced with a growing challenge to innovate and develop more advanced products with higher performance and quality.

The task is awesome, but this volume of novel circuits and software should help. It is a collection of the creative solutions developed by readers of *Electronics* for specific design problems and offered for public consumption in Designers' Casebooks and Software Notebooks from mid-1980 through the end of 1982. Over 300 pages of thought-provoking ideas contain speedy answers for short-term projects and stimulating new wrinkles for long-term programs. □

CONTENTS

I. AMPLIFIERS

II. AUDIO CIRCUITS

III. CLOCK CIRCUITS

IV. COMPARATORS

V. CONTROL CIRCUITS

VI. CONVERTERS

VII. ENCODERS/DECODERS

VIII. FILTERS

IX. FUNCTION GENERATORS

X. INSTRUMENT CIRCUITS

XI. LOGIC CIRCUITS

XII. MEMORY CIRCUITS

XIII. MICROPROCESSORS

XIV. MODULATORS/DEMODULATORS

XV. MULTIPLEXERS

XVI. MULTIPLIERS

XVII. OPERATIONAL AMPLIFIERS

XVIII. OPTOELECTRONIC CIRCUITS

XIX. OSCILLATORS

XX. PERIPHERAL INTERFACING

XXI. POWER SUPPLIES

XXII. PROTECTION CIRCUITS

XXIII. PULSE GENERATORS

XXIV. SOFTWARE/CALCULATORS

XXV. SOFTWARE/COMPUTERS

1. AMPLIFIERS

Pair of pnp/npn transistors form high-voltage amplifier

by H. F. Nissink
Electrical Engineering Department, University of Adelaide, Australia

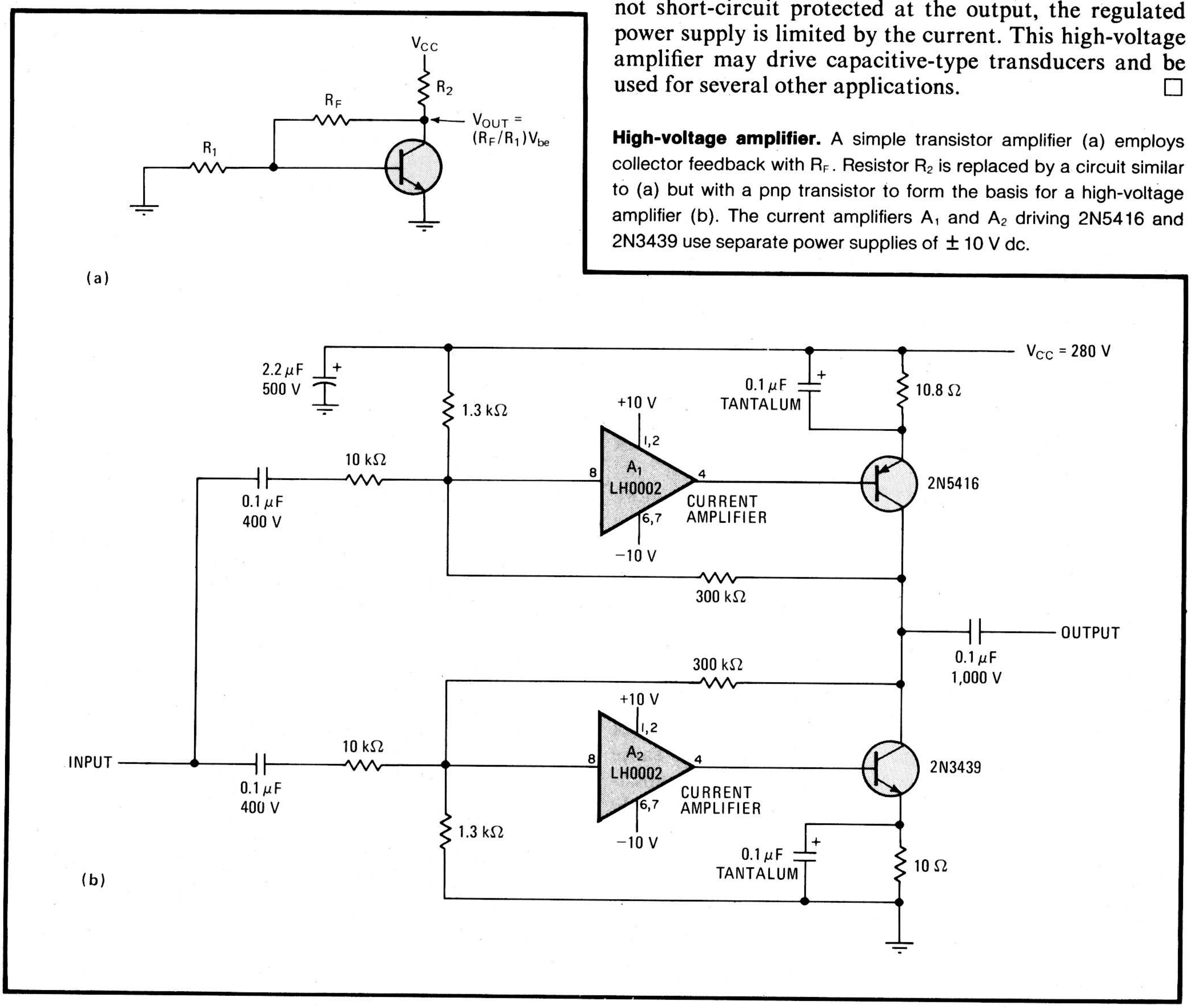
This simple high-voltage amplifier circuit provides a large output voltage swing with low-current consumption and uses only a few components. Its 280-volt regulated supply produces an unclipped output of up to 260 V peak to peak. In addition, rise and fall times of the output for a square-wave input are 150 nanoseconds, and the no-load supply current is only 4 milliamperes.

The principle behind this circuit is just a simple transistor amplifier (a) employing collector feedback through resistor R_F. The dc output is approximately $V_{be} \times R_F/R_1$. The circuit has an active pull-down action, with pull-up through R_2. However, if R_2 is replaced with a pnp transistor in a similar circuit, the pull-up and pull-down are through the transistor.

This substitution is the basis for the circuit in (b). Its output-voltage level is theoretically determined by the 300-kilohm and 1.3-kΩ resistors and thus the ac circuit gain is approximately 300 kΩ/10 kΩ = 30. The power supply (±10 V dc) for the current amplifier A_1 driving 2N5416 is isolated from the supply for A_2, which is driving the 2N3439.

The circuit has an input impedance of 5 kΩ and an output impedance of 2.4 kΩ. For the component values shown, the actual gain measures about 27, and the output over the frequency range of 1 kilohertz to 300 kHz is 260 V peak to peak (without clipping) and 100 V peak to peak at 1 megahertz. Because the amplifier is not short-circuit protected at the output, the regulated power supply is limited by the current. This high-voltage amplifier may drive capacitive-type transducers and be used for several other applications. □

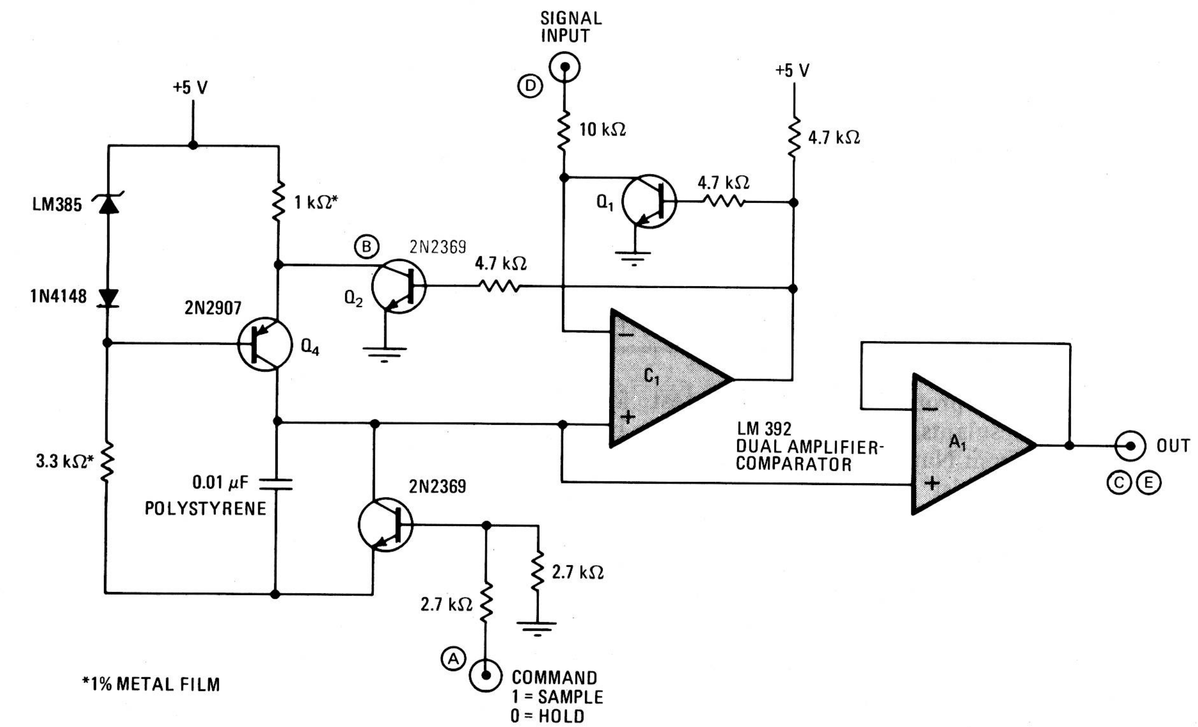
High-voltage amplifier. A simple transistor amplifier (a) employs collector feedback with R_F. Resistor R_2 is replaced by a circuit similar to (a) but with a pnp transistor to form the basis for a high-voltage amplifier (b). The current amplifiers A_1 and A_2 driving 2N5416 and 2N3439 use separate power supplies of ± 10 V dc.

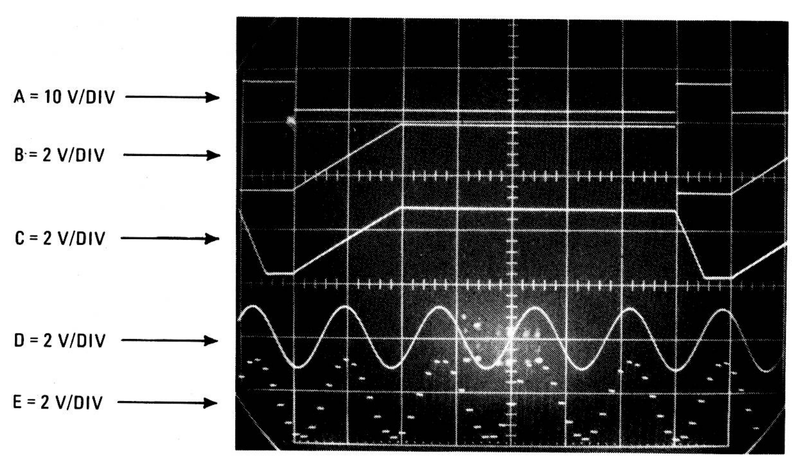


Dual-function amp chip simplifies many circuits

by Jim Williams
National Semiconductor Corp., Santa Clara, Calif.

Various circuits that combine low cost, single- or dual-supply operation, and ease of use can easily be built with comparators and operational amplifiers like National Semiconductor's LM339 and LM324 because of their general applicability to a wide range of design problems. Now circuit complexity can be reduced even further with up-and-coming dual-function devices like the LM392, which put both a comparator and an op amp on one chip. Besides allowing a degree of flexibility in circuit function not readily implemented with separate chips, this device retains simplicity at low cost. The building of such circuits as a sample-and-hold circuit, a feed-forward low-pass filter, and a linearized platinum thermometer is





1. Compact sampler. A comparator and op amp chip consolidates a sample-and-hold circuit, which utilizes only one supply, has virtually zero gain error, and will not self-trigger. Owing to the configuration, the device does not have to rely on the hold cycle, so that the circuit is simplified.

discussed here in the first of two articles.

The circuit in Fig. 1 is an unusual implementation of the sample-and-hold function. Although its input-to-output relationship is similar to standard configurations, its operating principle is different. Key advantages include no hold-step glitch, essentially zero gain error and operation from a single 5-volt supply.

When the sample-and-hold command pulse (trace A) is applied to transistor Q_3, it turns on, causing Q_4's collector to go to ground. Thus the output sits at ground. When the command pulse drops to logic 0, however, Q_4 drives a constant current into the 0.1-microfarad capacitor (trace B). At the instant the capacitor ramping voltage equals the signal input voltage, comparator C_1 switches, thereby causing transistor Q_2 to turn off the current source. Thus the voltage at Q_4's collector and A_1's output (trace C) will equal the input.

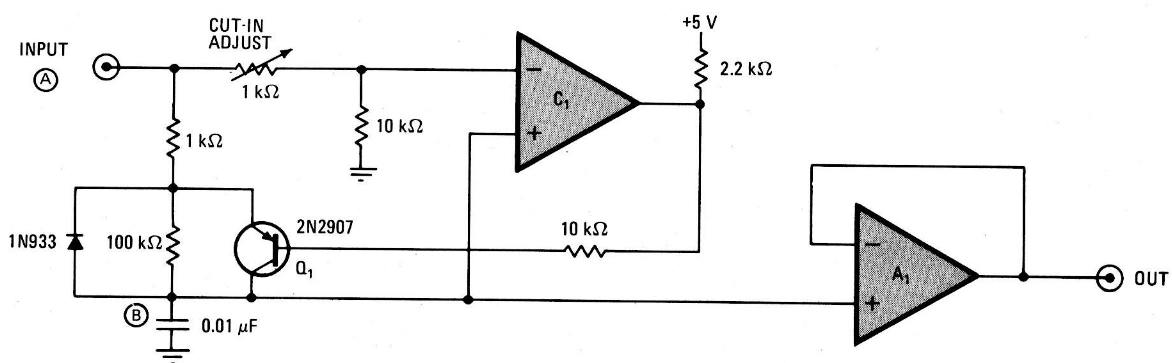
Q_1 ensures that the comparator will not self-trigger if the input voltage increases during a hold interval. If a dc-biased sine wave should be applied to the circuit (trace D), a sampled version of its contents will appear at the output (trace E). Note that the ramping action of the current source, Q_4, will just be visible at the output during sample states.

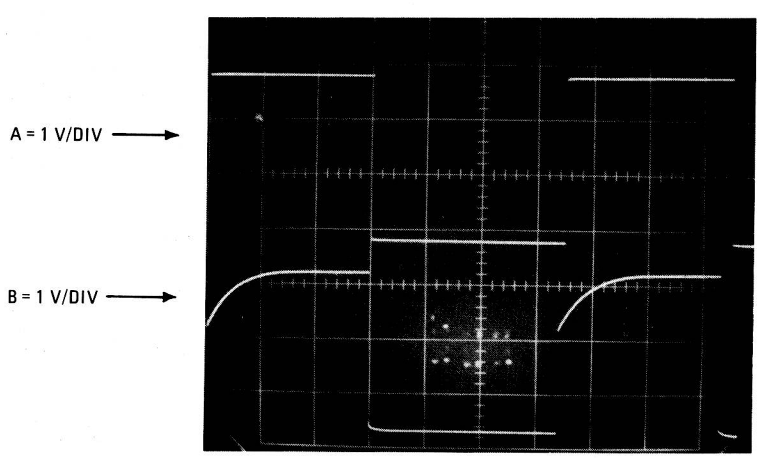
In Fig. 2, the LM392 solves a problem common to filters used in multiplexed data-acquisition systems, that of acquiring a signal rapidly but providing a long filtering time constant. This characteristic is desirable in electronic scales where a stable reading of, for example, an infant's weight is desired despite the child's motion on the scale's platform.

When an input step (trace A) is applied, C_1's negative input will immediately rise to a voltage determined by the setting of the 1-kilohm potentiometer. C_1's positive input, meanwhile, is biased through the 100 K $-$0.01 F time constant, and phase lags the input. Under these conditions, C_1's output will go low, turning on Q_1.

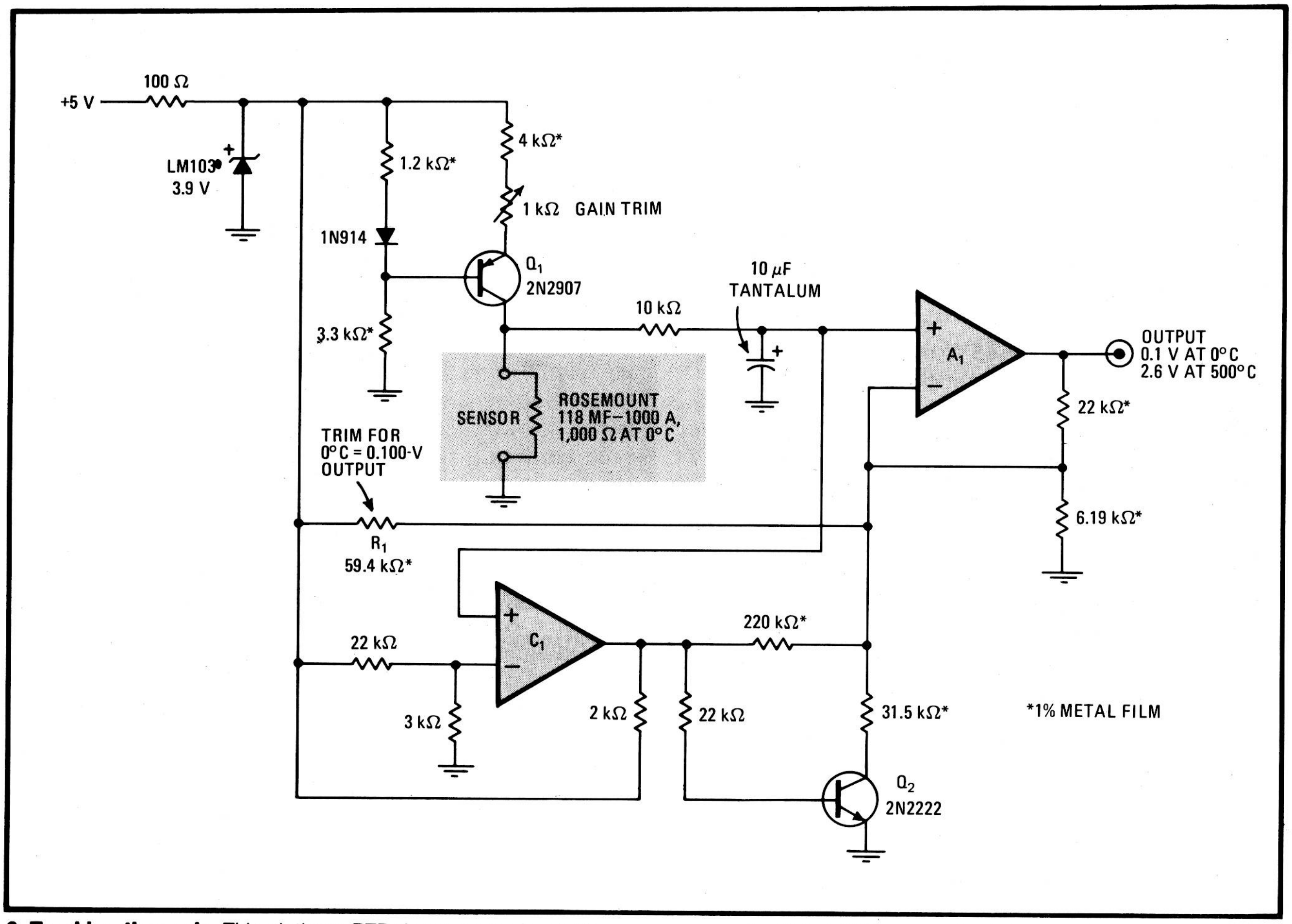
This action causes the capacitor (trace B) to charge rapidly up to the input value. When the voltage across the capacitor equals the voltage at C_1's positive input, C_1's output will go high, turning off Q_1. Now, the capacitor can only charge through the 100-kΩ resistor and the time constant must therefore be long.

The point at which the filter switches from the short to the long time constant is adjustable with the potentiometer. Normally, this pot will be set so that switching occurs at 90% to 98% of the final value (note that the trip point is taken at about the 70% point in the photo so that circuit operation may be easily seen). A_1 provides a buffered output. When the input returns to zero, the





2. Feedforward. This simple low-pass filter provides sharp acquisition and long decay, so that it is perfect for multiplexed data systems and electronic scales for infants. Its time constant is adjustable with the potentiometer and is typically set to 90% to 98% of the full input value.



3. Tracking thermals. This platinum RTD thermometer has 99% accuracy over the 0°-to-500°C range. C_1 derives the breakpoint change in A_1's gain for sensor outputs exceeding 250°C, compensating for the sensor's nonlinearity. Current through the 220-kΩ resistor shifts A_1's offset voltage, in effect preventing glitches at the breakpoint. The instrument is calibrated only at two points with a decade resistor box.

1N933 diode (a low forward-drop type), provides rapid discharge for the capacitor.

In Fig. 3, the LM392 is used to provide gain and linearization for a platinum resistor-temperature device in a single-supply thermometer circuit. This one measures from 0°C to 500°C with ±1° accuracy.

Q_1 functions as a current source that is slaved to the 3.9-V reference. The constant-current–driven platinum sensor consequently yields a voltage drop that is proportional to its temperature. A_1 amplifies the signal and provides the circuit output.

Normally, the slightly nonlinear response of the sensor would limit the circuit accuracy to about ±3°C. C_1 compensates for this error by generating a breakpoint change in A_1's gain at sensor outputs corresponding to temperatures exceeding 250°C. Then, the potential at the comparator's positive output exceeds the potential at the negative input and C_1's output goes high. This turns on Q_2, which shunts A_1's 6.19-kΩ feedback resistor and causes a change in gain that compensates for the sensor's slight loss of gain from 250° to 500°C. Current through the 220-kΩ resistor shifts the offset voltage of A_1 so no discernible glitch will occur at the breakpoint.

A precision decade box should be used to calibrate this circuit. Once inserted in place of the sensor, it is adjusted for a value of 1,000 ohms and a 0.10-V output by means of resistor R_1. Next, its resistance is set to 2,846 Ω (500°C) and its gain trim control adjusted for an output of 2.6 V. These adjustments are repeated until the zero and full-scale readings remain fixed at these points. □

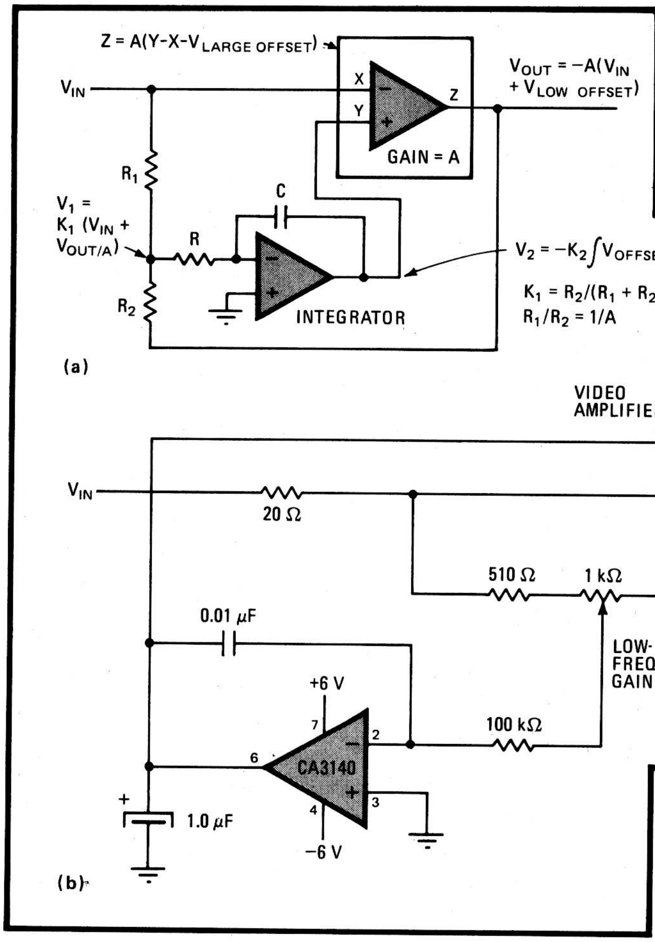
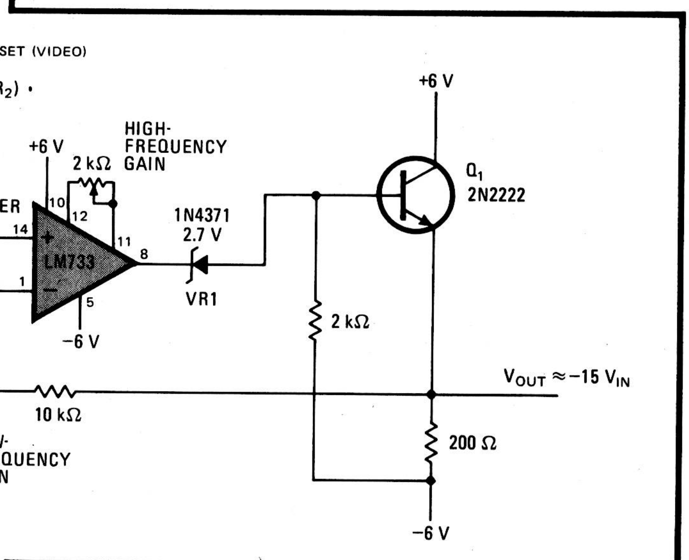
Feedback reduces offset in wideband video amplifiers

by Alan Cocconi
California Institute of Technology, Pasadena, Calif.

Wideband video amplifiers such as the LM733 generally have large input offset voltages that, when multiplied by their gain, can result in unacceptably high dc offset at the output. This undesirable effect can be reduced by feedback by means of a low–input-offset integrator.

As shown in (a), summing resistors R_1 and R_2 are selected so that the input to the integrator is proportional to the video amplifier's input offset voltage. The integral feedback drives the video amp's input offset to zero, leaving only the low offset of the integrator (which can be trimmed to zero) to appear at the amplifier output.

A practical implementation of the approach is given in (b). The integrating operational amplifier, a CA3140, was chosen for its low input offset voltage. Here, the 1N4371 zener diode and the 2N2222 transistor, in an emitter-follower configuration, are required to ensure that the output can go down to 0 volt, since the 733 video amp suffers from the restriction of a minimum positive output voltage. □

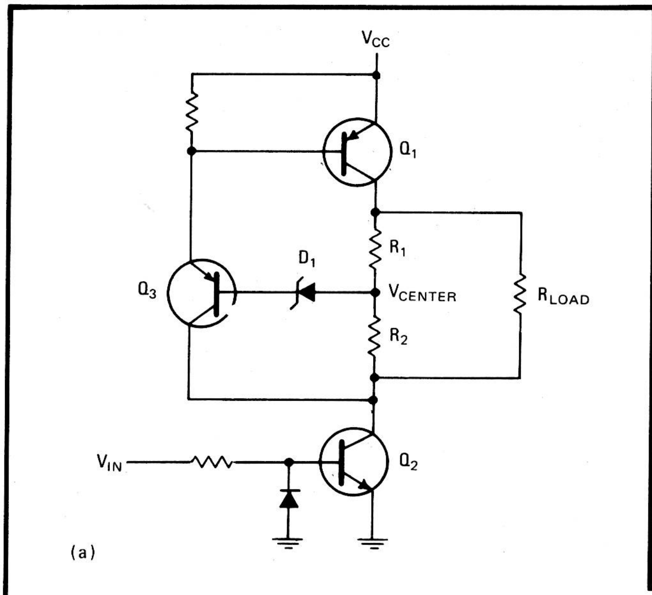
Reducing offset. The offset voltage of a wideband video amplifier can be reduced almost to zero if a resistor-scaled feedback integrator is applied (a). Practical implementation (b) adds a zener diode and an emitter follower in order to push the output of LM733, which has a minimum positive output voltage, down to zero.

Power-sharing bridge circuit improves amplifier efficiency

by Jim Edrington
Texas Instruments Inc., Austin, Texas

This linear bridge amplifier offers several advantages in driving motors and servo systems, including obtaining maximum efficiency with a single power supply and with dc coupling, which as a result reduces circuit complexity. Most notable, however, is that the four transistors in the amplifier will equally share load currents, as well as simplifying the drive requirements. These factors permit lower-cost transistors to be applied and allow their heat-sink requirements to be reduced.

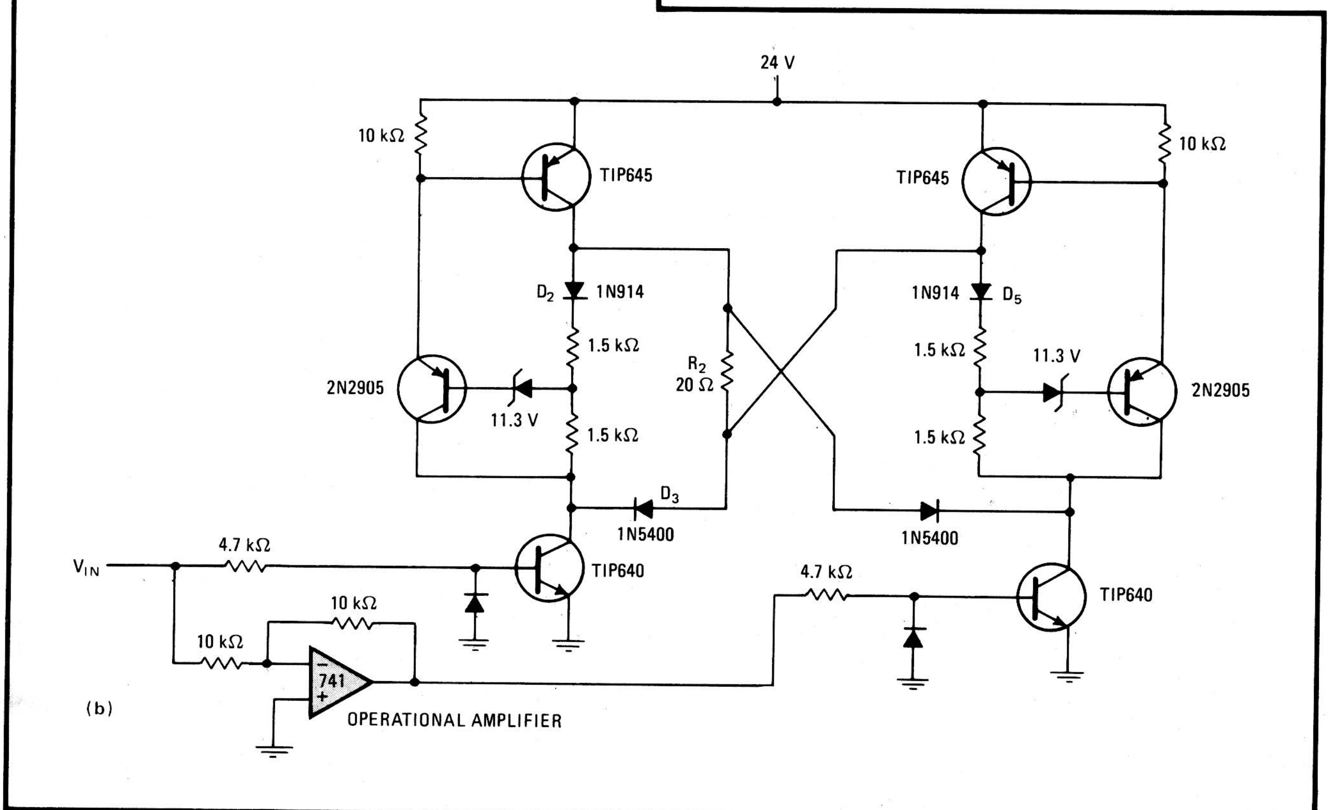
Shown in (a) is one half of the bridge-type circuit, which illustrates the amplifier's operation. Positive input excursions from the driver turn on current sink Q_2, with a portion of Q_2's collector current passing through transistor Q_3. Q_3's current flow causes source transistor Q_1 to turn on.



Because the majority of the flow must pass through Q_1 and Q_2, the collector-to-emitter voltage of both transistors must be equal to ensure equal power dissipation. This voltage-matching requirement is achieved by clamping the gain of Q_1 to the voltage at the center of the load with a zener diode. Thus the virtual center of the load will be maintained at $V_{cc}/2$ and $V_{Q_1ce} = V_{Q_2ce}$, provided $R_1 = R_2$. The zener diode, D_1, must have a value of $V_z = (V_{cc}/2) - 1.4$ to meet the requirement for the reference potential.

Two of these circuits may be readily incorporated into a full-bridge arrangement, as shown in (b), that is suitable for driving electromechanical devices. Adding diodes D_2 through D_5 isolate one branch's functions from the other. With this configuration, each branch conducts for half of the input cycle thereby eliminating virtually all crossover difficulties.

The isolation diodes will alter the divider's center voltage by 0.7 volts, however, and so the value of the zener voltage must be slightly changed. In this case, it will be $V_z = (V_{cc}/2) - 1.4 + 0.7 = 11.3$ V. In most applications, selecting the nearest standard zener value will suffice. □



Divided driver. A rudimentary amplifier (a) may be designed so that Q_1 and Q_2 carry equal load on a positive excursion of an input signal, using a zener diode of suitable value for biasing a load center to cause $V_{Q_1ce} = V_{Q_2ce}$. Combining two such sections in a balanced bridge arrangement (b) builds a dc-coupled amplifier that is simple, can run from one supply, and can ensure that all amplifiers may handle a proportionate share of the power. This combination reduces electrical specifications of individual transistors, thereby reducing their cost.

Knowing gate-charge factor eases power MOS FET design

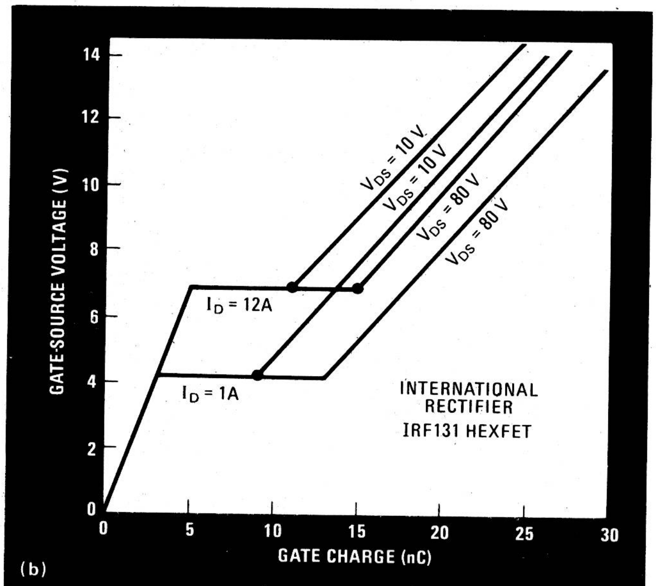
by Brian Pelly
International Rectifier Corp., El Segundo, Calif.

Unlike bipolar transistors, power MOS field-effect transistors are essentially voltage-controlled devices whose drive circuits are best designed around their gate-charge factor. Obtaining a measurement of this factor with this circuit (a) will ease switching-time calculations and, as a result, reduce drive-component selection to a series of simple Ohm's Law equations.

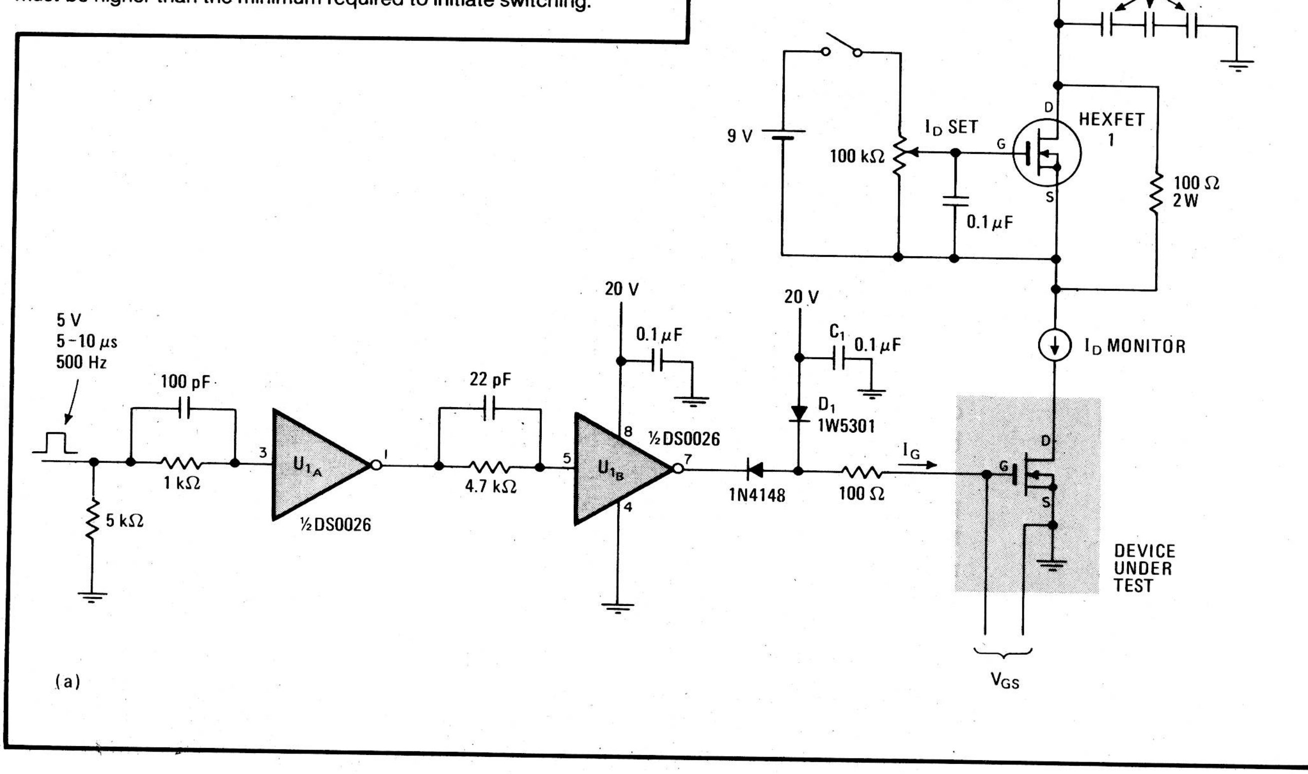
Gate charge comprises both gate-to-source and gate-to-drain (Miller) capacitances. To measure this charge, a constant current is supplied to the gate of the device under test from capacitor C_1 through regulator diode D_1. In addition, a constant current is established in the drain circuit by setting the voltage on the gate of power MOS FET Hexfet 1. The net charge consumed by the gate is related to the given current and voltage that is in the source-to-drain path.

The graph in (b) represents gate voltage versus gate charge in nanocoulombs. It shows exactly when the gate-to-source and gate-to-drain capacitances take on charge. The first voltage rise charges the gate-to-source capacitance and the flat portion charges the gate-to-drain capacitance. At the second voltage rise, both capacitances are charged to a level that can switch the given voltage and current.

Although the second voltage rise indicates the point at which the switching operation is completed, the design safety margin requires that the drive-voltage level applied to the gate be slightly higher than the voltage that is required to switch the given drain current and voltage. Since gate charge is the product of the gate input current and the switching time, a designer can quickly develop a drive circuit that is appropriate for the switching time required. □



Charge. The gate-charge factor, measured with test circuit (a), is the total charge that must be supplied to the gate to switch a given drain current and voltage. The gate voltage versus gate charge (b) for Hexfet IRF 131 shows that the total charge consumed by the gate must be higher than the minimum required to initiate switching.



Dynamic depletion circuits upgrade MOS performance

by Clay Cranford, *IBM Corp.,*
System Communications Division, Research Triangle Park, N. C.

In the design of MOS integrated circuits, the need frequently arises for an efficient, low-power driver to charge and discharge high-capacitance loads, be they on chip or off. Standard driver circuits include either enhancement-depletion inverters or inverters with push-pull output stages. However, both suffer from high input capacitance, and with a push-pull driver the high-state output voltage is limited to a threshold-voltage drop below the power-supply potential. Clocked driver circuits cut power dissipation, but chip area must be provided for clock-signal generation or routing or both.

Two new circuit solutions include the dynamic depletion-mode driver (Fig. 1) and the active bootstrap driver (Fig. 2). The first takes advantage of the high conductance of a depletion-mode device under high gate bias. The output can be charged to the full power-supply voltage, V_{DD}, and dc power is reduced by limiting the low output-level current drain. The idea behind the approach is to charge a bootstrap capacitor, C_B, and then redistribute that capacitor's charge when the output is being driven to its high level.

In Fig. 1, transistor Q_6 serving as the bootstrap capacitor is charged to V_{DD} when the input is low. Q_4 is in a low-conductivity state and Q_3 and Q_5 are turned on, causing the gate of Q_7 to be held near ground. As the input rises, the charge on C_B is redistributed between C_B and the gate of Q_7 via Q_4. At this point, Q_3 and Q_5 turn off (Q_3 has functioned as the dynamic depletion-mode device, switching between conductive and nonconductive states). Device Q_7 is switched to its linear region and Q_8 has turned off, charging the output to V_{DD}.

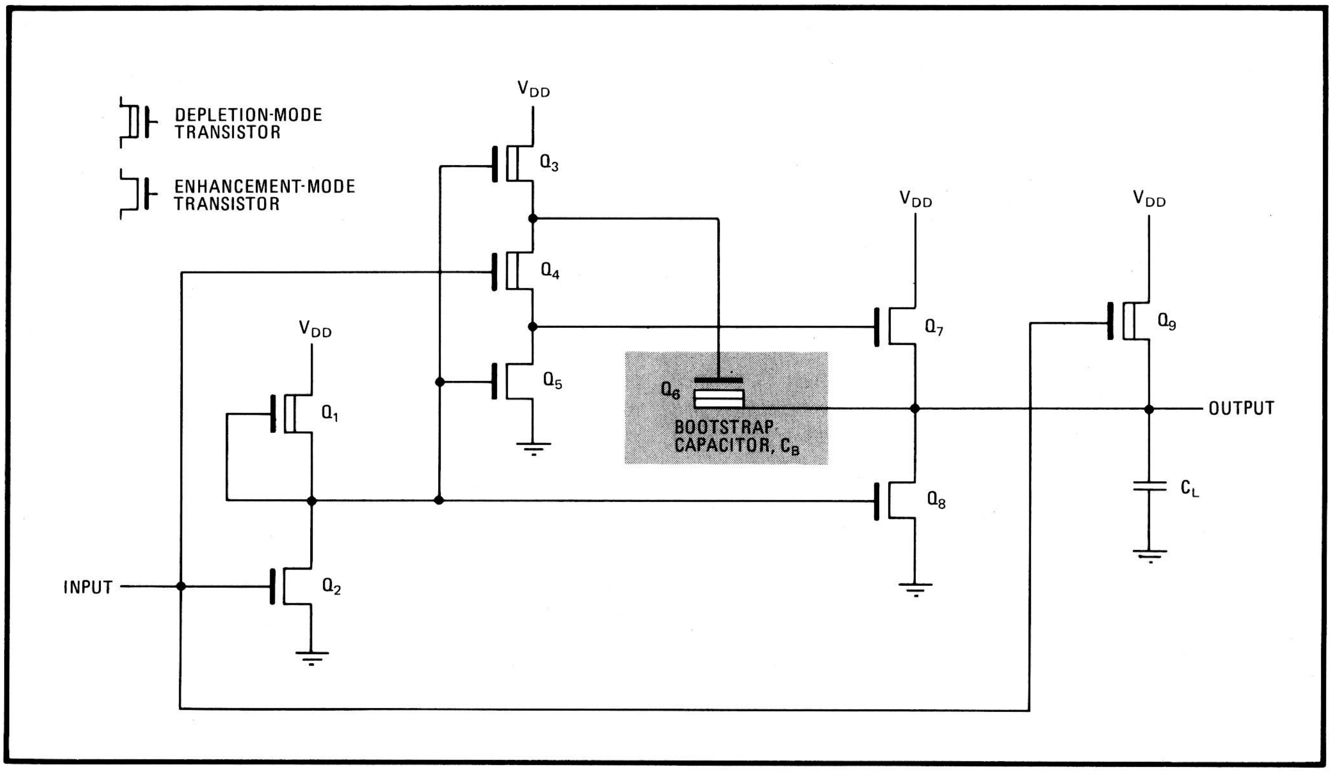
In the active bootstrap technique (Fig. 2), a voltage-bootstrapping circuit and a power-down feature provide a large amount of overdrive and a reduced output-low power dissipation, respectively. The operation of this circuit also has several steps.

With the input low, node 1 is high. Q_6 is turned off and Q_7 turned on; consequently, node 3 is low and driver Q_3 shuts off. Since Q_8 can be made physically long, its current can be limited to a negligible amount. This accounts for the minimal output-low current.

When the input is raised, Q_6 turns on, and after one inverter delay, Q_7 turns off. The bootstrap capacitor—Q_5 in this circuit—is then charged to approximately a threshold voltage below the input, since node 2 is heavily loaded. Node 2 is held near ground by Q_4 during part of the time that Q_6 is turned on because of the inverter delay between the input and the gate of Q_4.

If node 2 begins to move upward during this precharge period because of different loading conditions or because Q_6 is given a smaller width-to-length ratio, Q_6 will dynamically precharge node 3, being bootstrapped by the rising voltage at node 2 and the bootstrap capacitor, and it will turn off when node 3 reaches a threshold voltage below the level of the input signal. Q_4 is not conducting while node 2 is being charged through Q_3.

Since the bootstrap capacitor is precharged, it will



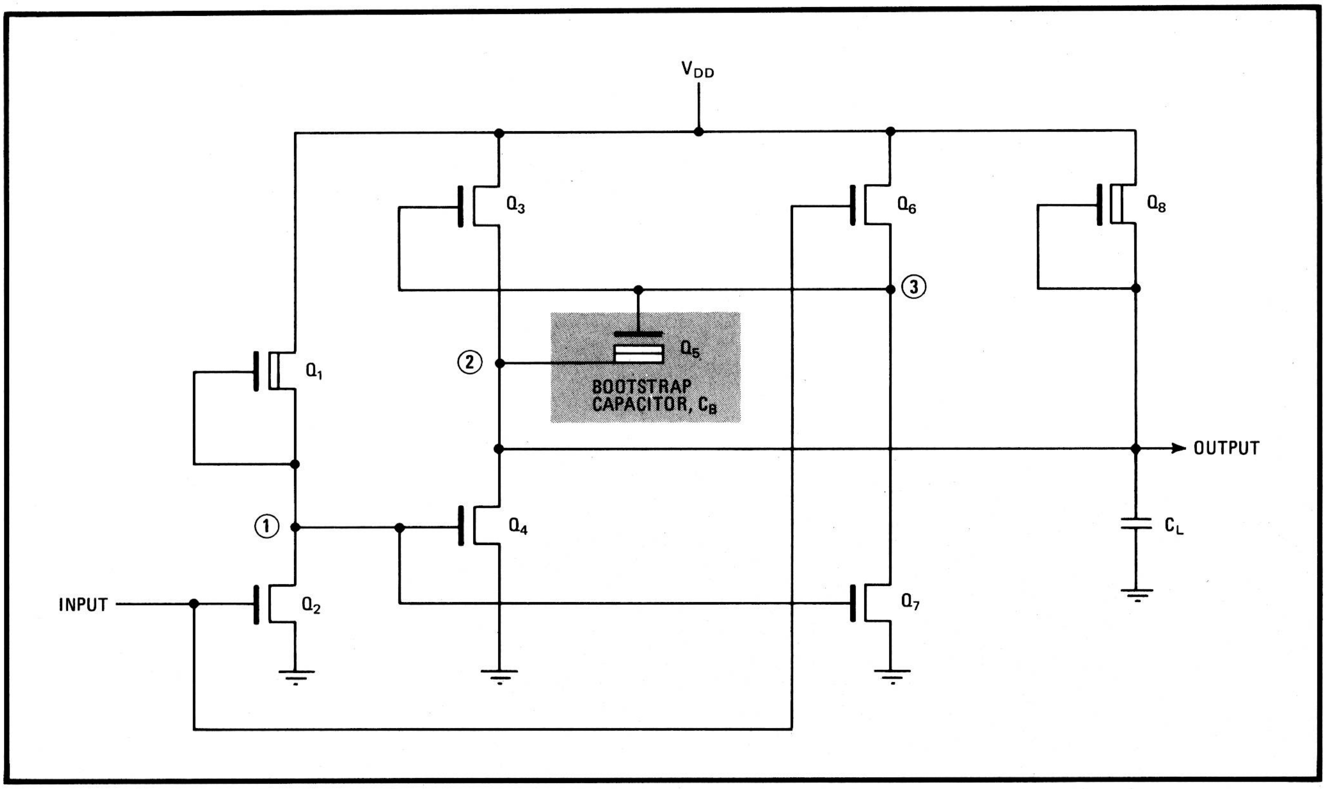
1. Dynamic driver. Bootstrap capacitor C_B is charged to V_{DD} when the input is low, causing the gate of Q_7 to be held near ground. As the input rises, the charge on C_B is redistributed between C_B and the gate of Q_7. The output is charged to V_{DD} as Q_7 is switched to its linear region.

boost node 3 to a voltage higher than a threshold drop below the input. This provides increased on-drive for Q_3 and, in turn, a faster rising output transition than might otherwise be possible. The actual voltage to which node 3 is bootstrapped is determined by the ratio of the bootstrap capacitance to that of Q_3 plus the contribution made by parasitic capacitances.

When the input falls, Q_6 turns off, Q_7 turns on, and node 3 is pulled near ground. Q_3 enters a nonconducting state, resulting in a rapidly falling response, since Q_4 need sink current only from the load capacitance. This action helps to reduce the down-level power consumption as well.

Unlike the dynamic depletion-mode driver, this configuration provides for dynamic precharging of the bootstrap capacitor directly from the power supply (through Q_6). A detailed analysis shows that to obtain a given amount of bootstrap voltage, a bootstrap capacitor less than half the size of that necessary for other configurations is required. For the typical layout, it will be considerably less than half.

The active bootstrap technique can be applied wherever high speed and low power are prime considerations—if the extra chip area required is acceptable. The circuit of Fig. 2 has been designed and tested using n-channel silicon-gate technology. □



2. Better bootstrap. With the input low, node 1 is high, Q_6 is turned off, and Q_7 is turned on. As a result, node 3 is low and driver Q_3 shuts off. Q_8 can be made physically long, limiting its current and reducing overall power consumption.

Exploiting the full potential of an rf power transistor

by Dan Moline and Dan Bennett
Motorola Semiconductor Products Sector, Phoenix, Ariz.

With improved packaging and appropriate circuit design, the new MRF630 radio-frequency power transistor can be used out to its design limits—the generation of 3 watts with 9.5 decibels of gain at ultrahigh frequencies when assembled with an all-gold metal system.

Good heat sinking enables Motorola's low-cost grounded-emitter TO-39 package for rf transistors to perform like a stripline opposed-emitter type. In this package, the MF630, also from Motorola, shows impressive boardband response, excellent heat dissipation, and high reliability.

So that heat can flow directly away from the transistor die, a flange is soldered to the bottom of the TO-39 can and secured to a heat sink by one or two screws (Fig. 1a). This assembly method maximizes heat dissipation while minimizing space requirements. Also, electrical grounding is better as the package is now connected mechanically to the chassis ground.

The broadband uhf amplifier circuit in Fig. 1b uses a distributed-element design to optimize the gain and bandwidth of the MRF630. The transmission lines are simulated by epoxy fiberglass G-10 board, whose high dielectric constant and low cost keep the circuit small