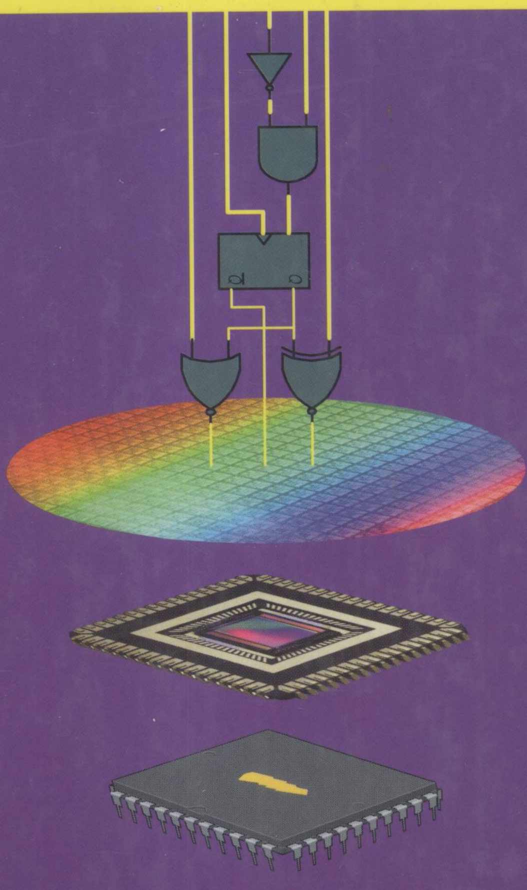
ADVANCED ASIC CHIP SYNTHESIS

Using Synopsys® Design Compiler™ Physical Compiler™ and PrimeTime®

SECOND EDITION



Himanshu Bhatnagar

Kluwer Academic Publishers

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KLUWER ACADEMIC PUBLISHERS
Boston / Dordrecht / London

Distributors for North, Central and South America:
Kluwer Academic Publishers
101 Philip Drive
Assinippi Park
Norwell, Massachusetts 02061 USA
Telephone (781) 871-6600
Fax (781) 871-6528
E-Mail <kluwer@wkap.com>

Distributors for all other countries:
Kluwer Academic Publishers Group
Distribution Centre
Post Office Box 322
3300 AH Dordrecht, THE NETHERLANDS
Telephone 31 78 6392 392
Fax 31 78 6546 474
E-Mail <orderdept@wkap.nl>

Electronic Services <http://www.wkap.nl>

Library of Congress Cataloging-in-Publication Data

Printed on acid-free paper.

Printed in the United States of America

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To my wife Nivedita
and my daughter Nayan

Foreword

The semiconductor industry has a proven track record of quickly reducing reference to IC design scale to the ridiculously irrelevant. We, as a group, quickly saturated our terminology to refer to levels of integration as we applied the term "Large Scale Integration" (LSI) in the mid 80's to chips containing more than 1,000 transistors and moved to the more progressive "Very Large Scale" (VLSI) as we passed into the 10,000 to 100,000 transistor territory only a year or two later. A few more attempts at renaming our design output with terms such as ULSI (Ultra-Large Scale Integration) were fortunately left in the annals of history as the more insightful realized that the consequences of Moore's Law would quickly require us to move beyond the confines of the English language to create appropriate superlatives. We, however, could not resist changing our conception of the design task by coining the phrase "System on a Chip" in the early to mid 90's to convey the understanding that these levels of integration allowed for the development of more than complex electronic components but self contained information processing systems. Once again, however, we find ourselves struggling with the reality that the "systems" referred to only 3 to 4 years ago are today barely enough to fill the pad ring of a modest pin count device.

We should not be surprised, therefore, that some in the design community are recognizing the need to again rethink and redefine the metrics that scope the modern IC design task. Now, however, instead of focusing on the collection of transistors or functions as a metric of design production, this group has moved to focus on our most precious commodity, time. For them, today's design task is being defined by the window of opportunity in which the design output is relevant, usually a period that cannot extend beyond 12 - 18 months. This group, therefore, is focused on the tools and techniques that can raise the design productivity to the point that the transistor counts, functions and subsystems that can fill the silicon can be reliably designed and characterized in this amount of time. We should not be caught completely by surprise therefore if our lexicon begins to define levels of integration with terms such as SMSI ("Six Month Scale Integration") or TMSI ("Twelve Month Scale Integration") perhaps.

This books sets itself squarely in the middle of this effort as it explores and conveys a collection of tools and techniques focused on dramatically reducing the time required to complete the IC design task and get an IC product to market. The author, Mr. Bhatnager, takes a set of today's most productive IC design tools and exposes ways in which these tools can be applied to further streamline the full design process. These techniques challenge the designer to move beyond linear high-level design flows that utilize HDL languages for design description, synthesis to create gate and transistor implementation and timing analysis. This book exposes practical techniques by which more information can either be introduced sooner in the design flow or fed back quicker in order to both reduce the number of iterations and the complexity associated with each one. The result is techniques that lead to better quality designs sooner.

Today's semiconductor business operates in the world of compressed time and hyper-competition. To compete effectively in this world every designer and every design team is well advised to focus on continually improving their time-to-market metric. This book will serve the advanced student in VLSI design as well as the seasoned practitioner in this quest.

Mr. F. Matthew Rhodes
Sr. Vice President and General Manager
Personal Computing Division
Conexant Systems, Inc.

Preface

This second edition of this book describes the advanced concepts and techniques used towards ASIC chip synthesis, physical synthesis, formal verification and static timing analysis, using the Synopsys suite of tools. In addition, the entire ASIC design flow methodology targeted for VDSM (Very-Deep-Sub-Micron) technologies is covered in detail.

The emphasis of this book is on real-time application of Synopsys tools, used to combat various problems seen at VDSM geometries. Readers will be exposed to an effective design methodology for handling complex, sub-micron ASIC designs. Significance is placed on HDL coding styles, synthesis and optimization, dynamic simulation, formal verification, DFT scan insertion, links to layout, physical synthesis, and static timing analysis. At each step, problems related to each phase of the design flow are identified, with solutions and work-around described in detail. In addition, crucial issues related to layout, which includes clock tree synthesis and back-end integration (links to layout) are also discussed at length. Furthermore, the book contains in-depth discussions on the basics of Synopsys technology libraries and HDL coding styles, targeted towards optimal synthesis solution.

Target audiences for this book are practicing ASIC design engineers and masters level students undertaking advanced VLSI courses on ASIC chip design and DFT techniques.

This book is not intended as a substitute or a replacement for the Synopsys reference manual, but is meant for anyone who is involved in the ASIC design flow. Also, it is useful for those designers (and companies) who do not have layout capability, or their own technology libraries, but rely on outside vendors for back-end integration and final fabrication of the device. The book provides alternatives to traditional method of netlist hand-off to outside vendors because of various problems related to VDSM technologies. It also addresses solutions to common problems faced by designers when interfacing various tools from different EDA tool vendors.

All commands have been updated to Tcl version of Design Compiler in this edition of the book. The commands have been changed to reflect the most up–to–date version (2000.11–SP1) of Synopsys suite of tools.

Overview of the Chapters

Chapter 1 presents an overview to various stages involved in the ASIC design flow using Synopsys tools. The entire design flow is briefly described, starting from concept to chip tape-out. This chapter is useful for designers who have not delved in the full process of chip design and integration, but would like to learn the full process of ASIC design flow.

Chapter 2, outlines the practical aspects of the ASIC design flow as described in Chapter 1. Beginners may use this chapter as a tutorial. Advanced users of Synopsys tools may benefit by using this chapter as a reference. Users with no prior experience in synthesis using Synopsys tools should skip this chapter and return to it later after reading the rest of the chapters.

The basic concepts related to synthesis are described in detail in Chapter 3. These concepts introduce the reader to synthesis terminology used throughout the later chapters. Readers will find the information provided here useful by gaining a basic understanding of these tools and their environment. In addition to describing the purpose of each tool and their setup, this chapter also focuses on defining objects, variables, attributes and compiler directives used by the Design Compiler.

Chapter 4 describes the basics of the Synopsys technology library. Designers usually do not concern themselves with the full details of the technology library, as long as the library contains a variety of cells with different drive strengths. However, a rich library usually determines the quality of synthesis. Therefore, the intent of this chapter is to describe the Synopsys technology library from the designer's perspective. Focus is provided on delay calculation method and other techniques that designers may use in order to alter the behavior of the technology library, hence the quality of the synthesized design.

Proper partitioning and good coding style is essential in obtaining quality results. Chapter 5 provides guidelines to various techniques that may be used to correctly partition the design in order to achieve the optimal solution. In addition, the HDL coding styles is covered in this chapter that illustrates numerous examples and provides recommendations to designers on how to code the design in order to produce faster logic and minimum area.

The Design Compiler commands used for synthesis and optimization are described in Chapter 6. This chapter contains information that is useful for the novice and the advanced users of Synopsys tools. The chapter focuses on real-world applications by taking into account deviations from the ideal situation i.e., "Not all designs or designers, follow Synopsys recommendations". The chapter illustrates numerous examples that help guide the user in real-time application of the commands.

Chapter 7 discusses optimization techniques in order to meet timing and area requirements. Comparison between older version of Design Compiler and the new version is highlighted. Emphasis is provided on the new optimization technique employed by Design Compiler called "TNS". Also, detailed analysis on various methods used for optimizing logic is presented. In addition, different compilation strategies, each with advantages and disadvantages are discussed in detail.

DFT techniques are increasingly gaining momentum among ASIC design engineers. Chapter 8 provides a brief overview of the different types of DFT techniques that are in use today, followed by detailed description on how devices can be made scannable using Synopsys's Test Compiler. It describes commands used for inserting scan through Design Compiler. A multitude of guidelines is presented in order to alleviate the problems related to DFT scan insertion on a design.

Chapter 9 discusses the links to layout feature of Design Compiler. It describes the interface between the front-end and back-end tools. Also, this chapter provides different strategies used for post-layout optimization of designs. This includes in-place and location based optimization techniques. Furthermore, a section is devoted to clock tree insertion and problems related to clock tree transfer to Design Compiler. Various solutions to this common problem are described. This chapter is extremely valuable for designers (and companies) who do not posses their own layout tool, but would like to learn the place and route process along with full chip integration techniques.

The introduction of Physical Compiler dramatically changed the traditional approach to synthesis. Chapter 10 describes this flow in detail. The chapter describes various methods of achieving optimal results using Physical Compiler. In order to understand the Physical Compiler flow, readers are advised to read all chapters related to the traditional flow (especially Chapter 9) before reading this chapter. This will help correlate the topics described in this chapter to the traditional flow. Various example scripts are provided in this chapter illustrating the usage of this novel tool.

Chapter 11, titled "SDF Generation: for Dynamic Timing Simulation" describes the process of generating the SDF file from Design Compiler or PrimeTime. A section is devoted to the syntax of SDF format, followed by detailed discussion on the process of SDF generation, both for pre and post-layout phases of the design. In addition, few innovative ideas and suggestions are provided to facilitate designers in performing successful simulation. This chapter is useful for those designers who prefer dynamic simulation method to formal verification techniques, in order to verify the functionality of the design.

Chapter 12 introduces to the reader, the basics of static timing analysis, using PrimeTime. This includes a brief section devoted to Tcl language that is utilized by PrimeTime. Also described in this chapter are selected PrimeTime commands that are used to perform static timing analysis, and also facilitate the designer in debugging the design for possible timing violations.

The key to working silicon usually lies in successful completion of static timing analysis performed on a particular design. This capability makes static timing analysis one of the most important steps in the entire design flow and is used by many designers as a sign-off criterion to the ASIC vendor. Chapter 13 is devoted to several basic and advanced topics on static timing analysis, using PrimeTime. It effectively illustrates the usage of PrimeTime, both for the pre and the post-layout phases of the ASIC design flow process. In addition, numerous examples on analyzing reports and suggestions on various scenarios are provided. This chapter is useful to those who would like to migrate from traditional methods of dynamic simulation to the method of analyzing designs statically. It is also helpful for those readers who would like to perform in-depth analysis of the design through PrimeTime.

Conventions Used in the Book

All Synopsys commands are typed in "Ariel" font. This includes all examples that contain synthesis and timing analysis scripts.

The command line prompt is typed in "`Courier New`" font. For example:

```
dc_shell>        and,        pt_shell>
```

Option values for some of the commands are enclosed in < and >. In general, these values need to be replaced before the command can be used. For example:

```
set_false_path –from <from list> –to <to list>
```

The "\" character is used to denote line continuation, whereas the "|" character represents the "OR" function. For example:

```
compile –map_effort low | medium | high \
        –incremental_mapping
```

Wherever possible, keywords are *italicized*. Topics or points, that need emphasis are underlined or highlighted through **bold** font.

Acknowledgements

I would like to express my heartfelt gratitude to a number of people who contributed their time and effort towards this book. Without their help, it would have been impossible to take this enormous undertaking.

First and foremost, a special thanks to my family, who gave me continuous support and encouragement that kept me constantly motivated towards the completion of this project. My wife Nivedita, who patiently withstood my nocturnal and weekend writing activities, spent enormous amount of time towards proofreading the manuscript and correcting my "Engineers English". I could not have accomplished this task without her help and understanding.

I would like to thank my supervisor, Anil Mankar for giving me ample latitude at work, to write the book. His moral support and innovative suggestions kept me alert and hopeful. I would also like to thank my colleagues at Conexant; Khosrow Golshan who helped me design the front cover of the book. He also provided me inescapable suggestions for the backend design flow. Young Lee, Hoat Nguyen, Vinson Chua, Hien Truong, Songhua Xu, Chilan Nguyen, Randy Kolar, Steve Schulz, Richard Ward, Sameer Rao, Chih-Shun Ding and Ravi Ranjan who devoted their precious time in reviewing the manuscript.

I was extremely fortunate to have an outstanding reviewer for this project, Dr. Kelvin F. Poole (Clemson University, S.C.). I have known Dr. Poole for a number of years and approached him for his guidance while writing this book. He not only proofread the entire manuscript word-by-word (gritting his teeth, I'm sure!), but also provided valuable suggestions, which helped make the book more robust. Thank you Dr. Poole.

I wish to express my thanks to Bill Mullen, Ahsan Bootehsaz, Steve Meier, Russ Segal, Juergen Froessl, Elisabeth Moseley, Kelly Conklin, Bob Moussavi and Amanda Hsiao at Synopsys, who participated in reviewing this manuscript and provided me with many valuable suggestions. Julie Liedtke and Bryn Ekroot of Synopsys helped me write the necessary Trademark information. Special thanks are also due to Jeff Echtenkamp, Heratch Avakian, Chung-Jue Chen and Chin-Sieh Lee of Broadcom Corporation for providing me valuable feedback and engaging in lengthy technical discussions. Thanks are also due to Kameshwar Rao (Consultant) Jean-Claude Marin (ST Microelectronics, France), Tapan Mohanti (Centillium Communications), Dr. Sudhir Aggarwal (Philips Semiconductors) and Abu Horaira (Intel Corporation) for giving me positive feedback at all times. Their endless encouragement is very much appreciated.

During SNUG 2000, I met Cliff Cummings (President & Consultant, Sunburst Designs). Cliff is very well known in this industry as an expert in Verilog RTL coding and synthesis. I asked him to help me review certain chapters of my book. I would like to thank him for providing valuable suggestions, which I incorporated in Chapter 5.

Writing the second edition of this book took longer than previously anticipated. The main reason was the introduction of Physical Compiler. I wanted to enhance the book but did not want to write about something that was not mature. Carl Harris of Kluwer Academic Publishers understood this and supported me throughout the project. His understanding even when I kept on delaying the book is appreciated.

A final word, "Thank you Mom and Dad for your endless faith in me".

Himanshu Bhatnagar
Conexant Systems, Inc.
Newport Beach, California

About The Author

Himanshu Bhatnagar is an ASIC Design Group Leader at Conexant Systems, Inc. based in Newport Beach, California U.S.A. Conexant Systems Inc. is the world's largest independent company focused exclusively on providing semiconductor products for communication electronics. Himanshu has been instrumental in defining the next generation ASIC design flow methodologies using latest high performance tools from Synopsys and other EDA tool vendors.

Before Joining Conexant, Himanshu worked for ST Microelectronics in Singapore and the corporate headquarters based in Grenoble, France. He completed his undergraduate degree in Electronics and Computer Science from Swansea University (Wales, U.K), and his masters degree in VLSI design from Clemson University, (South Carolina, USA).

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