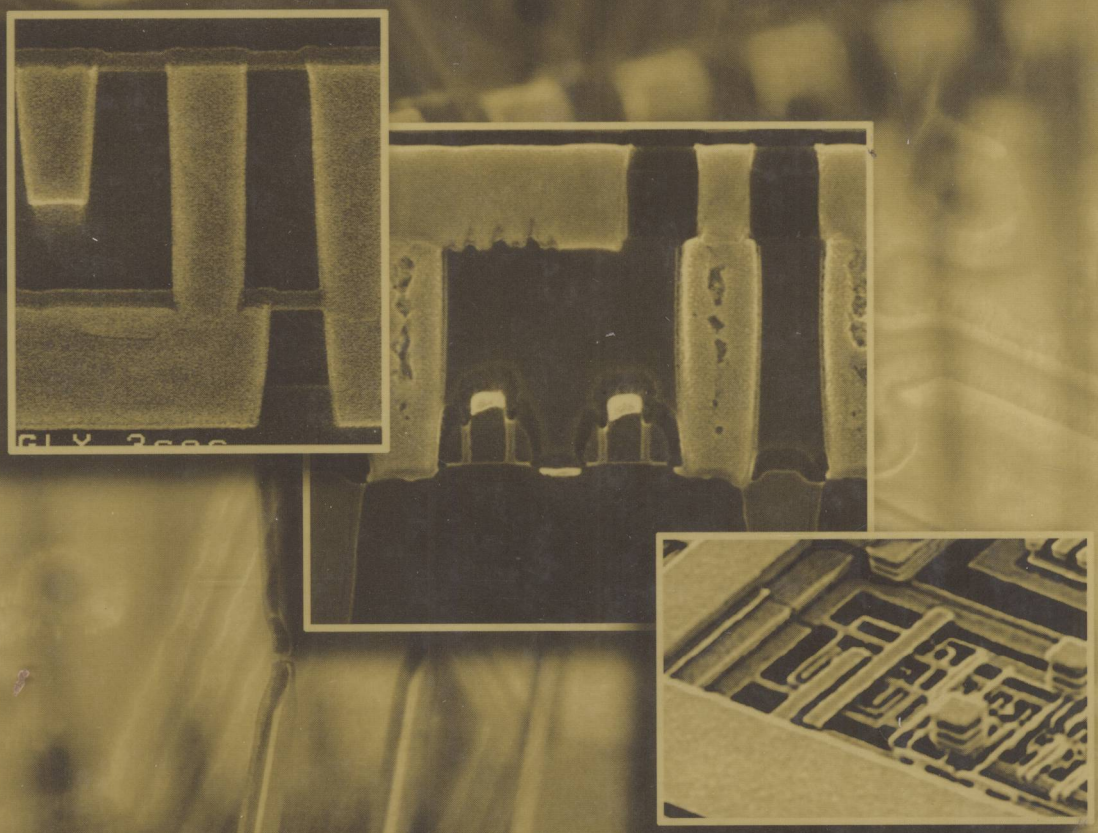
HANDBOOK OF SEMICONDUCTOR INTERCONNECTION TECHNOLOGY

Second Edition



EDITED BY
GERALDINE C. SCHWARTZ
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CRC Taylor & Francis
Taylor & Francis Group

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Taylor & Francis
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Boca Raton London New York

A CRC title, part of the Taylor & Francis imprint, a member of the Taylor & Francis Group, the academic division of T&F Informa plc.

Published in 2006 by
CRC Press
Taylor & Francis Group
6000 Broken Sound Parkway NW, Suite 300
Boca Raton, FL 33487-2742

Printed in the United States of America on acid-free paper
10 9 8 7 6 5 4 3 2 1

International Standard Book Number-10: 1-57444-674-6 (Hardcover)
International Standard Book Number-13: 978-1-57444-674-6 (Hardcover)
Library of Congress Card Number 2005054909

Library of Congress Cataloging-in-Publication Data

Handbook of semiconductor interconnection technology / edited by Geraldine C. Schwartz and Kris V. Srikrishnan.--2nd ed.
p. cm.
Includes bibliographical references and index.
ISBN 1-57444-674-6 (alk. paper)
1. Interconnects (Integrated circuit technology) 2. Semiconductors--Junctions. 3. Semiconductors--Design and construction. I. Schwartz, G. C. II. Srikrishnan, K. V., 1948-

TK7874.53.H36 2006
621.3815--dc22 2005054909

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Preface

Since the first edition of this handbook, semiconductor technology has gone through a continued evolution of new devices and materials like never before. Wafer sizes continue to grow with most of the new fabs equipped for 12-inch wafers. The changes are triggered by many considerations: continued need to provide more functions at lower cost; technology features less than 1000 Å requiring new processes, and exponential increase in the number of device elements. At the device level, the field effect transistor (FET) speed is continually improved by things such as use of insulating substrates, straining the silicon (channel region), and use of dual- and triple-gate (FINFET) structures. The interconnection technology is also going through changes, starting with copper wiring in place of AlCu, low-dielectric insulators in place of silicon dioxide, and use of cobalt and nickel silicide in place of titanium silicide for contacts. In parallel, the decreasing feature size and increasing aspect ratio of lines and studs (vertical vias), along with an increase in the number of wiring levels, have created not only the need for new materials but also unprecedented requirement of reliability per unit interconnect. This again has led to process innovations and improvement in equipment for depositing and patterning conducting and insulating films. *In situ* monitoring of several processes has become routine.

Many of the materials and processes described as likely directions in the first edition of this book have become standard in today's chip fabrication facilities: for example (1) dual damascene processes, including both insulator and metal polished using CMP, (2) use of electroplating of copper, which at one time was considered to be potentially fatal, and (3) fluorine-doped silicon dioxide followed by low-dielectric films containing silicon, carbon, hydrogen, and oxygen, and increasing discussion on the use of porous films. Even more fascinating is the evolution of the fabs which process the 12-inch wafers extensively, using single-wafer equipment that is kept isolated from ambient exposure through most of the process steps, traveling in ambient controlled tunnels from station to station with little human intervention. There has been a huge shift in the traditional focus for cleanrooms with emphasis shifting to particulate generation within tools and during processes from ambient- and operator-generated particulates. This is the main reason why the last chapter in the previous edition on cleanrooms has not been included in this revised edition.

Chapter 1 describes the equipment commonly used in manufacturing for deposition and etching and the principles underlying the design and use of the equipment. In this edition, electrochemical deposition equipment used for plating copper is discussed in detail, in addition to updating previous discussions on equipment used for evaporation, chemical vapor deposition (CVD), and plasma processes. Chapter 2 includes many standard techniques used for characterizing metal and insulator films. The principles of electrochemical deposition are also covered. Measurement of the mechanical and thermal properties of insulators is emphasized in this edition, as is the greater use of electron energy loss spectroscopy (EELS), energy filtering TEM, and atomic force microscopy (AFM). The several recently reported methods for characterizing porous dielectric thin films are also included. Chapter 3 is devoted to contacts and in this edition greater focus has been given to integration issues and properties of titanium, cobalt, and nickel. The need for borderless contacts for gates and source/drain has led to newer process schemes that are also discussed. Use of contact studs with planarized CVD tungsten has become widely established. From all indications this is not likely to change in the future. Based on the need to keep the devices and interconnection safely apart, the use of barrier films for both physical (diffusion barrier) and electrical (barrier heights) requirements is reviewed. Chapter 4 now includes a greater discussion of recently reported choices for low-dielectric insulators. The need for planarization at the macro level has become less, since the use of dual damascene has now become widespread; however, the challenges of managing topography fluctuations at the local level remain. There is extensive coverage of low dielectric constant insulators, particularly the newer ones. The mechanical properties of insulators have become important along with their

thermal and thermomechanical properties. Chapter 5 covers the deposition and etching of metallic films (tungsten, copper, aluminum) but a greater focus is placed on electroplated copper, with emphasis on the morphology of plated films and their properties. Clearly a big challenge for the next generations of devices is the continuing need to form thin adhesion and barrier layers for copper films in the lines and studs. This has led to the pursuit of atomic layer deposition processes and precursor materials that result in continuous nonporous films covering all sides of trench openings of high aspect ratios (two or more). Chapter 6 deals with two main issues: (1) the problems associated with topography and solutions to these problems, emphasizing the details of CMP and dual damascene processes, (2) process/structure choice conflicts, process compatibility, reliability, manufacturability, and methods for defect-free manufacturing. Chapter 7 is devoted to the reliability of thin metallic and insulating films and this revised edition has an expanded discussion on copper reliability. There is an extensive review of electromigration mechanism and testing procedures as well as other wear-out phenomena for wires and vias. The issue of corrosion is also addressed. The reliability of interlevel insulators is examined, with the impact of migration to low dielectric constant materials and the planned use of pores.

The Editors

Geraldine Cogin Schwartz was a senior engineer at IBM Microelectronics, Hopewell Junction, New York. She retired from IBM after more than 25 years of research in many areas of semiconductor interconnection technology and since has given several invited talks. A Fellow of the Electrochemical Society and a member of the American Vacuum Society and Sigma Xi, she is the author of several key publications in semiconductor technology and the holder of over 15 U.S. patents. Dr. Schwartz received a Ph.D. degree in chemistry from Columbia University, New York.

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Contents

CHAPTER 1

Methods/Principles of Deposition and Etching of Thin Films

Geraldine Cogin Schwartz

CONTENTS

1.1 INTRODUCTION

This chapter covers many of the methods of depositing and etching both dielectric and conducting films used today in semiconductor manufacturing as well as the basic principles behind them. Some specialized techniques such as beam deposition and chemical mechanical polishing (CMP) are covered in Chapter 6.

A brief overview of deposition techniques can be found in Table 1.1 and of etching in Table 1.2.

1.2 EVAPORATION

Sputtering has almost completely displaced evaporation as a method of deposition because of its superior control of alloy composition, step coverage/hole fill by substrate biasing, ease of integration into cluster tools, etc. Since there are some applications of evaporation, particularly for forming lift-off metal patterns, a brief review of the technique is included.

Evaporation is usually used for metal deposition but has also been used to deposit some nonmetallic compounds (e.g., SiO, MgO). Early reviews of evaporation principles and equipment can be found in Holland (1961) and in Glang (1970); a later one is in Bunshah (1982). A review of some of the basics of high-vacuum technology can be found in Glang et al. (1970).

Glang distinguished the steps of the evaporation process: (1) transition from a condensed phase (solid or liquid) into a gaseous phase, (2) transport of the vapor from source to substrate at reduced

Table 1.1 Deposition Methods

Method	Materials Deposited	General Comments
Evaporation[a]	Pure metals; alloys; compounds	High-vacuum process; need adequate vapor pressure; various support materials;[b] single/multiple sources for alloys; reactive evaporation
Sublimation	Metals; compounds	Used when very high temperature is needed
Sputtering[c]	Pure metals; alloys; compounds; dielectrics	Can control film properties; control stoichiometry of alloys; use bias, high-density plasma, magnetic enhancement, ICP, IMP; directional deposition using collimation, large source-to-substrate distance
CVD/PECVD/ALD[d]	Pure metals; alloys; dielectrics	Better step coverage/gap fill; film composition and properties by choice of reactants, deposition conditions; commercial cluster systems; operating parameters, bias, temperature
Plating[e]	Pure metals; alloys	Hole fill; film properties through bath control
Spin coat[f]	Soluble, dispersible materials: organic insulators	Planarization; step coverage; curing to remove solvents or promote reactions
Beams[g]	Metals; dielectrics	

[a] Source heating: resistance heaters, RF induction heaters, e-gun.
[b] Crucibles, wires, foils.
[c] Metals: DC or RF; dielectrics: RF; option of DC or RF reactive sputtering.
[d] Includes high-density PECVD systems.
[e] Electroless; electrolytic.
[f] Examples: polyimides, xerogels, FOx, SiLK; one report of Cu spin-on.
[g] Beams covered in Chapter 6.

Table 1.2 Etching for Pattern Definition

Method	Materials Etched	General Comments
Wet chemical	Conductors, insulators, silicon	Almost always isotropic[a]; form a soluble product; need insoluble mask with good adhesion; mask profile not important; usually selective, batch processing
Sputter etch, ion-beam etching	All above	Poor selectivity; faceting, trenching, possible vertical etch; redeposition, possible substrate damage; slow, ion beam (single-wafer mode), sputter etch single or batch mode; used in dep-etch gap fill; angle-dependent etch
Reactive plasma, RIE, RSE, RIBE	Widely used in BEOL	Product needs to be volatile/desorbed by ions; high selectivity possible; profile control: both anisotropic and isotropic;[b] mask profile, erosion; redeposition, trenching, and substrate damage issues; aspect ratio-dependent etch rates; batch, single wafer (cluster); high etch rates attainable

[a] Directionality possible in some cases: e.g., "slow" etched for Si which follow crystal planes; columnar structure resulting in vertical profile (Mo).
[b] Anisotropy vs. isotropy: depends on many factors: reactants, etch parameters, ion energy, sidewall protection, etc.

gas pressure, and (3) condensation of the gas at the substrate. The stages of film growth following condensation of the vapor were outlined by Neugebauer (1970): (1) nucleation and island growth, (2) coalescence of islands, (3) channel formation, and (4) formation of a continuous film.

The source that contains the evaporant must have a negligible vapor pressure at the operating temperature and must not react with the evaporant. There are many types of sources and materials (Holland, 1961; Glang, 1970; Bunshah, 1982), e.g., crucibles of refractory oxides, nitrides,

carbides, and metals, refractory metal wires, and foils of various designs and shapes (Mathis Co. bulletins). Some materials, such as Cr, Mo, Pd, Si, can be sublimed which relaxes the temperature stability requirements for the source. Vaporization is accomplished by the use of resistance, induction, or electron bombardment heating; several configurations of electron guns (e-guns) are described by Bunshah. Many types are available commercially. E-guns are now used most commonly, except where radiation damage may be a problem, e.g., causing flat-band shifts in FET devices. In properly controlled e-gun evaporation, a shell of solid material shields the molten mass from the crucible, preventing interaction between the evaporant and the hearth. Multiple-pocket crucibles are also available. They may be used for sequential evaporation of different films. Or, using several guns simultaneously, with appropriate control of the source temperatures, multiple component films of a desired composition may be deposited (Glang, 1970). Alloy sources have also been used; the component ratio of the source is adjusted so that the deposited film has the required composition, although the vapor pressures of the constituents are different. The source composition is usually determined empirically. Flash evaporation, in which small quantities of the constituents in the desired ratio are completely evaporated, is another way of depositing alloy films and many kinds of dispensers have been used (Glang, 1970). However, whatever the evaporative technique, the control of the composition is rarely as reliable as that obtained by sputtering an alloy target.

Evaporation is carried out at very low pressures, e.g., 10^{-5} to 10^{-8} torr. At these low pressures, the mean free path is very large compared to the source to substrate distance, so that the transport of the vapor stream is collisionless. The emission pattern of the evaporating species is directional; it is described by a cosine law: $dM/dA = M/\pi r^2(\cos\phi \cos\theta)$ which is illustrated in Figure 1.1. The profile of the emitted flux is shown in Figure 1.2. A comprehensive discussion can be found in Neugebauer (1970).

Since the thickness of the deposited film is greatest directly in line with the source and decreases to either side, uniformity requires the use of planetary (rotating) substrate holders tailored to the particular deposition requirements. Typical of the holders available commercially is the so-called normal-angle-of incidence fixture (Figure 1.3a), which is used for high uniformity and minimum step coverage, suitable for lift-off processes. Another type (Figure 1.3b) has additional planets which rotate at a higher speed and is designed for good step coverage as well as uniformity. Radiant substrate heating, using refractory wires or quartz lamps, is required because the properties

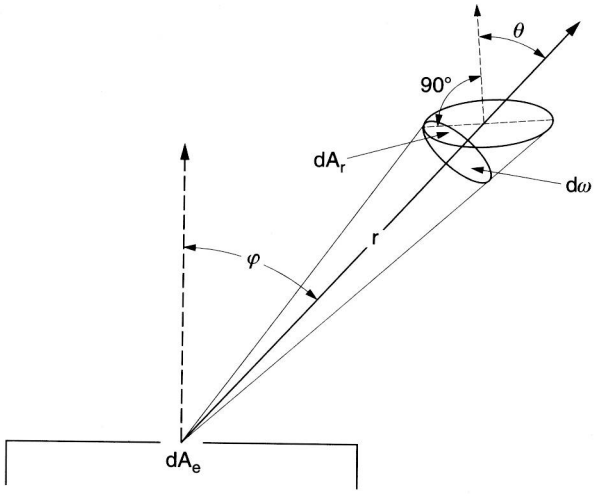

Figure 1.1 Evaporation from a point source dA_e onto a receiving surface element dA_r.

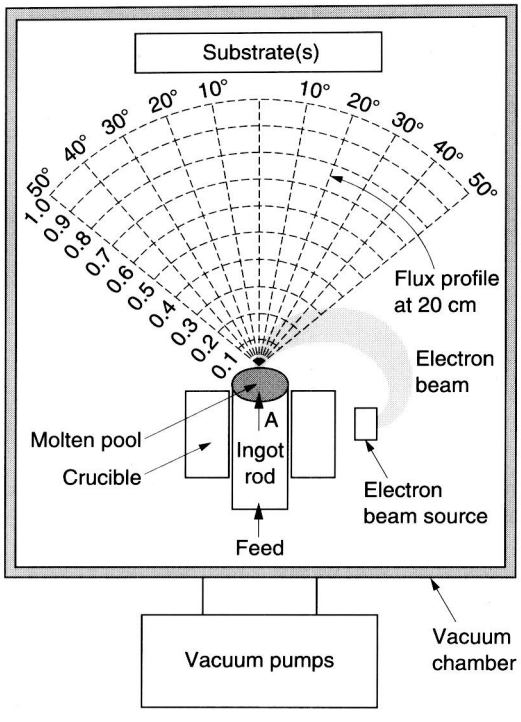

Figure 1.2 Profile of emitted flux. (From Bunshah, R.F., Ed., *Deposition Technologies for Films and Coatings*, Noyes Publications, Park Ridge, NJ, 1982.)

of the deposited thin films are dependent upon the deposition temperature. Temperature monitors and controllers are, therefore, also needed.

There are several kinds of thickness monitors, e.g., ionization gauges and particle impingement rate monitors, for the vapor stream. Crystal oscillators are used most frequently to measure the deposited mass; they utilize the piezoelectric properties of quartz. A thin crystal is part of an oscillator circuit so that the AC field induces thickness-shear oscillations whose frequency is inversely proportional to the crystal thickness; increasing the mass of deposit decreases the frequency. The crystal used has a specific orientation known as the AT cut, because this orientation exhibits the smallest temperature dependence. The thinner the crystal, the greater the sensitivity, if the mass deposited is small with respect to the wafer thickness. For a quartz thickness of 0.28 mm, and an initial frequency of 6 MHz, the change of frequency/thickness is 81.5 Hz/μg/cm (Wagendristel and Wang, 1994). The availability and simplicity of use makes the crystal oscillator preferable to microbalances. Interferometry is used for transparent films. For metals, optical techniques such as light absorption, transmittance and reflectance techniques, as well as resistance monitoring have also been used, but with less success. Thickness control is achieved by simply following the thickness monitor and stopping the process when the desired thickness is reached. Rate control is more complex; it requires adjustment of the source temperature, which means that a measurement and feedback mechanism is required.

The brochures supplied by equipment manufacturers are an excellent source of detailed information about the currently available evaporation systems and their operation. *In situ* sputter cleaning prior to evaporation of a metal film into a via hole is used to remove a contaminant film which causes high interfacial resistance (Bauer, 1994). When the lower surface is aluminum, the native oxide can be regrown quickly after sputter cleaning, due to the presence of residual water vapor.

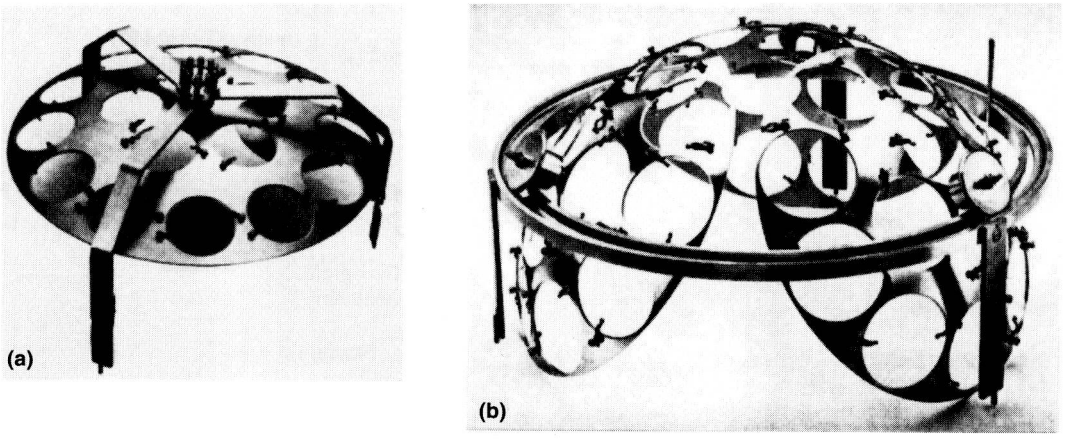

Figure 1.3 Substrate holders for evaporators: (a) normal angle of incidence fixture; (b) planetary fixture. (From Temescal Co., Airco coating technology bulletins. With permission.)

Sputtering of an aluminum electrode, before exposing the wafers to the plasma, is an efficient way of reducing the partial pressure of water vapor, thereby eliminating the need for prolonged sputter cleaning.

1.3 CHEMICAL VAPOR DEPOSITION

1.3.1 Introduction

The term chemical vapor deposition, CVD, used without modifiers, refers to a thermally activated reaction. Plasma and photon activation have also been used; these processes are called plasma-enhanced CVD (PECVD) and photon-enhanced CVD (sometimes referred to as LACVD, for laser-activated CVD) and are discussed elsewhere in this chapter. The term MOCVD refers to the use of an organometallic compound as a source gas in CVD. CVD processes have been used in the preparation of both metallic and insulating thin films as well as for depositing semiconductors. There are a number of reviews that contain more detailed information than can be covered here: Kern and Ban (1978), Sherman, (1987), Mitchener and Mahawili (1987), and Jensen (1989). There is also a book by Kodas and Hampden-Smith (1994). In addition, there are individual papers collected in CVD symposia proceedings volumes of the Electrochemical Society.

Because of temperature restraints imposed by interconnnection metallization, high-temperature CVD processes cannot be used for interlevel dielectrics but have been used for (usually) doped oxides to smooth the topography beneath the first interconnection level. CVD is being used to deposit metals (e.g., W, Al, Cu, Ti), nitrides of, for example, Ti and Ta, and various silicides. Currently, important uses of CVD of metals are the deposition of (1) thin conformal metal films to line trenches (barriers and seed layers) and (2) thicker films to fill vertical via holes (the vertical interconnections are termed "plugs" or "studs") and to fill vertical vias and trenches of damascene structures.

A more recent development is atomic layer deposition (ALD) used to prepare *very* thin, continuous, conformal metal films for barriers and as seed layers in the electrodeposition of Cu. Discussions of specific CVD processes are postponed to the chapters covering the particular flms.

1.3.2 Principles

Film formation by chemical vapor deposition is a heterogeneous chemical reaction in which volatile reactants produce a solid film upon reaction at a hot surface. The sequential kinetic steps have been summarized by Jensen (1989) as follows:

"(1) mass transport in the bulk gas flow region from the reactor inlet to the deposition zone, (2) gas-phase reactions leading to the formation of film precursors, (3) mass transport of film precursors to the growth surface, (4) adsorption of film precursors on the growth surface, (5) surface diffusion of film precursors to growth sites, (6) incorporation of film constituents into growing film, (7) desorption of volatile byproducts of the surface reaction, (8) mass transport of byproducts in the bulk gas flow region away from the deposition zone toward the reactor exit."

Homogeneous gas-phase reactions must be suppressed since they are responsible for the formation of dust particles which become incorporated into the growing film, making it hazy and defective. In a thermally activated reaction, the dependence of rate on the temperature is given by the Arrhenius equation:

$$\ln (\text{rate}) = -E/RT + \text{constant}$$

where E is the energy of activation. However, if the deposition rate is controlled by the transport of the reactant, the rate will be approximately independent of temperature. In many CVD reactions, two regions are observed: (1) the surface rate-limited reaction (temperature controlled) and (2) the mass transport-limited reaction (temperature independent), as illustrated in Figure 1.4. In the latter, the surface reaction is fast relative to the transport of reactants. Temperature uniformity is critical for film uniformity for the first type of reactions. For the second type flow across the wafer surface is critical.

1.3.3 Reactors

1.3.3.1 Classification

One way of classifying CVD reactors is by the relative temperatures of the parts of the system: there is the hot-wall system in which the substrate and reactor walls are at the same temperature, and the cold-wall system in which the substrate is at a higher temperature than the walls so that deposition occurs only on the substrate. There is the possibility of contamination by

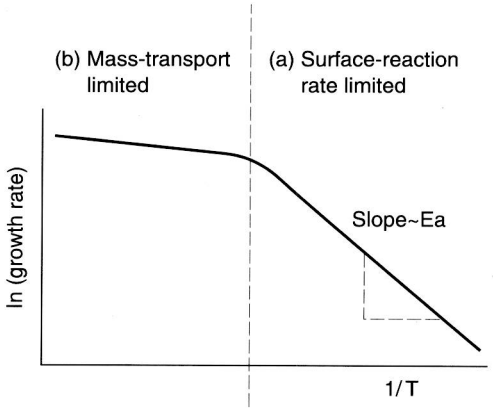

Figure 1.4 Deposition rate vs. temperature for CVD processes.

deposition on and subsequent flaking off the heated chamber walls. As pointed out by Kern and Ban (1978), the deposit is dense and adherent, and if not permitted to become too thick the problem of flaking may not be severe, particularly since there is no thermal cycling. Also, since the wafers are stacked vertically, any flakes would not be likely to fall on them. In the cold-wall reactor, this source of contamination is negligible, but convection due to temperature differentials can arise (Carlsson, 1985).

Another classification scheme is in terms of the pressure at which a reactor is operated. The earlier classifications were atmospheric pressure (APCVD) and low pressure (LPCVD) which covers a pressure range of about 0.05 torr to several torr. More recently, particularly for the deposition of SiO_2 films, both sub-atmospheric (SACVD; ~600 torr) and intermediate pressure (no acronym; ~60 torr) have been used. At higher pressures, the rates of mass transfer of the volatile reactants and byproducts and of reaction at the surface are about the same order of magnitude. Reducing the pressure increases the mass transfer rate so that reaction at the surface becomes the rate-limiting step. Reactor configuration greatly influences mass transport and thus is a critical factor for APCVD, but not for LPCVD. Uniform deposition is more easily achieved in LPCVD but the deposition rates are much lower than in APCVD.

Another way of classifying a reactor is by the deposition temperature: high temperature (HTCVD; ~750 to 950°C) and low temperature (LTCVD; below ~500°C). It can be seen that there are many possible combinations for CVD reactor and process design.

1.3.3.2 Examples of Reactors

Winkle and Nelson (1981) described a cold-wall low-temperature (LT) APCVD reactor, made by Watkins-Johnson. It is used for depositing undoped and P-doped SiO_2 and is shown in Figure 1.5. At temperatures of ~350 to 450°C, deposition rates as high as ~1 μm/min were achieved using mixtures of O_2 and the appropriate hydrides. A feature of this reactor is the gas injector design which improves surface reaction uniformity and coating efficiency and prevents homogeneous gas phase reactions.

An example of a hot-wall LPCVD system is shown in Figure 1.6; this is typical of reactors used to deposit insulators and metals. Two versions of an experimental single-wafer, LP cold-wall reactor, designed for selective W deposition from WF_6 and H_2, are shown in Figure 1.7 (Stoll and Wilson, 1986). In the system in Figure 1.7a, the substrate is heated radiantly by means of quartz lamps; in

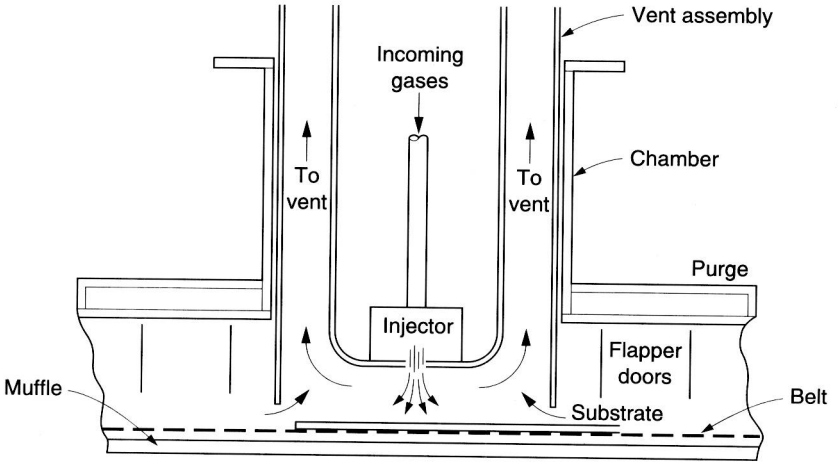

Figure 1.5 Schematic of an APCVD reactor. (Watkins-Johnson.)